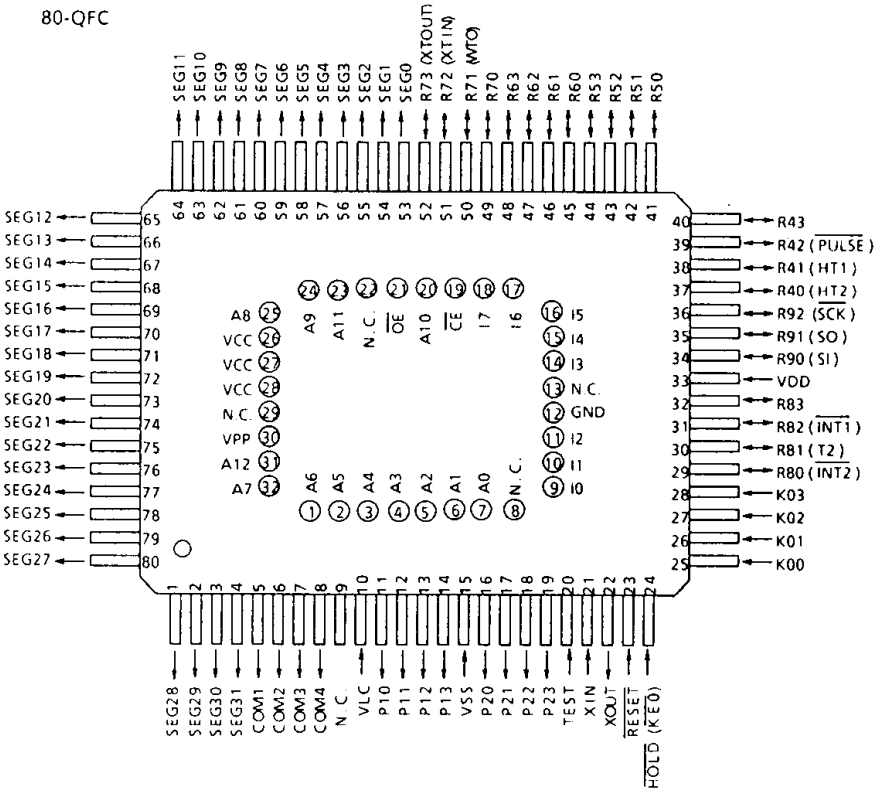
CMOS 4-BIT MICROCONTROLLER

# TMP47C020G

The 47C020, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C620/820 application systems (programs).
The 47C020 is pin compatible with the 47C620/820 which are mask-programed ROM devices.

## PIN ASSIGNMENT (TOP VIEW)

80-QFC




## PIN FUNCTION (Top of the package)

| PIN NAME | Input / Output | FUNCTIONS |
|---|---|---|
| A12 - A0 | Output | Program memory address output |
| I7 - I0 | Input | Program memory data input |
| $\overline{CE}$ | Output | Chip enable signal output |
| $\overline{OE}$ | | Output enable signal output |
| VCC | Power supply | + 5V (connected with VDD) |
| GND | | 0V (connected with VSS) |

## A.C. CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|
| Address Delay Time | $t_{AD}$ | $V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V | – | – | 150 | ns |
| Data Setup Time | $t_{IS}$ | $C_L$ = 100pF | 150 | – | – | ns |
| Data Hold Time | $t_{IH}$ | $T_{opr}$ = – 40 to 70°C | 50 | – | – | ns |

## NOTES FOR USE

(1) Program memory

The program areas are as shown in Figure 1.

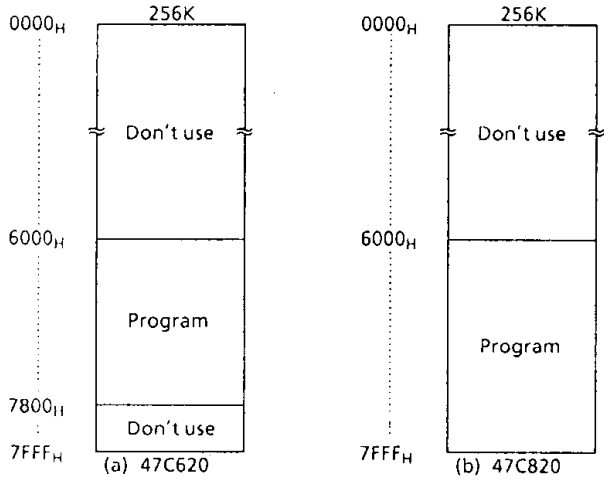



Figure 1. Capacity of EPROM and program area

(2) Data memory

47C020 contains two 256 x 4 bit data memory banks (DMB0, DMB1).

When 47C020 is used as the 47C620 evaluator, DMB1 has address space at addresses 00-FF$_H$ but do not write data to 80$_H$ and following addresses. DMB0 includes a special function common area so this need not be taken into consideration.

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C020 are similar to the code GA of the 47C620/820.

When this chip is used as evaluator with other I/O code (GB-GF), it is necessary to provide the external resistors.

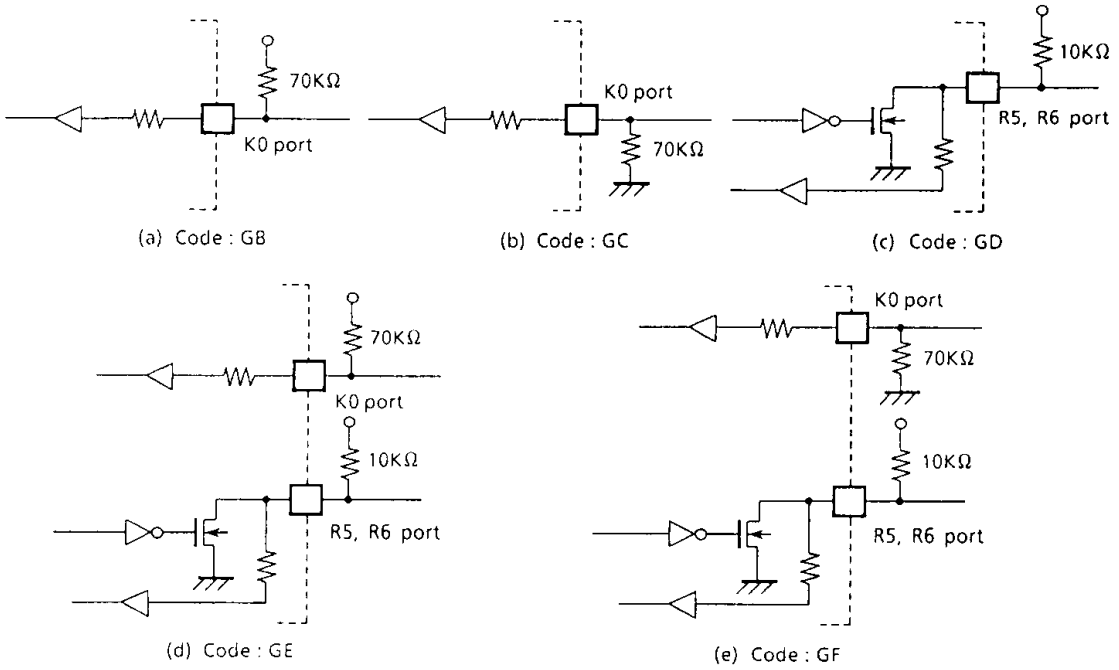



Figure2. I/O code and external circuitry