

### CMOS 8-bit Single Chip Microcomputer

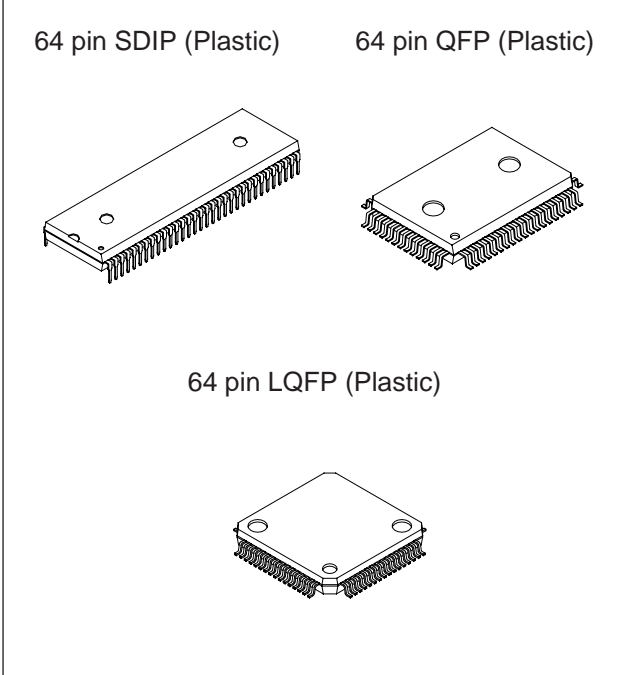
#### Description

The CXP86212/86216, CXP86324/86332, CXP86440/86448/86460 are the CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I<sup>2</sup>C bus interface, PWM output, remote control reception circuit, HSYNC counter, watchdog timer, 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, I/O ports.

The CXP86212/86216, CXP86324/86332, CXP86440/86448/86460 also provide a SLEEP function that enables to lower the power consumption.

#### Features

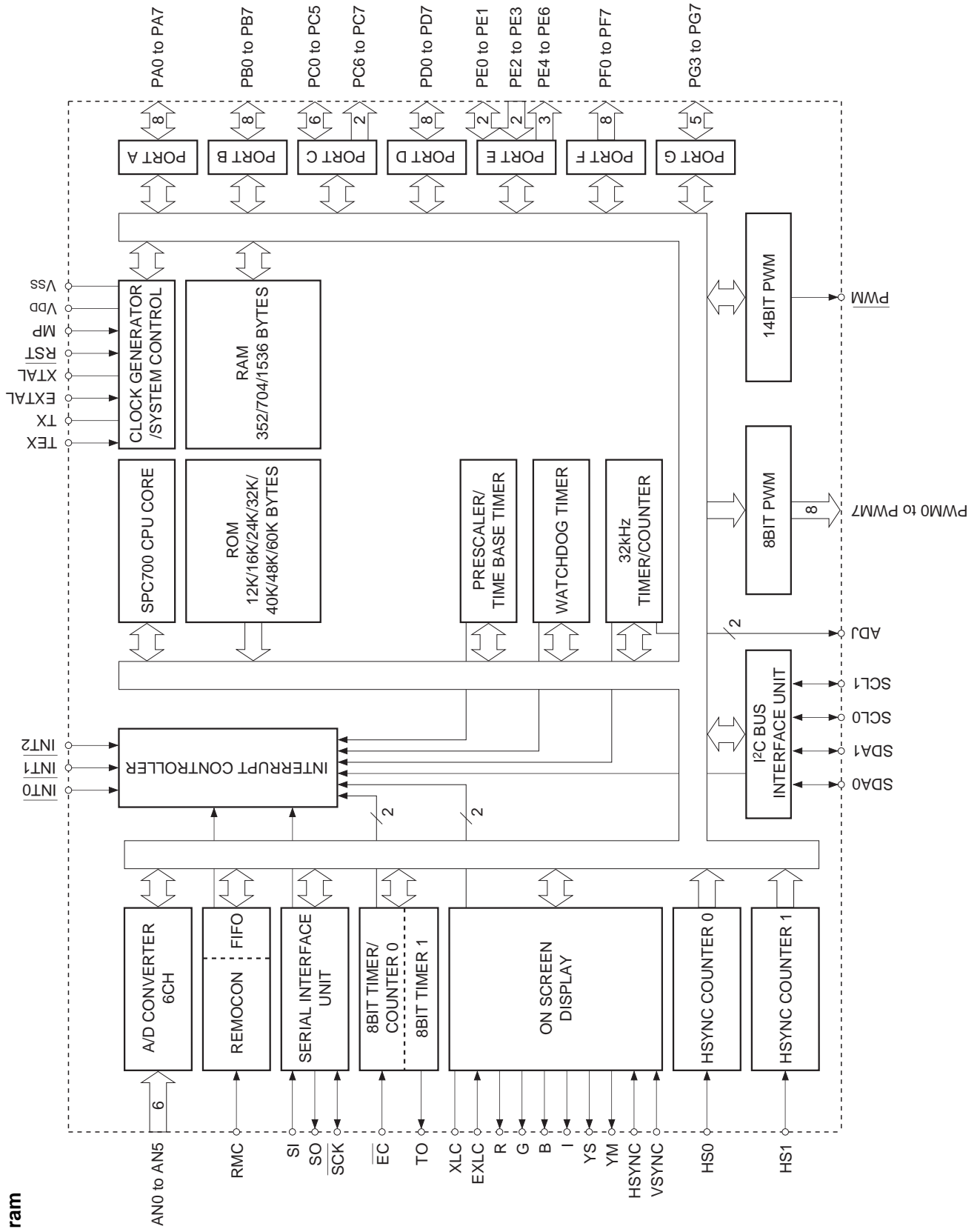
- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle      250ns at 16MHz operation  
 122µs at 32kHz operation
- Incorporated ROM                    12K bytes (CXP86212)  
 24K bytes (CXP86324)  
 40K bytes (CXP86440)  
 16K bytes (CXP86216)  
 32K bytes (CXP86332)  
 48K bytes (CXP86448)  
 60K bytes (CXP86460)
- Incorporated RAM                    352 bytes (CXP86212/86216) 704 bytes (CXP86324/86332) 1536 bytes (CXP86440/86448/86460)  
 (Excludes VRAM for on-screen display and sprite RAM)
- Peripheral functions
  - A/D converter                        8-bit 6-channel successive approximation method (Conversion time of 3.25µs at 16MHz)
  - Serial interface                      8-bit clock sync type, 1 channel
  - Timer                                    8-bit timer  
 8-bit timer/counter  
 19-bit time-base timer  
 32 kHz timer/counter
  - On-screen display (OSD) function    12 × 16 dots, 128 character types (CXP86212/86216),  
 256 character types (CXP86324/86332),  
 384 character types (CXP86440/86448/86460)  
 15 character colors, 2 lines × 24 characters,  
 frame background 8 colors/ half blanking,  
 background on full screen 15 colors/ half blanking  
 edging/ shadowing/ rounding for every line,  
 background with shadow for every character (CXP86440/86448/86460),  
 double scanning,  
 sprite OSD (CXP86440/86448/86460),  
 12 × 16 dots, 1 screen, 8 colors for every dot
  - I<sup>2</sup>C bus interface                      8 bits, 8 channels
  - PWM output                            14 bits, 1 channel
  - Remote control reception circuit    8-bit pulse measurement counter, 6-stage FIFO
  - HSYNC counter                        2 channels
  - Watchdog timer
- Interruption                            13 factors, 13 vectors, multi-interruption possible
- Standby mode                          Sleep
- Package                                 64-pin plastic SDIP/QFP/LQFP  
 CXP86400 64-pin ceramic PQFP  
 CXP86490 64-pin ceramic PSDIP (Supports custom font)
- Piggyback/evaluator



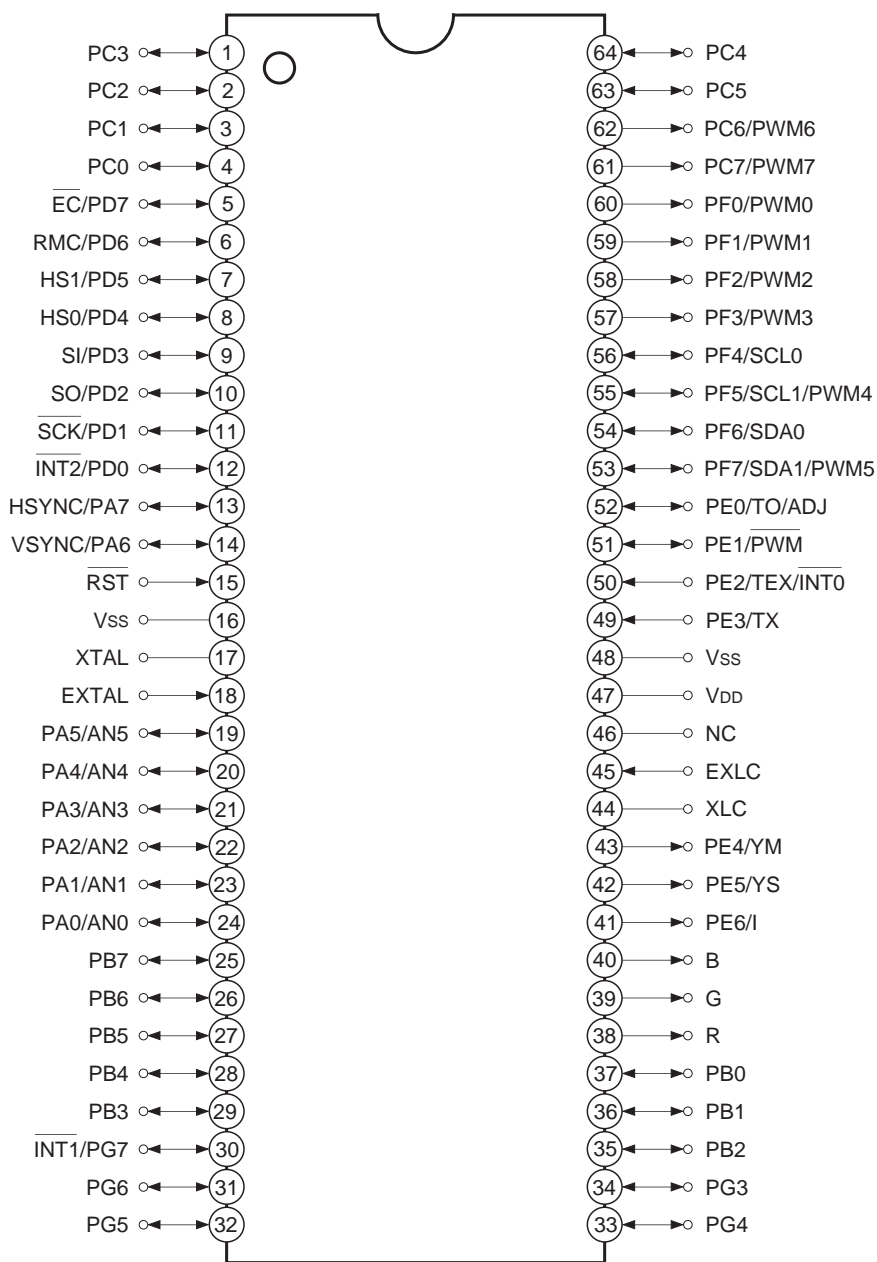
**Structure**  
Silicon gate CMOS IC

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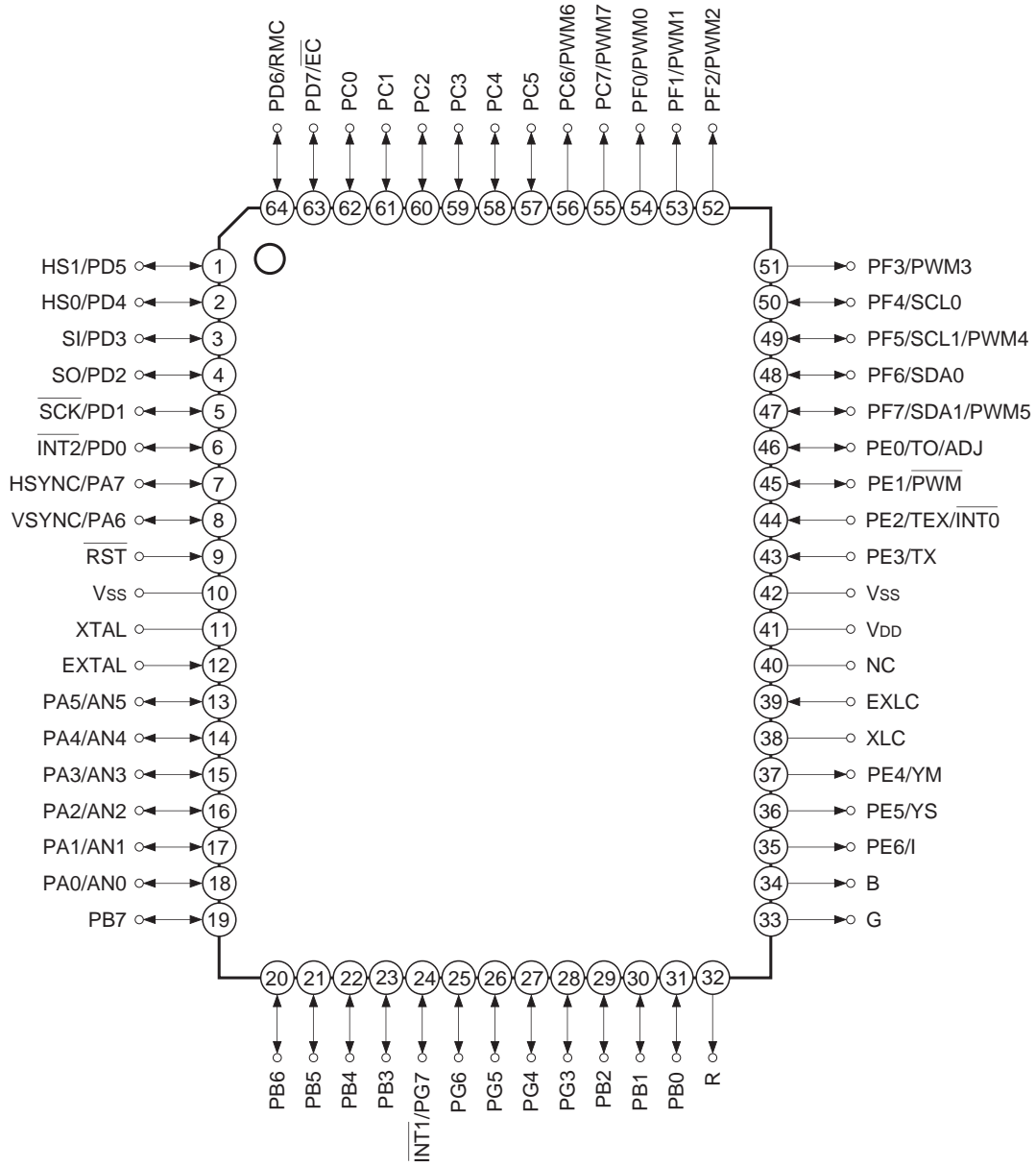
Pin Assignment (Top View) 64-pin SDIP



**Note)**

1. NC (Pin 46) is left open.
2. Vss (Pins 16 and 48) are both connected to GND.

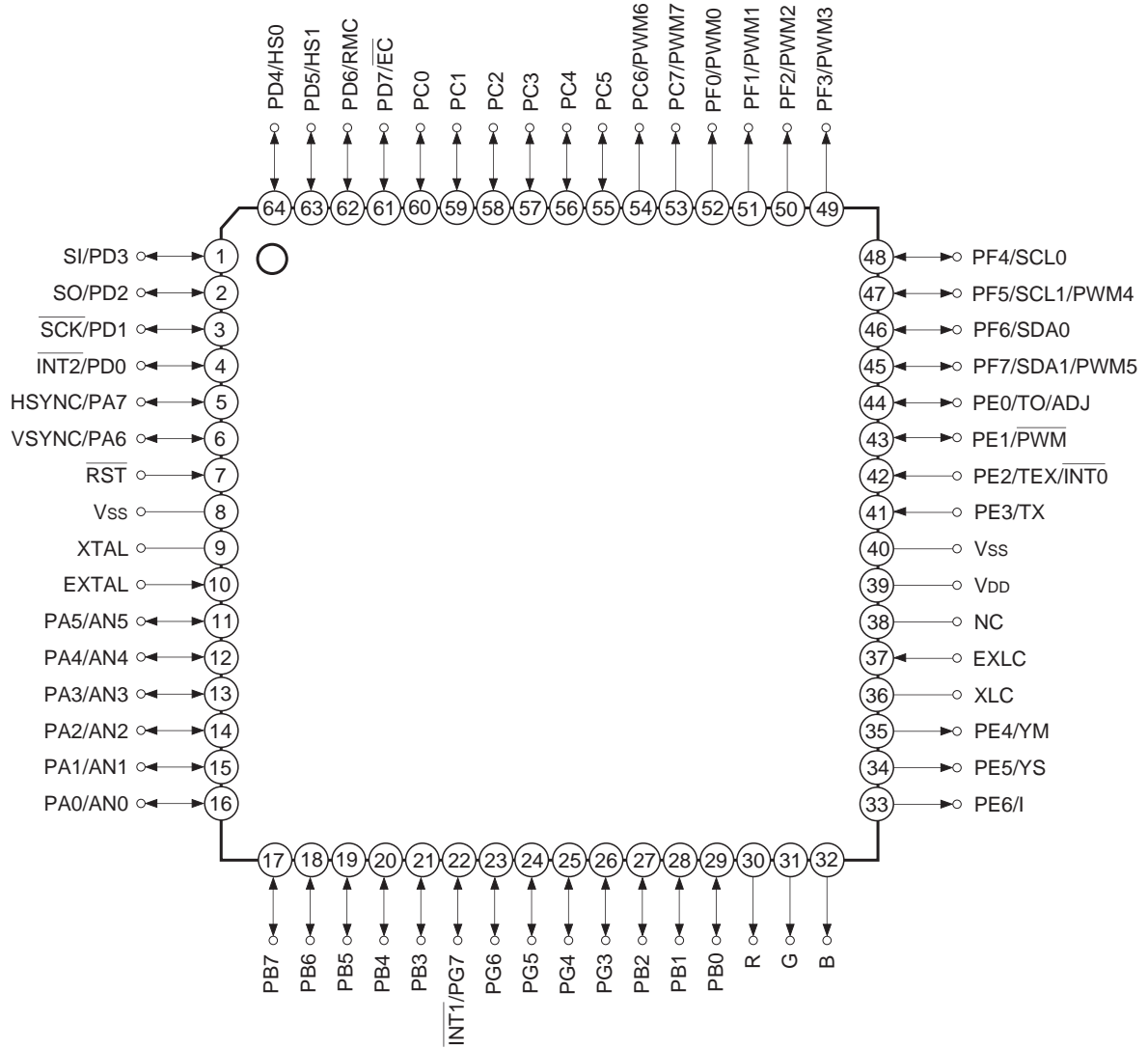
Pin Assignment (Top View) 64-pin QFP



**Note)**

1. NC (Pin 40) is left open.
2. Vss (Pins 10 and 42) are both connected to GND.

Pin Assignment (Top View) 64-pin LQFP



**Note)**

1. NC (Pin 38) is left open.
2. Vss (Pins 8 and 40) are both connected to GND.

**Pin Description**

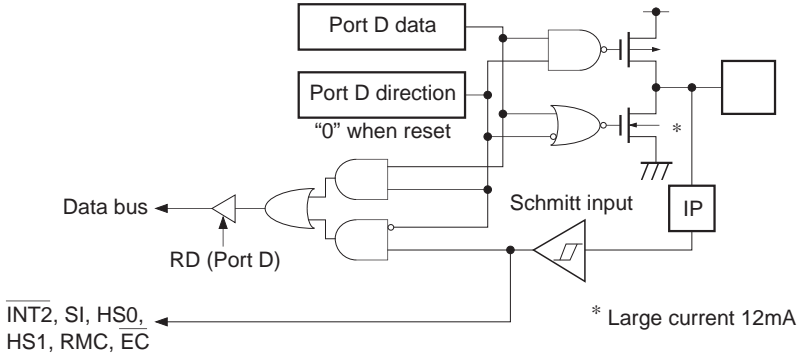
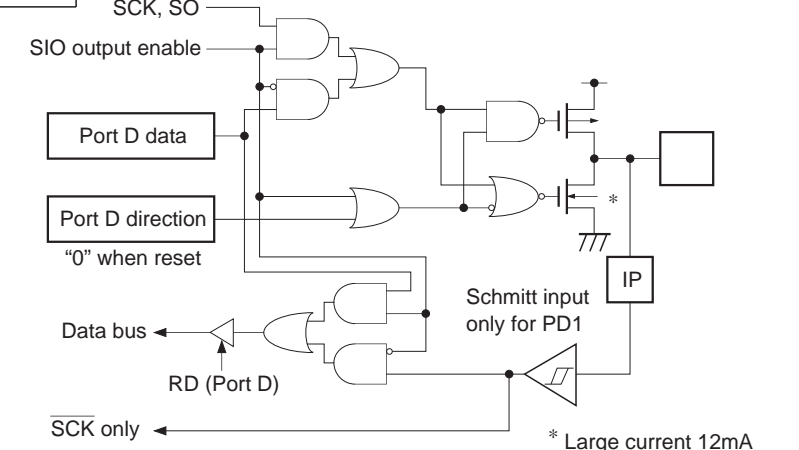
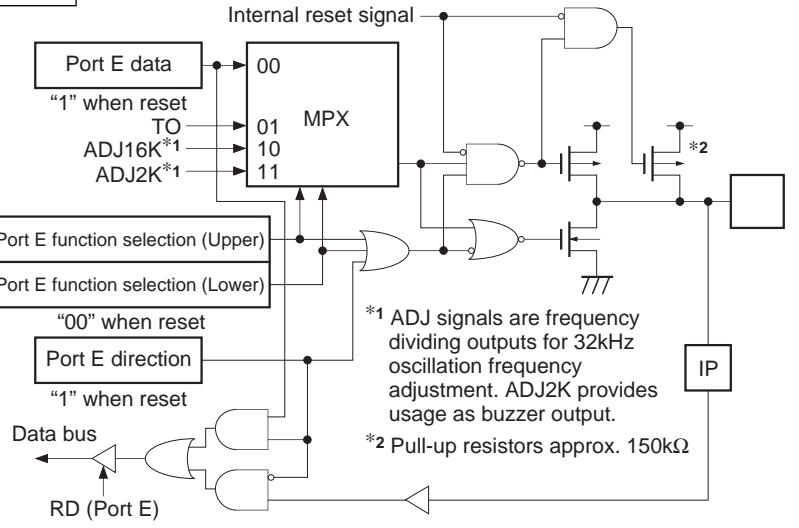
Symbol	I/O	Description	
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PC0 to PC5	I/O	(Port C) Lower 6 bits are I/O ports; I/O can be set in a unit of single bits. Upper 2 bits are output port and large current (12mA) N-channel open drain output. Upper 2 bits are medium drive voltage (12V); lower 6 bits are 5V drive. (8 pins)	
PC6/PWM6 to PC7/PWM7	Output/Output		8-bit PWM output. (2 pins)
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA synk current. (8 pins)	External interruption request input. Active at the falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.
PD6/RMC	I/O/Input		Remote control reception circuit input.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.
PE0/TO/ADJ	I/O/Output/ Output		
PE1/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output.
PE2/TEX/ $\overline{\text{INT0}}$	Input/Input/ Input	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)	Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.
PE3/TX	Input/Output		External interruption request input. Active at the falling edge.
PE4/YM	Output/Output		
PE5/YS	Output/Output		
PE6/I	Output/Output		
B	Output		OSD display 6-bit output. (6 pins)
G	Output		
R	Output		

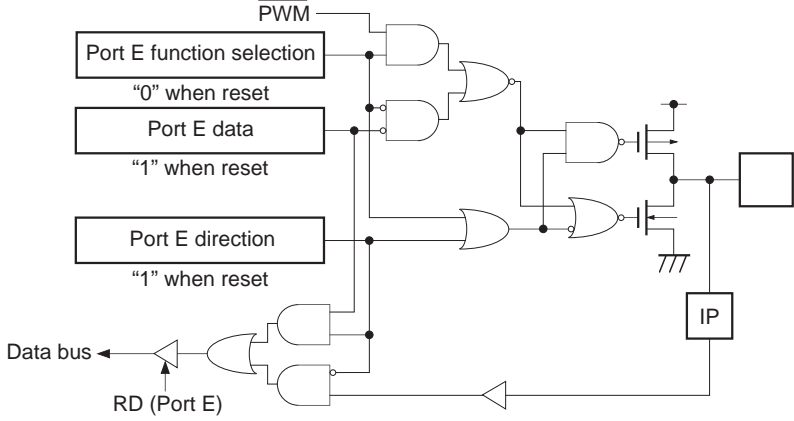
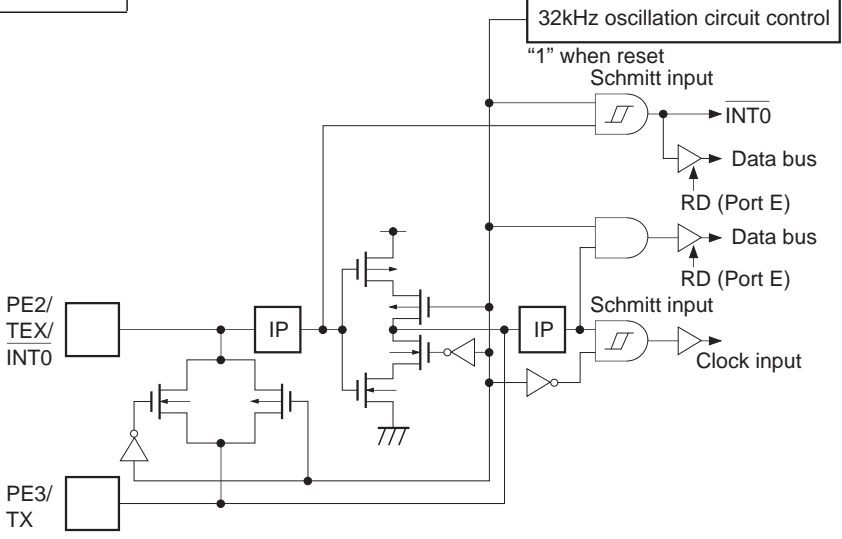
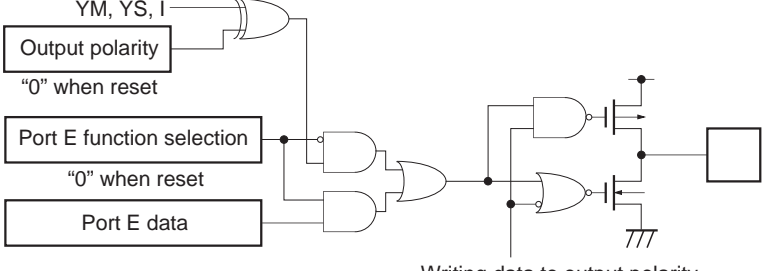
Symbol	I/O	Description	
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-channel open drain output. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (4 pins)
PF4/SCL0	Output/I/O		I <sup>2</sup> C bus interface transfer clock I/O. (2 pins)
PF5/SCL1/PWM4	Output/I/O/Output		
PF6/SDA0	Output/I/O		I <sup>2</sup> C bus interface transfer data I/O. (2 pins)
PF7/SDA1/PWM5	Output/I/O/Output		
PG3 to PG6	I/O	(Port G) 5-bit I/O port. I/O can be set in a unit of single bits. (5 pins)	
PG7/ $\overline{\text{INT1}}$	I/O/Input	External interruption request input. Active at the falling edge.	
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.	
XLC	Output		
NC		No connected.	
V <sub>DD</sub>		Positive power supply.	
V <sub>SS</sub>		GND. Connect two V <sub>SS</sub> pins to GND.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
<p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" when reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>IP</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PA6/VSYNC PA7/HSYNC</p> <p>2 pins</p>	<p>Port A</p> <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>HSYNC, VSYNC</p> <p>Schmitt input</p> <p>IP</p> <p>Input polarity "0" when reset</p>	<p>Hi-Z</p>
<p>PB0 to PB7 PC0 to PC5 PG3 to PG6 PG7/INT1</p> <p>19 pins</p>	<p>Port B</p> <p>Port C</p> <p>Port G</p> <p>Ports B, C, G data</p> <p>Ports B, C, G direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports B, C, G)</p> <p>Schmitt input only for PG7</p> <p>IP</p> <p>INT1</p>	<p>Hi-Z</p>
<p>PC6/PWM6 PC7/PWM7 PF0/PWM0 to PF3/PWM3</p> <p>6 pins</p>	<p>Port C</p> <p>Port F</p> <p>PWM0 to PWM3 PWM6, PWM7</p> <p>Ports C and F function selection "0" when reset</p> <p>Ports C and F data "1" when reset</p> <p>IP</p> <p>* 12V drive voltage Large current 12mA</p>	<p>Hi-Z</p>



Pin	Circuit format	When reset
<p>PD0/<math>\overline{\text{INT2}}</math>                      PD3/SI                      PD4/HS0                      PD5/HS1                      PD6/RMC                      PD7/EC</p> <p>6 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PD1/<math>\overline{\text{SCK}}</math>                      PD2/SO</p> <p>2 pins</p>	<p>Port D</p>  <p>* Large current 12mA</p>	<p>Hi-Z</p>
<p>PE0/TO/ADJ</p> <p>1 pin</p>	<p>Port E</p>  <p>*1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*2 Pull-up resistors approx. 150k<math>\Omega</math></p>	<p>High level                      (with                      approximately                      150k<math>\Omega</math>                      resistor when                      reset)</p>

Pin	Circuit format	When reset
<p>PE1/PWM</p> <p>1 pin</p>	<p>Port E</p> 	<p>High level</p>
<p>PE2/TEX/INT0 PE3/TX</p> <p>2 pins</p>	<p>Port E</p> 	<p>Oscillation halted Port input</p>
<p>PE4/YM PE5/YS PE6/I</p> <p>3 pins</p>	<p>Port E</p>  <p>Writing data to output polarity register and port data register brings output to active.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/SCL0 PF5/SCL1/PWM4 PF6/SDA0 PF7/SDA1/PWM5</p> <p>4 pins</p>	<p>Port F</p> <p>SCL, SDA</p> <p>I<sup>2</sup>C bus enable</p> <p>PWM4, PWM5</p> <p>Port F function selection "0" when reset</p> <p>Port F data "1" when reset</p> <p>Schmitt input</p> <p>SCL, SDA (I<sup>2</sup>C bus circuit)</p> <p>* Large current 12mA</p> <p>To internal I<sup>2</sup>C pins (SCL1 for SCL0)</p>	<p>Hi-Z</p>
<p>R G B</p> <p>3 pins</p>	<p>R, G, B</p> <p>Output polarity "0" when reset</p> <p>Writing data to output polarity register brings output to active.</p>	<p>Hi-Z</p>
<p>EXLC XLC</p> <p>2 pins</p>	<p>Oscillation control</p> <p>EXLC</p> <p>XLC</p> <p>OSD display clock</p>	<p>Oscillation halted</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	<p>EXTAL</p> <p>XTAL</p> <ul style="list-style-type: none"> <li>• Diagram shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop. (This device does not enter the stop mode.)</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	<p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>	<p>Low level</p>

**Absolute Maximum Ratings**

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0*1	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0*1	V	
Medium drive output voltage	V <sub>OUTP</sub>	-0.3 to +15.0	V	
High level output current	I <sub>OH</sub>	-5	mA	
High level total output current	∑I <sub>OH</sub>	-50	mA	Total of all output pins
Low level output current	I <sub>OL</sub>	15	mA	Ports excluding large current output (value per pin)
	I <sub>OLC</sub>	20	mA	Large current output ports (value per pin*2)
Low level total output current	∑I <sub>OL</sub>	130	mA	Total of all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	1000	mW	SDIP-64P-01
		600	mW	QFP-64P-L01
		380	mW	LQFP-64P-L01

\*1 V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3 V.

\*2 The large current output port is Port C (PC6, PC7), Port D (PD) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

**Recommended Operating Conditions**

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or sleep
		2.7	5.5	V	Guaranteed operation range for TEX mode
		—	—	V	Guaranteed data hold range for stop*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	*3
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*4, TEX pin*5
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	*3
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*4, TEX pin*5
Operating temperature	T <sub>opr</sub>	-20	+75	°C	

\*1 This device does not enter the STOP mode.

\*2 PA1 to 5, PB3 to 7, PC0 to PC5, PD2, PE0, PE1, PE3, PG3 to PG6, SCL0 to 1, SDA0 to 1 pins

\*3 V<sub>SYNC</sub>, H<sub>SYNC</sub>, INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, RST pins

\*4 Specifies only during external clock input.

\*5 Specifies only during external event count input. - 12 -

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA, PB, PC0 to PC5, PD, PE0 to PE1, PE4 to PE6, PG, R, G, B	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL	PA to PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG, R, G, B	VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
		PC6, PC7, PD, PF	VDD = 4.5V, IOL = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	VDD = 4.5V, IOL = 3.0mA			0.4	V
			VDD = 4.5V, IOL = 4.0mA			0.6	V
Input current	IiHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
	IiLE		VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IiHT	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
	IiLT		VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IiLR	RST*1	VDD = 5.5V, VIL = 0.4V	-1.5		-400	μA
I/O leakage current	IIZ	PA to PE, PG, R, G, B, RST*1	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Open drain I/O leakage current (in N-ch Tr off state)	ILOH	PC6, PC7, PF0 to PF3	VDD = 5.5V, VOH = 12.0V			50	μA
		PF4 to PF7	VDD = 5.5V, VOH = 5.5V			10	μA
I <sup>2</sup> C bus switch connection impedance (in output Tr off state)	RBS	SCL0: SCL1 SDA0: SDA1	VDD = 4.5V VSCL0 = VSCL1 = 2.25V VSDA0 = VSDA1 = 2.25V			120	Ω
Supply current*2	IDD1	VDD	1/2 frequency dividing mode		18	28	mA
			VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)				
	IDD2		VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF)		30	80	μA
			Sleep mode				
	IDDS1		VDD = 5.5V, 16MHz crystal oscillation (C1 = C2 = 15pF)		1.2	2.1	mA
			VDD = 3.3V, 32MHz crystal oscillation (C1 = C2 = 47pF)				
IDDS2			12	35	μA		
IDDS3	Stop mode*3 VDD = 5.5V, termination of 16MHz and 32MHz oscillation		—	—	—	μA	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	PA to PD, PE0 to PE3, R, G, B, PF4 to PF7, PG3 to PG7, $\overline{\text{EXTAL}}$ , TEX, EXLC, $\overline{\text{RST}}$	Clock 1 MHz 0V other than the measured pins		10	20	pF

\*1 For  $\overline{\text{RST}}$  pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

\*2 When all output pins are left open. Specifies only when the OSD oscillation is halted.

\*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig.2	8		16	MHz
System clock input pulse width	t <sub>XL</sub> , t <sub>XH</sub>	EXTAL	Fig. 1, Fig.2 External clock drive	28			ns
System clock input rise and fall times	t <sub>CR</sub> , t <sub>CF</sub>	EXTAL	Fig. 1, Fig.2 External clock drive			200	ns
Event count input clock pulse width	t <sub>EH</sub> , t <sub>EL</sub>	$\overline{EC}$	Fig. 3	4t <sub>sys</sub> *1			ns
Event count input clock rise and fall times	t <sub>ER</sub> , t <sub>EF</sub>	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5 V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t <sub>TL</sub> , t <sub>TH</sub>	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t <sub>TR</sub> , t <sub>TF</sub>	TEX	Fig. 3			20	ms

\*1 Indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

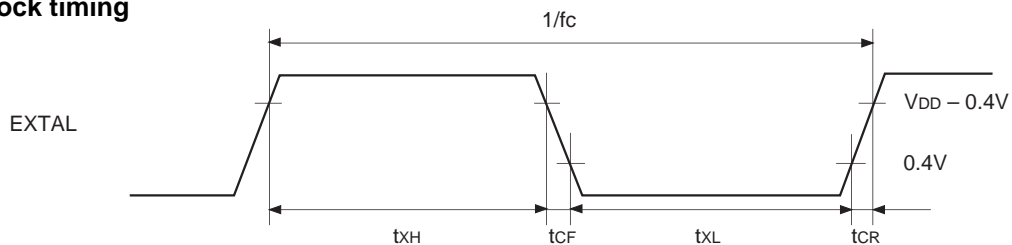


Fig.2. Clock applied conditions

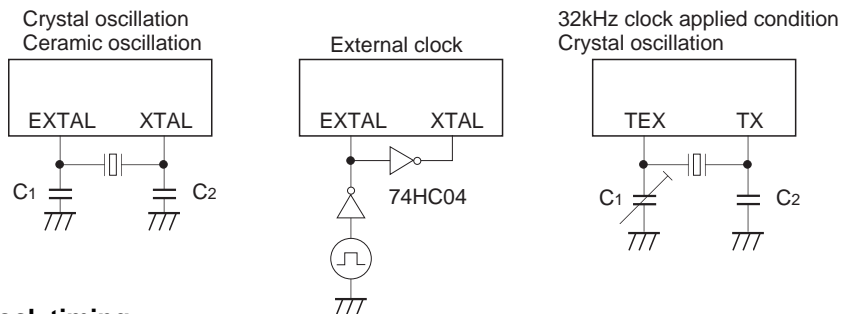
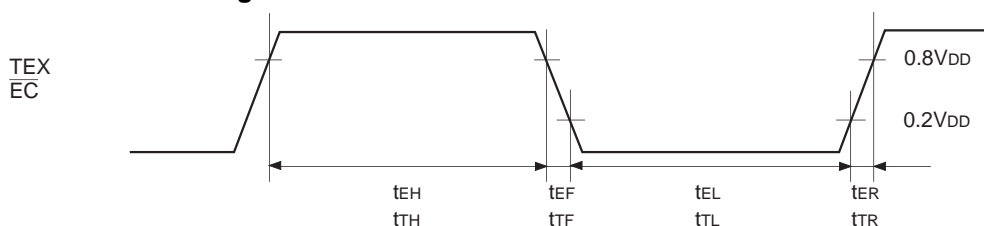


Fig. 3. Event count clock timing



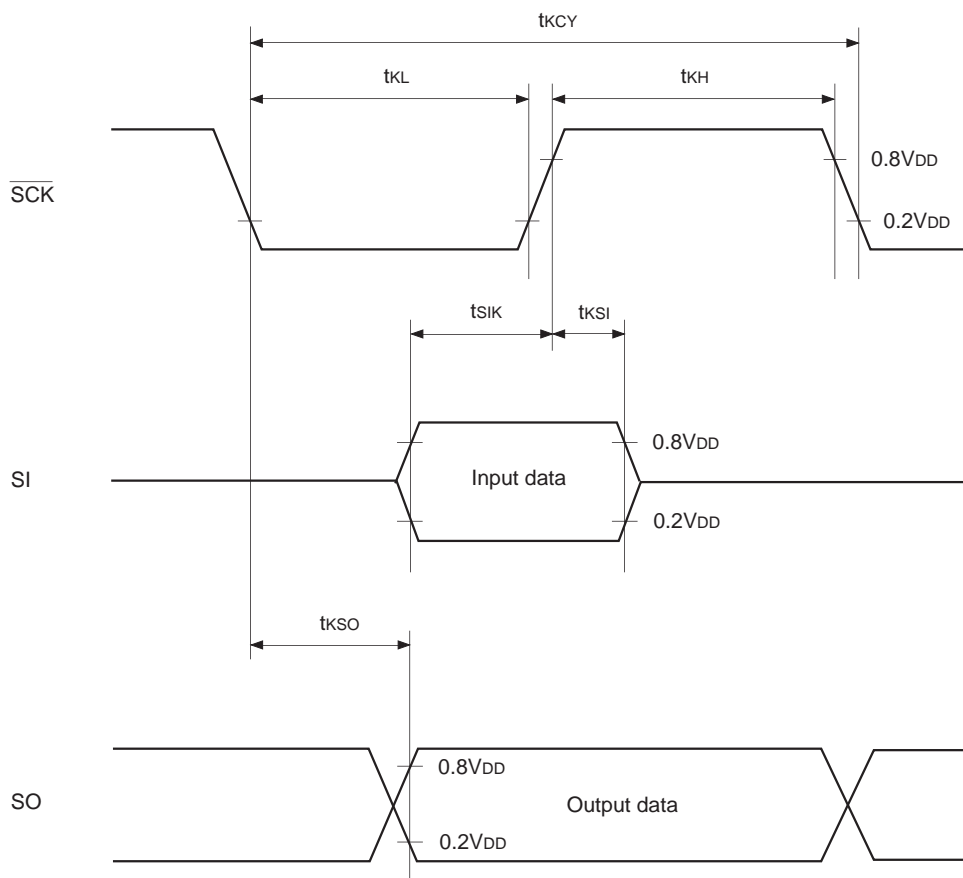
(2) Serial transfer

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level width	$t_{\text{KH}}$	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
	$t_{\text{KL}}$		$\overline{\text{SCK}}$ output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{SIK}}$	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$ )	$t_{\text{KSI}}$	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	$t_{\text{KSO}}$	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note)** The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing



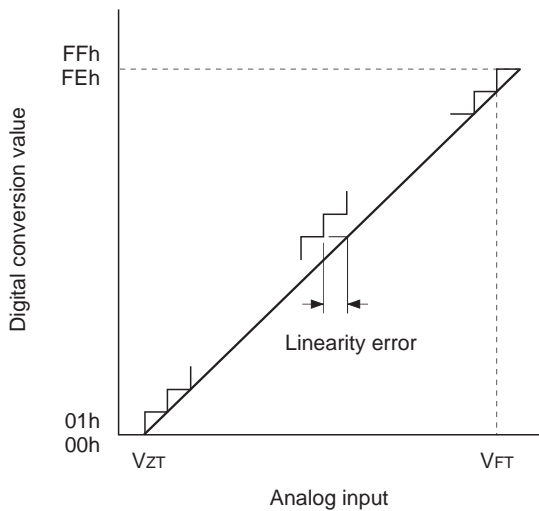


(3) A/D converter

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	VZT*1			-10	10	70	mV
Full-scale transition voltage	VFT*2			4910	4970	5030	mV
Conversion time	tCONV			26/fADC*3			µs
Sampling time	tSAMP			6/fADC*3			µs
Analog input voltage	VIAN	AN0 to AN5		0		VDD	V

Fig. 5. Definitions for A/D converter terms



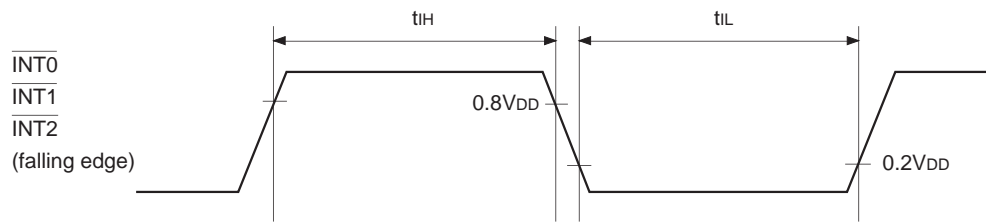
- \*1 VZT: Value at which the digital conversion value changes from 00h to 01h and vice versa.
- \*2 VFT: Value at which the digital conversion value changes from FEh to FFh and vice versa.
- \*3 fADC indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

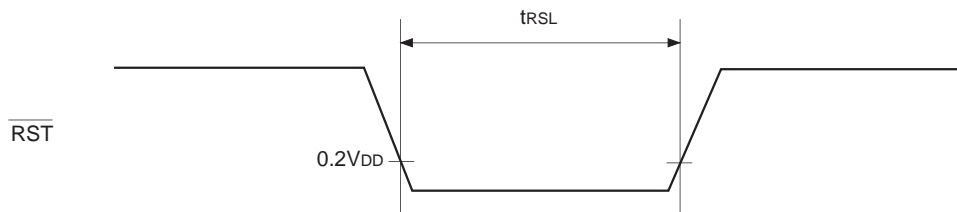
**(4) Interruption, reset input** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	$t_{IH}$ $t_{IL}$	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$		1		$\mu\text{s}$
Reset input Low level width	$t_{RSL}$	$\overline{\text{RST}}$		$32/f_c$		$\mu\text{s}$

**Fig. 6. Interruption input timing**



**Fig. 7.  $\overline{\text{RST}}$  input timing**



(5) I<sup>2</sup>C bus timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	SCL		0	100	kHz
Bus-free time before starting transfer	t <sub>BUF</sub>	SDA, SCL		4.7		μs
Hold time for starting transfer	t <sub>HD; STA</sub>	SDA, SCL		4.0		μs
Clock Low level width	t <sub>LOW</sub>	SCL		4.7		μs
Clock High level width	t <sub>HIGH</sub>	SCL		4.0		μs
Setup time for repeated transfers	t <sub>SU; STA</sub>	SDA, SCL		4.7		μs
Data hold time	t <sub>HD; DAT</sub>	SDA, SCL		0*1		μs
Data setup time	t <sub>SU; DAT</sub>	SDA, SCL		250		ns
SDA, SCL rise time	t <sub>R</sub>	SDA, SCL			1	μs
SDA, SCL fall time	t <sub>F</sub>	SDA, SCL			300	ns
Setup time for transfer completion	t <sub>SU; STO</sub>	SDA, SCL		4.7		μs

\*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

Fig. 8. I<sup>2</sup>C bus transfer timing

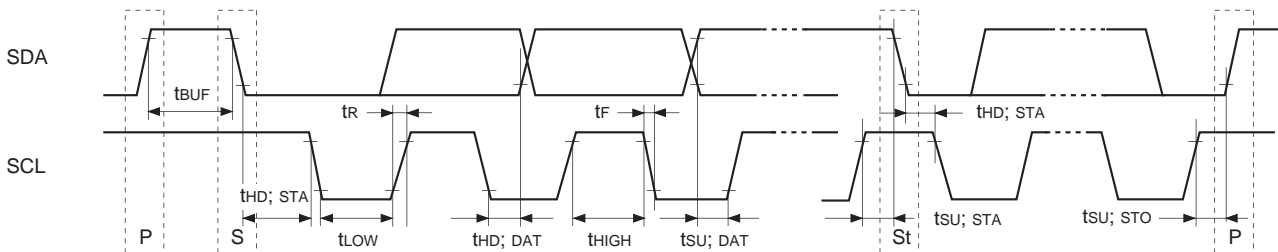
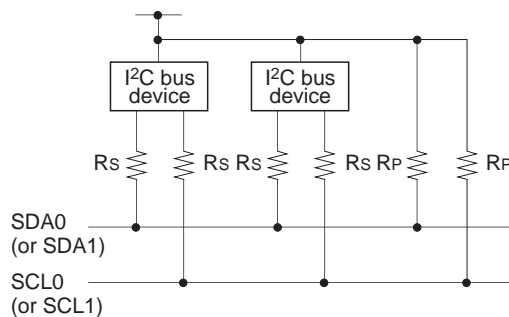


Fig. 9. I<sup>2</sup>C bus device recommended circuit



- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

**(6) OSD timing**

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

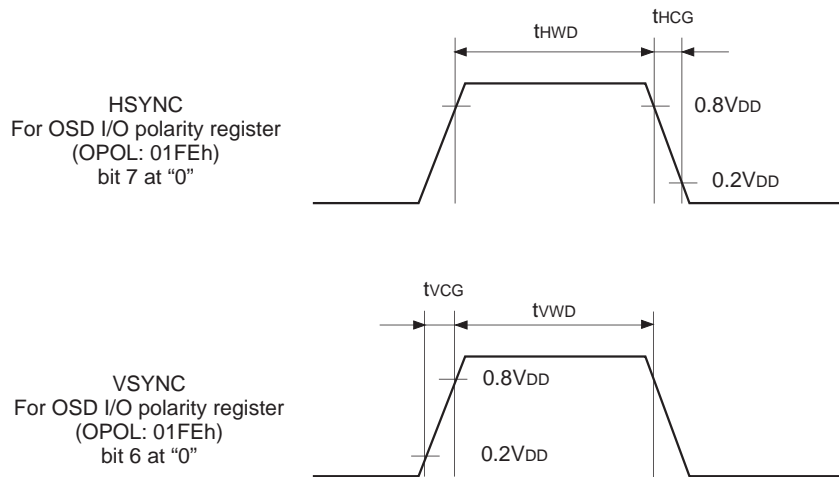
Item	Symbol	Pins	Conditions	Min.	Max	Unit
OSD clock frequency	fosc	EXLC XLC	Fig. 11	4	30.4	MHz
HSYNC pulse width	tHWD	HSYNC	Fig. 10	2		µs
VSYNC pulse width	tVWD	VSYNC	Fig. 10	1		H*2
HSYNC afterwrite rise and fall times	tHCG	HSYNC	Fig. 10		200	ns
VSYNC beforewrite rise and fall times	tVCG	VSYNC	Fig. 10		1.0	µs

\*1 The maximum value of fosc is specified with the following equation.

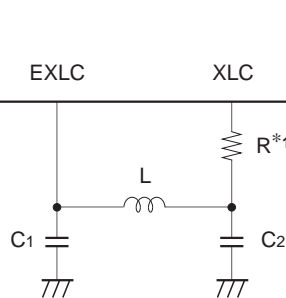
$$f_{osc} [max] \leq f_c \times 1.9$$

\*2 H indicates 1HSYNC period.

**Fig. 10. OSD timing**



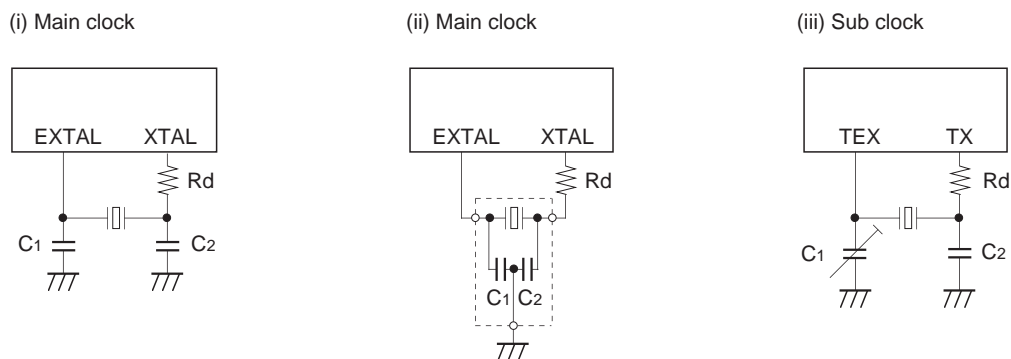
**Fig. 11. LC oscillation circuit connection**



\*1 The series resistor for XLC (R = 1kΩ or less) can reduce the frequency of occurrence of the undesired radiation.

Appendix

Fig. 12. Recommended oscillation circuit



Manufacture	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	Circuit example
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0* <sup>1</sup>	(i)
	CSA12.0MTZ	12.0				
	CSA16.00MXZ040	16.0	5	5		
	CST10.0MTW*	10.0	30	30		(ii)
	CST12.0MTW*	12.0				
	CST16.00MXW0C1*	16.0	5	5		
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330* <sup>1</sup>	(i)
		12.0	12	12		
		16.0	10	10		
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0* <sup>1</sup>	
		12.0	5	5		
		16.0	OPEN	OPEN		
	P3	32.768kHz	30	33	120k	(iii)

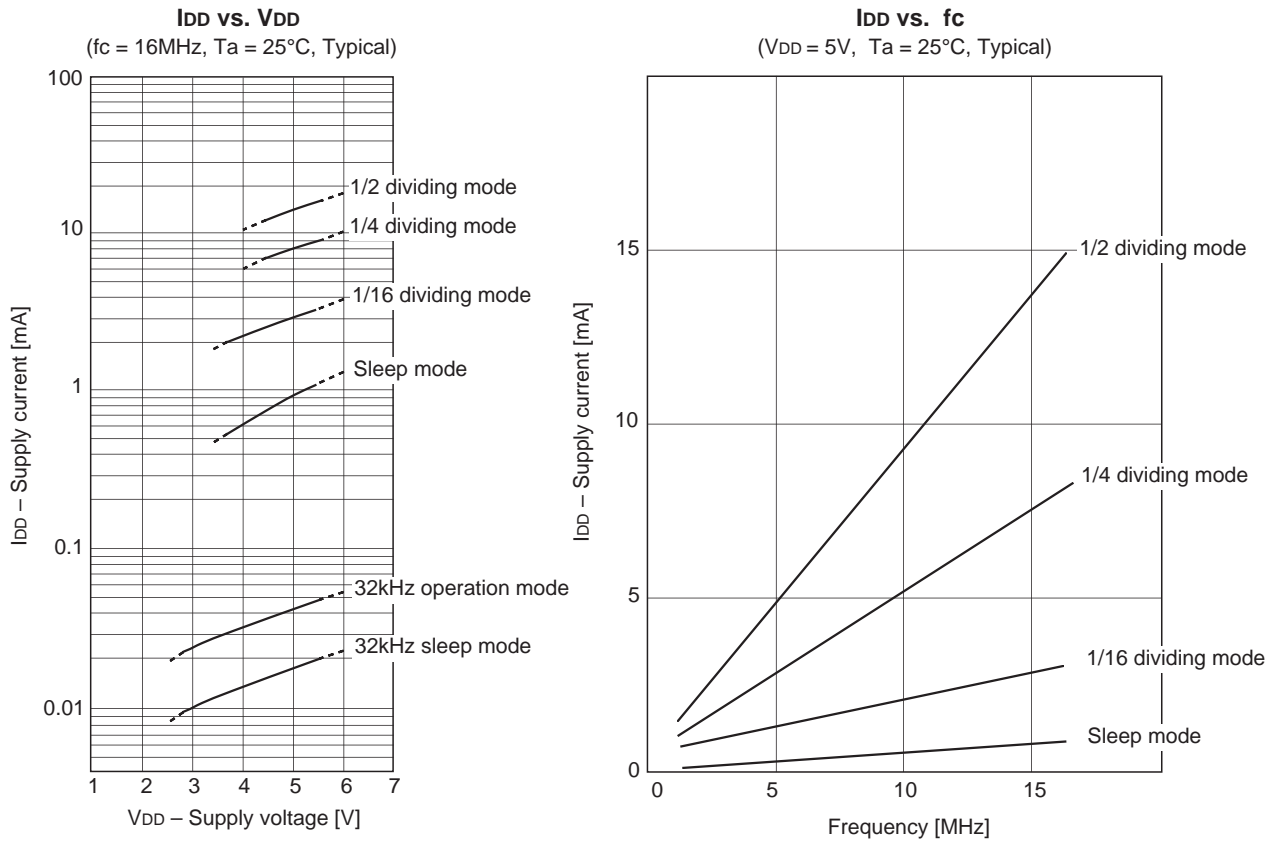
\* Models with an asterisk (\*) have the built-in ground capacitance (C1, C2).

\*1 The series resistor for XTAL (Rd = 500 $\Omega$  or less) can reduce the effect of the noise caused by the electrostatic discharge.

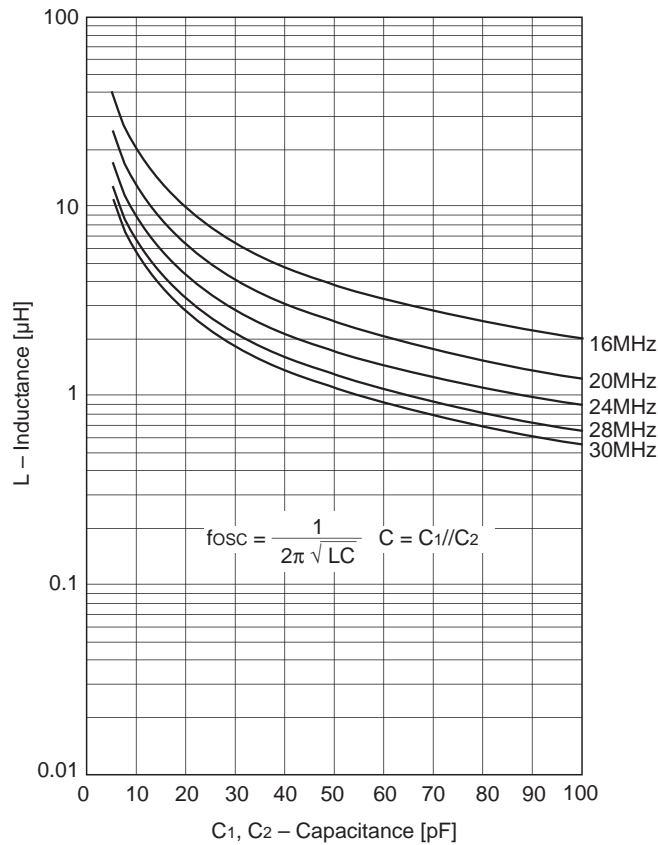
Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Fig. 13. Characteristic curves



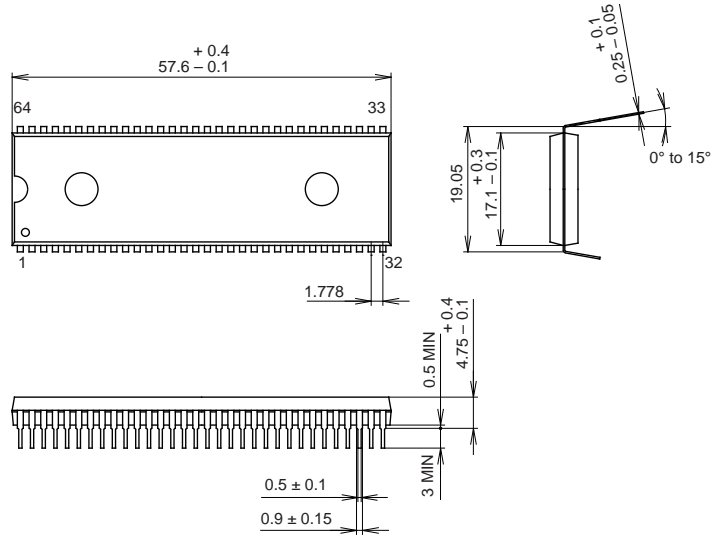
Parameter curve for OSD oscillator L vs. C  
(Analytically calculated value)



Package Outline

Unit: mm

64PIN SDIP (PLASTIC) 750mil

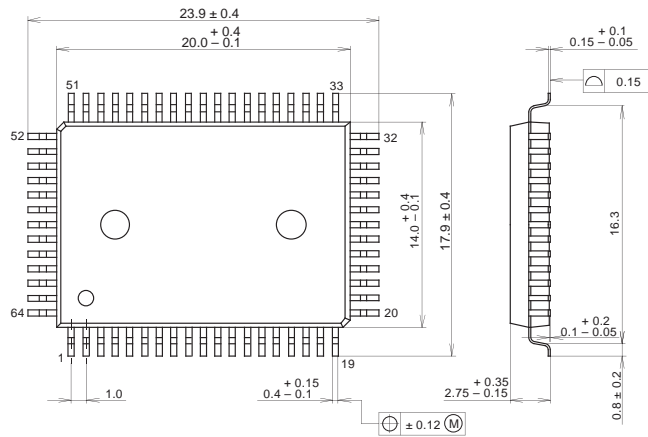


PACKAGE STRUCTURE

SONY CODE	SDIP-64P-01
EIAJ CODE	SDIP064-P-0750-A
JEDEC CODE	_____

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	8.6g

64PIN QFP(PLASTIC)

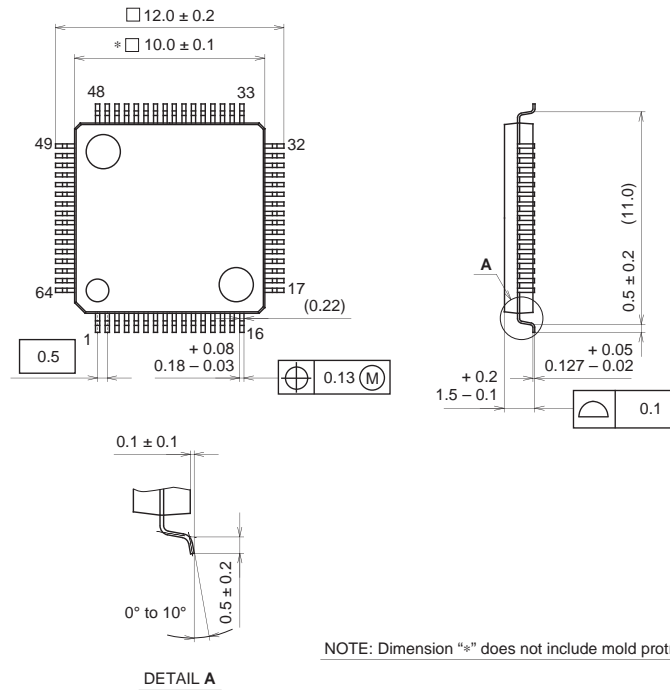


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	*QFP064-P-1420
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER /42 ALLOY
PACKAGE WEIGHT	1.5g

64PIN LQFP (PLASTIC)



SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g