Ordering number : EN5542A

Wideband Output Module (Video Pack)

VP603

CRT Display Video Output Amplifier: High-Voltage, Wideband Amplification

Function

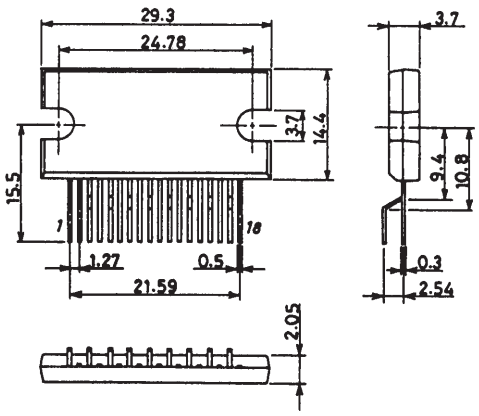
- Three-channel video output circuit for CRT displays
- Optimal for monitors that require $f_{VIDEO} \geq$ 70 MHz, 17-inch $f_H \geq 64$ kHz

Package Dimensions

unit: mm

2117

[VP603]



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
	V_{BB} max		15	V
Allowable power dissipation	Pd max	At Tc = 25°C with an ideal heat sink	25	W
Junction temperature	Tj max		150	°C
Case temperature	Tc max		100	°C
Storage temperature	Tstg		–20 to +110	°C

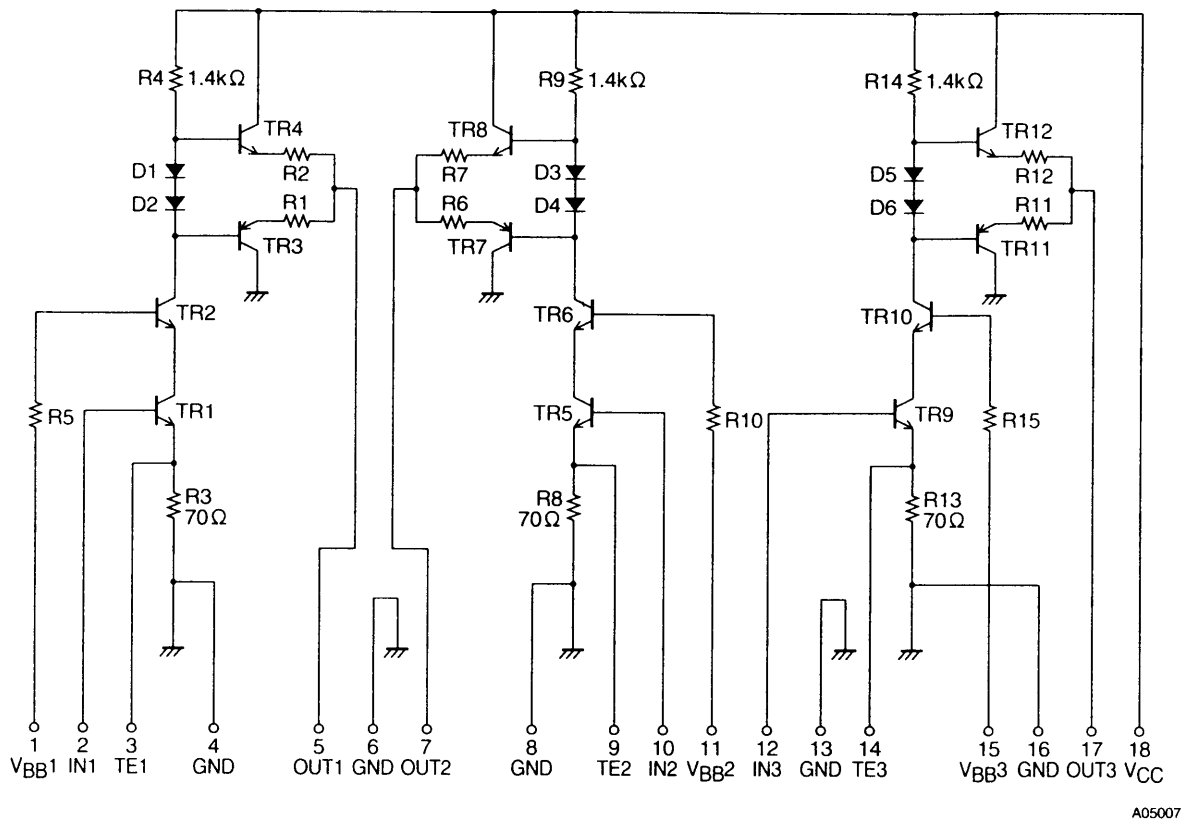
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage I	V_{CC}		70	V
	V_{BB}		10	V
Recommended supply voltage II	V_{CC}		80	V
	V_{BB}		10	V

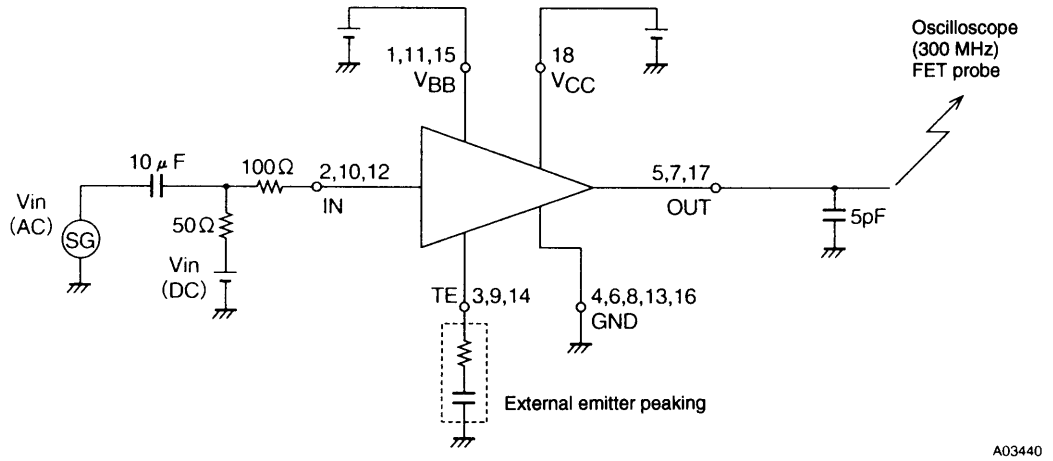
Electrical Characteristics at Ta = 25°C

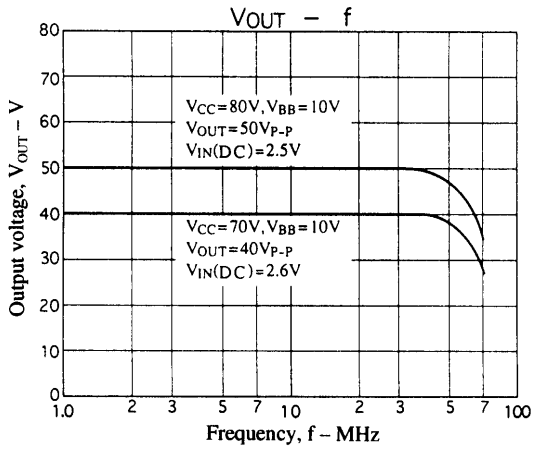
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Bandwidth I (–3 dB)	fc	V_{CC} = 70 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 2.5 V, V_{OUT} (p-p) = 40 V		75		MHz
Bandwidth II (–3 dB)	fc	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 2.7 V, V_{OUT} (p-p) = 50 V		70		MHz
Pulse response characteristics	tr	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 5 pF, V_{IN} (DC) = 2.7 V, V_{OUT} (p-p) = 40 V		5.2		ns
	tf			5.0		ns
Voltage gain	G_V (DC)		17	19	21	
Current drain I	$I_{CC}1$	V_{CC} = 70 V, V_{BB} = 10 V, V_{IN} (DC) = 2.3 V, f = 10 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 40 V		27		mA
	$I_{CC}2$	V_{CC} = 70 V, V_{BB} = 10 V, V_{IN} (DC) = 2.3 V, f = 70 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 40 V		40		mA
Current drain II	$I_{CC}1$	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.6 V, f = 10 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 50 V		32		mA
	$I_{CC}2$	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.6 V, f = 70 MHz clock, C_L = 5 pF, V_{OUT} (p-p) = 50 V		47		mA

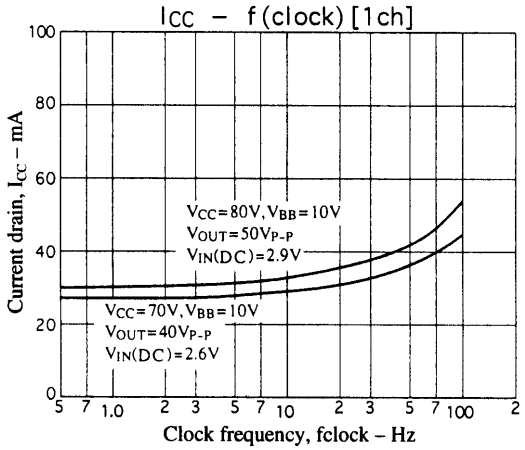
Internal Equivalent Circuit

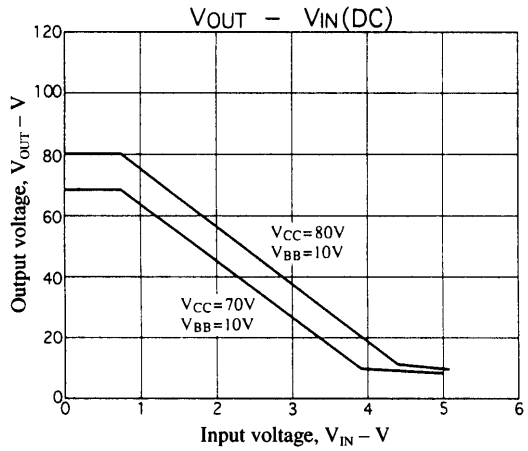


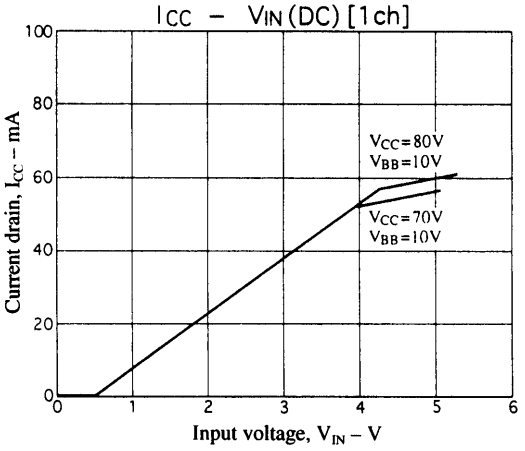
Test Circuit

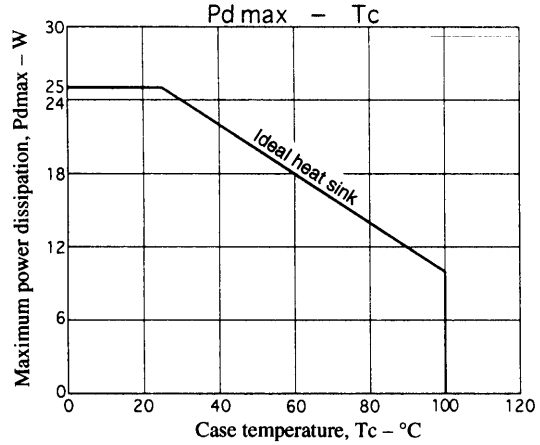






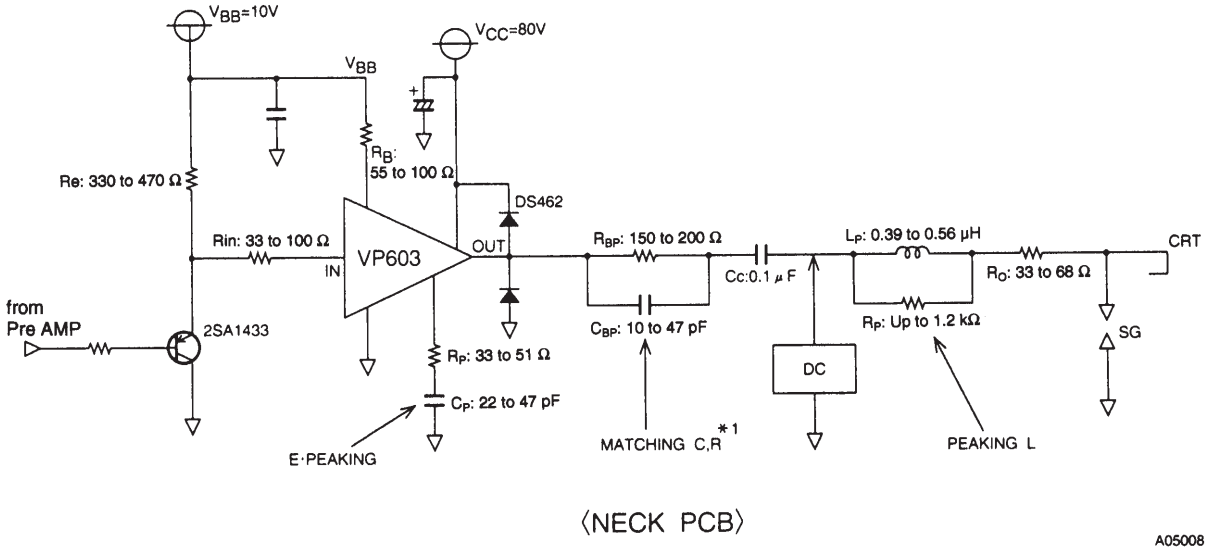






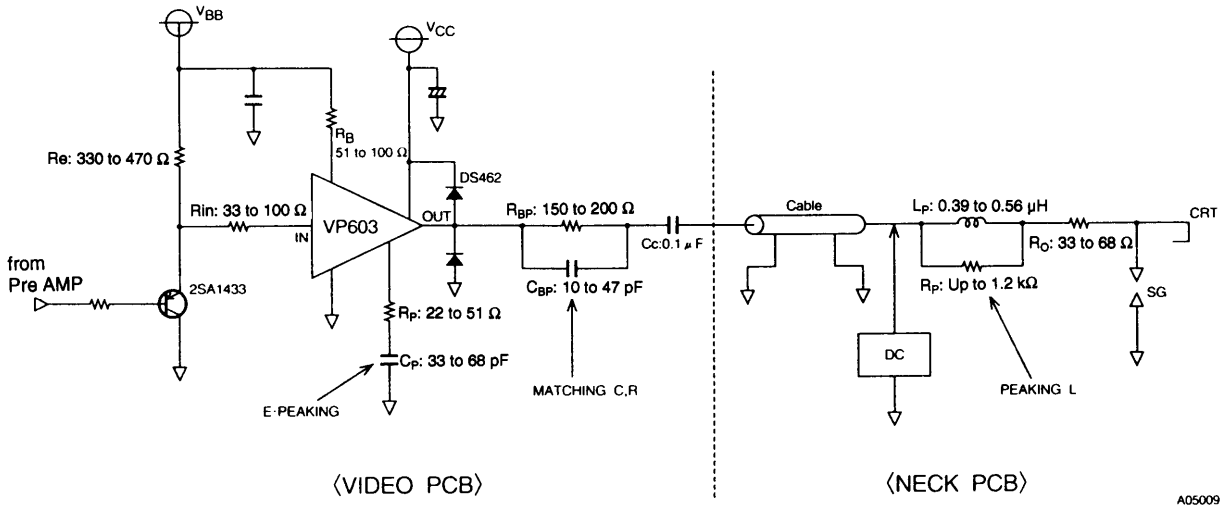
Sample Application Circuit

1. Mounting in the CRT neck



Note: * This RC matching circuit is provided to match the IC internal impedance with the output load impedance. When the IC is mounted in the CRT neck, this circuit can be removed if the total C_L (load capacitance) is under 10 pF.

2. Cable transmission (separate boards)



Mounting location for the C, G matching circuit
Add the RC matching circuit at a position as close as possible to the VP603 output pin.

Thermal Design for the VP603

Since the VP603 is a three-channel device, we first consider a single channel. The chip temperature of each transistor during actual operation is determined using the following formula.

$$Tj = (Tri) = \theta j\text{-}c\ (Tri) \times Pc\ (Tri) + \Delta Tc + Ta\ [°C] \quad \ldots\ldots (1)$$

$\theta j\text{-}c$ (Tri): Thermal resistance of an individual transistor
Pc (Tri): Collector loss for an individual transistor
ΔTc: Case temperature rise
Ta: Ambient temperature

The θj-c(Tri) for each chip is:

θj-c (Tr1) = 45°C/W/θj-c (Tr2) to (Tr4) = 35°C/W..... (2)

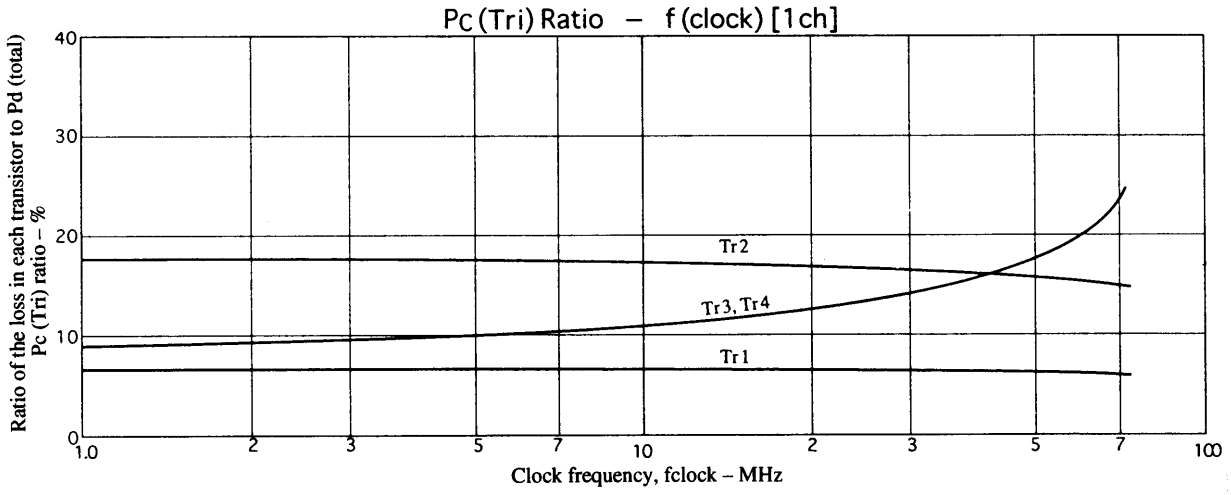
Although the loss for each transistor in a Video Pack varies with frequency and is not uniform, if we assume that the maximum operating frequency, f = 70 MHz (clock), then the chips with the largest loss will be transistors 3 and 4 and that loss will be about 1/4 of the total loss.Thus from the Pd for a single channel we have:

Pc (Tr3) f = 70 MHz = Pd (1CH) f = 70 MHz × 0.25 [W] ..... (3)

Here, we must select a heat sink with a capacity θh such that the Tj of these transistors does not exceed 150°C. Equation (4) below gives the relationship between θh and ΔTc.

ΔTc = Pd (TOTAL) × θh ..... (4)

The required θh is calculated using this equation and equation (1).



VP603 Thermal Design Example

Conditions: Using an f_H = 70 kHz class monitor, f_V = 100 MHz (clock)

V_{CC} = 80 V, V_{BB} = 10 V, V_{OUT} = 50 Vp-p (C_L = 10 pF)

Since this class of monitor can be operated up to Ta = 60°C, here we consider the case where the maximum clock frequency is 100 MHz.
As mentioned previously, the chip with the largest loss is transistor Tr3/Tr4. Determining the value gives:

Pc (Tr3) = 4.3 × 0.25 = 1.1 [W] ..... (5)

We determine ΔTj by substituting the value for θj-c in equation (5).

ΔTj = 1.1 × 35 = 38.5 [°C] ..... (6)

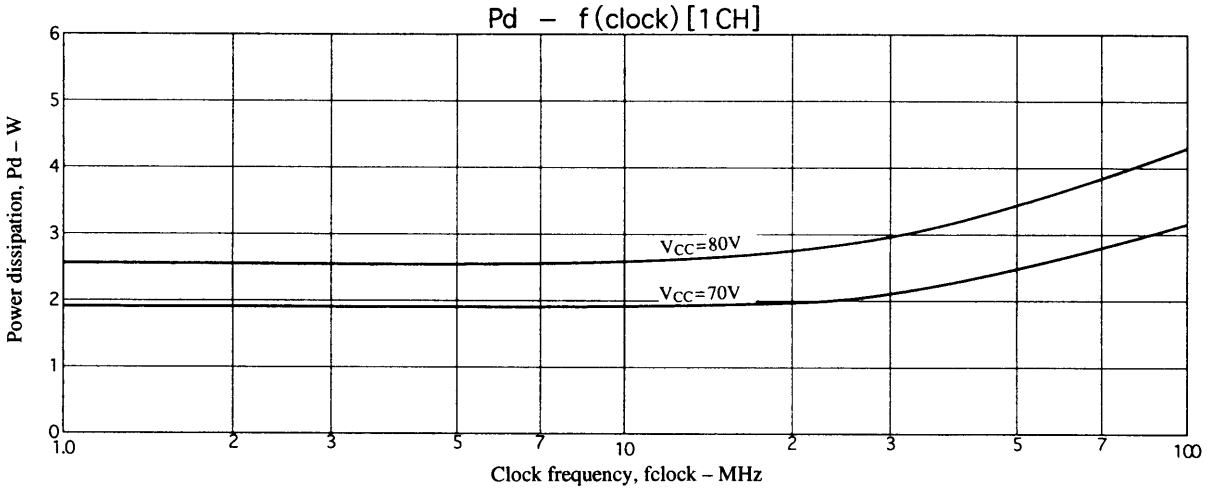
Here, Tc(max) (measured at the package surface) is taken to be under 100°C. This means that it suffices to design the heat sink taking Tc(max) < 100°C as the design target to fulfill the conditions that Tj(max) < 150°C and furthermore that Tc(max) < 100°C;

θh = ΔTc ÷ Pd (TOTAL) = (Tc – Ta) ÷ [Pd (1CH) × 3]
= 40 ÷ (4.3 × 3) = 3.1°C/W

Thus the thermal resistance in this case is

$\theta h = 3.1°C/W$.

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions into account is also required.



Surge Protection

Surge protection is required when this device is connected to a CRT. This product requires the same protection as earlier products.

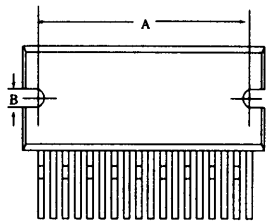
1. Termination spark gap
2. Surge suppression resistor (Recommended value: 33 to 68 Ω)
3. Surge suppression diode (Installed in the vicinity of the IC output pin.)

Note: The value of surge suppression resistors must be determined taking both the stipulated discharge test and the required frequency bandwidth into account.

Application Notes

Mounting notes:
Since the specified heat sink is required to operate a mounted Video Pack, we recommend the following mounting technique. (See the thermal design item for details on the required heat sink.) In particular, since the package used for this product is even more compact than that used in the earlier VPS series, the following points require special care. (These are recommendations.)

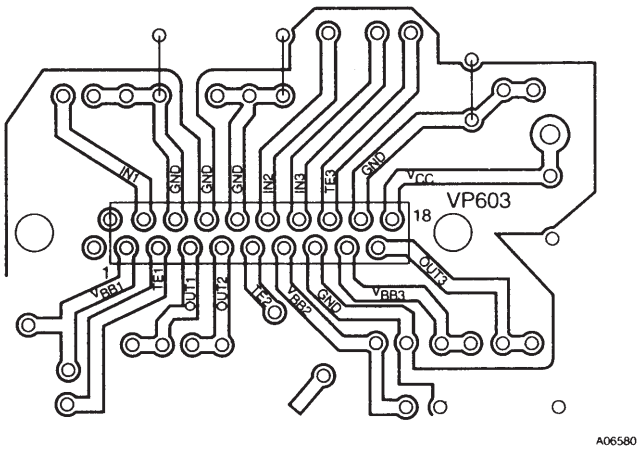
1. A tightening torque of between 0.39 and 0.88 N-m is recommended.
2. The bolt hole spacing in the heat sink should match that of the IC. In particular, the bolt hole spacing should be pulled in to be as close as possible, within the range that mounting is possible, to the dimensions A and B in the package dimensions drawing, as shown below.



3. Use either the truss screws (truss bolts) or binding screws stipulated in the JIS standards as the mounting bolts. Also, use washers to protect the IC case.
4. Foreign matter, such as machining chips, must not be left trapped between the IC case and the heat sink. If grease is applied to the junction surface, be sure to apply the grease evenly.
5. Solder the IC leads to the printed circuit board after mounting the heat sink to the IC.

Note: The heat sink is absolutely required to operate this Video Pack. Never, in any situation, apply power to a Video Pack as an independent device. The Video Pack may be destroyed.

Peripheral wiring and ground leading:
When shipped, the VP603 product lead pins have standard support for forming (zigzag) so that the distance between pins will be 2.54 mm. Also, the pin layout is standardized to the I/O and power supply line arrangement shown below.



IC Surrounding Pin Layout (Top view)

Note: Design applications that use two-sided printed circuit boards or similar technologies so that input and output lines do not cross. Crossed lines can lead to increased crosstalk. Also, lines should be kept as short as possible, and lines in the ground pattern should be made as wide as possible. These layout design principles will minimize bandwidth degradation and oscillation.