Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- No External Components
- 100:1 Clock to Center Ratio
- 150μV_{RMS} Total Wideband Noise
- 0.03% THD or Better
- 50kHz Maximum Corner Frequency
- Operates from ±2.37V to ±8V Power Supplies
- Passband Ripple Guaranteed Over Full Military Temperature Range

APPLICATIONS

- Antialiasing Filters
- Telecom PCM Filters

DESCRIPTION

The LTC1064-1 is an 8th order, clock sweepable elliptic (Cauer) lowpass switched capacitor filter. The passband ripple is typically ±0.15dB, and the stopband attenuation at 1.5 times the cutoff frequency is 68dB or more.

An external TTL or CMOS clock programs the value of the filter's cutoff frequency. The clock to cutoff frequency ratio is 100:1.

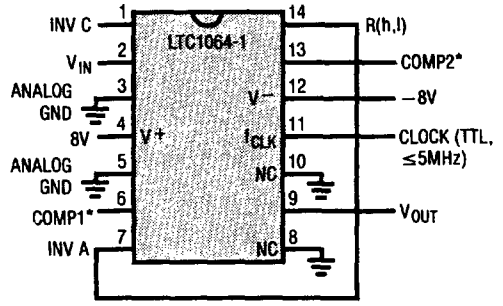
No external components are needed for cutoff frequencies up to 20kHz. For cutoff frequencies over 20kHz two low value capacitors are required to maintain passband flatness. The LTC1064-1 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-1 overall performance competes with equivalent multi op amp RC active realizations.

The LTC1064-1 is available in a 14-pin DIP or 16-pin surface mounted SOL package.

The LTC1064-1 is pin compatible with the LTC1064-2.

TYPICAL APPLICATION

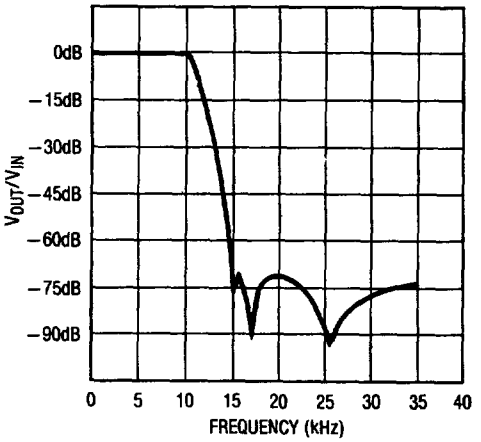
8th Order Clock Sweepable Lowpass Elliptic Antialiasing Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR CLOSE TO THE PACKAGE.

FOR SERVO OFFSET NULLING APPLICATIONS, PIN 1 IS THE 2ND STAGE SUMMING JUNCTION.
*FOR CUTOFF FREQUENCY ABOVE 20kHz, USE COMPENSATION CAPACITORS (5pF–56pF) BETWEEN PINS 13 AND 1 AND 6 AND 7.

Frequency Response

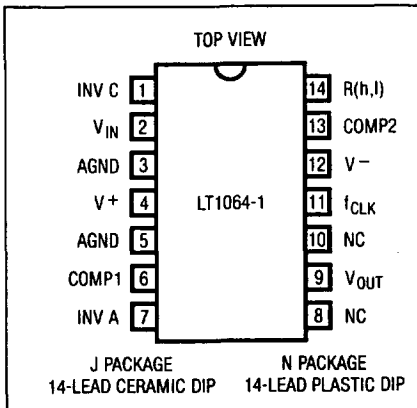


8TH ORDER CLOCK SWEEPABLE LOWPASS ELLIPTIC ANTIALIASING FILTER MAINTAINS, FOR $0.1Hz \le f_{CUTOFF} \le 10kHz$, a ±0.15dB PASSBAND RIPPLE AND 72dB STOPBAND ATTENUATION AT $1.50 \times f_{CUTOFF}$.
TOTAL WIDEBAND NOISE = $150\mu V_{RMS}$, THD = 0.03% FOR $V_{IN} = 1V_{RMS}$.

ABSOLUTE MAXIMUM RATINGS

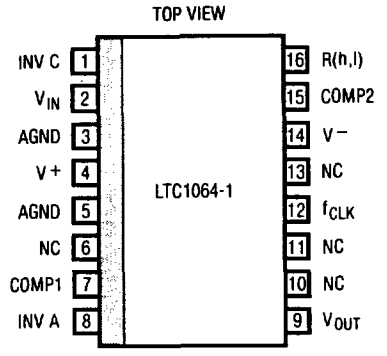
Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Operating Temperature Range
LTC1064-1M ..... –55°C to 125°C
LTC1064-1C ..... –40°C to 85°C

PACKAGE/ORDER INFORMATION



J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP



S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC1064-1MJ LTC1064-1CJ LTC1064-1CN
LTC1064-1CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$, $R_l = 10k\Omega$, $C_l = 10pF$, $T_A = 25°$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain, LTC1064-1, 1A	Referenced to 0dB, 1Hz to $0.1f_C$	●		±0.1	±0.35	dB
Gain TempCo				0.0002		dB/°C
Passband Edge Frequency, f_C				10 ± 1%		kHz
Gain at f_C	Referenced to Passband Gain					
LTC1064-1		●	–1.25		0.85	dB
LTC1064-1A		●	–0.75		0.65	dB
–3dB Frequency				10.7		kHz
Passband Ripple (Note 1)	$0.1f_C$ to $0.85f_C$ Referenced to Passband Gain,					
LTC1064-1	Measured at 6.25kHz and 8.5kHz	●		±0.15	±0.32	dB
LTC1064-1A		●		±0.1	±0.19	dB
Ripple TempCo				0.0004		dB/°C
Stopband Attenuation	At $1.5f_C$, Referenced to 0dB					
LTC1064-1		●	66	72		dB
LTC1064-1A		●	68	72		dB
Stopband Attenuation	At $2f_C$, Referenced to 0dB					
LTC1064-1		●	67	72		dB
LTC1064-1A		●	68	72		dB
Input Frequency Range			0		$f_{CLK}/2$	kHz
Output Voltage Swing and Operating Input Voltage Range	$V_S = \pm 2.37V$	●	–1.0		1	V
	$V_S = \pm 5V$	●	–3.2		3.2	V
	$V_S = \pm 7.5V$	●	–5.0		5.2	V

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$, $R_l = 10k\Omega$, $C_l = 10pF$, $T_A = 25°$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz			0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz			0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-999kHz			150		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-999kHz			165		μV_{RMS}
Output DC Offset	$V_S = \pm 7.5V$, Pin 2 Grounded					
LTC1064-1				50	175	mV
LTC1064-1A				50	125	mV
Output DC Offset TempCo	$V_S = \pm 5V$			−100		μV/°C
Input Impedance			10	20		kΩ
Output Impedance	$f_{OUT} = 10kHz$			2		Ω
Output Short Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 7.5V$				5	MHz
Power Supply Current	$V_S = \pm 2.37V$	●		10	16	mA
	$V_S = \pm 5V$			12	18	mA
		●			22	mA
	$V_S = \pm 8V$			16	22	mA
		●			28	mA
Power Supply Voltage Range		●	±2.37		±8	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For tighter specifications please contact LTC Marketing.

TYPICAL APPLICATIONS

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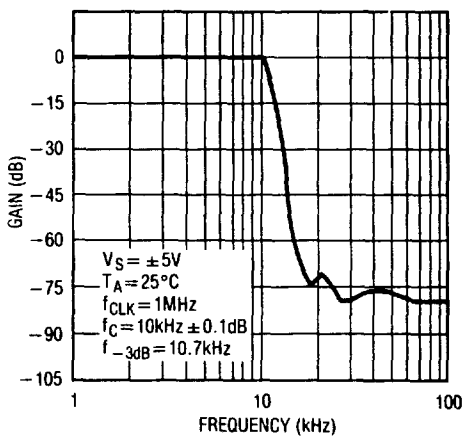
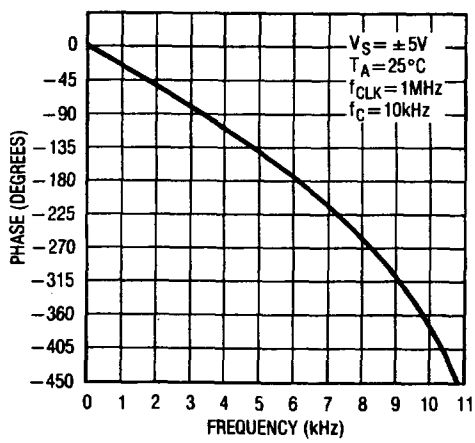
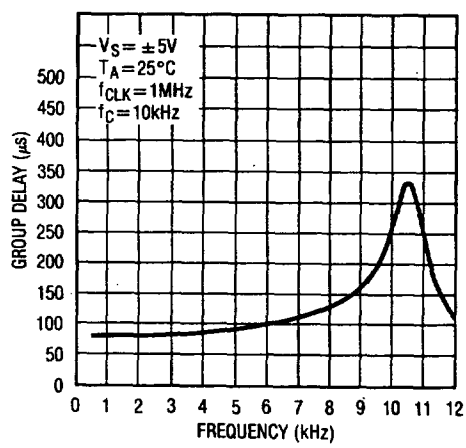
Graph 1. Gain vs Frequency



Graph 2. Phase vs Frequency

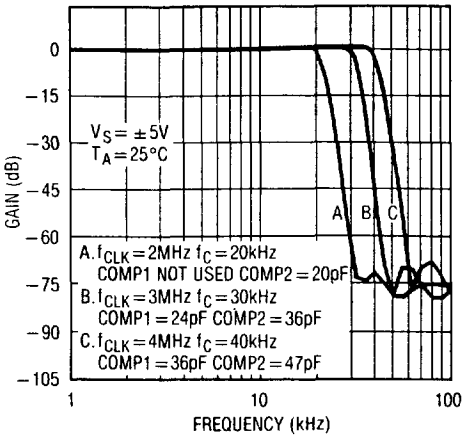


Graph 3. Group Delay

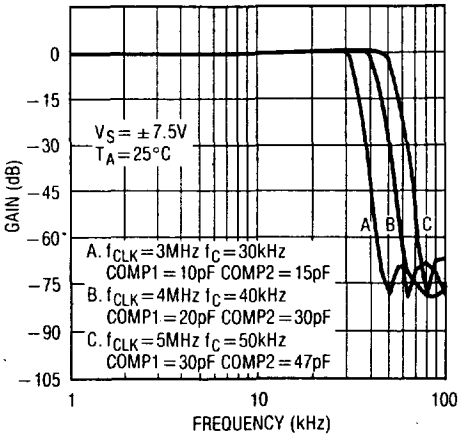


TYPICAL APPLICATIONS

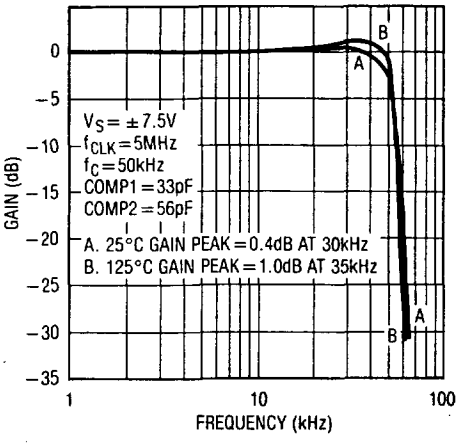
Graph 4. Gain vs Frequency



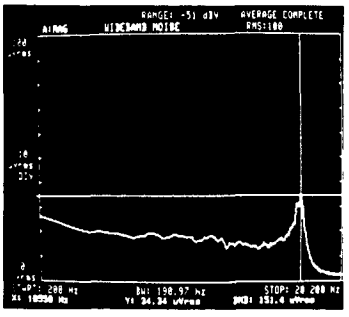
Graph 5. Gain vs Frequency



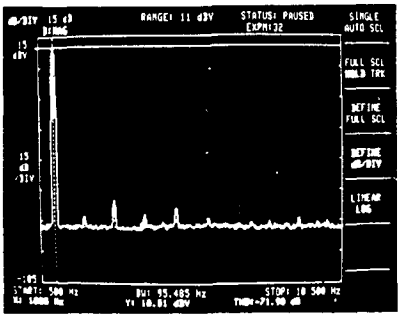
Graph 6. Gain vs Frequency



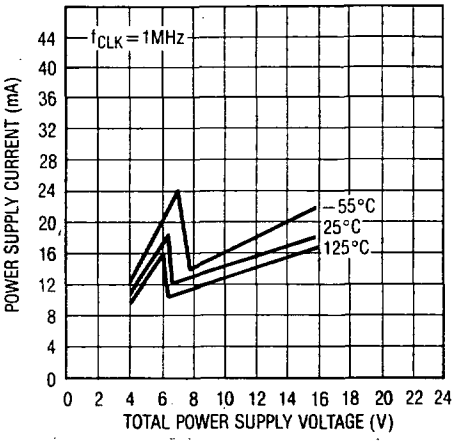
Graph 7. Typical Wideband Noise ($151\mu V_{RMS}$) $V_S = \pm 5V$ $T_A = 25°C$ $f_{CLK} = 1MHz$ $f_C = 10kHz$ Input Grounded



Graph 8. Total Harmonic Distortion (0.025%) $V_S = \pm 7.5V$ $T_A = 25°C$ $f_{CLK} = 1MHz$ $f_C = 10kHz$ Input = 1kHz at $3V_{RMS}$



Graph 9. Power Supply Current vs Power Supply Voltage



PIN DESCRIPTION

Power Supply Pins (4, 12)

The V^+ (pin 4) and V^- (pin 12) should be bypassed with a $0.1\mu F$ capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 schottky diode should be added from the V^+ and V^- pins to ground, Figure 1.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 5MHz. Do not allow the clock levels to exceed the power supplies. For clock level shifting, see Figure 3.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins

PIN DESCRIPTION

should be tied to one half supply, Figure 2. Also pins 8 and 10, although they are not internally connected should be tied to analog ground or system ground. This improves the clock feedthrough performance.

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

Compensation Pins (13 and 1, 6 and 7)

For filter cutoff frequencies higher than 20kHz, in order to minimize the passband ripple, compensation capacitors should be added between pins 6 and 7 (comp1) and pins 1 and 13 (comp2). For comp1 (comp2), add 1pF (1.5pF) mica capacitor for each kHz increase in cutoff frequency above 20kHz. For more details refer to graphs 4, 5, and 6.

Input, Output Pins (2, 9)

The input pin 2 is connected to an 18kΩ resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 4. **The op amp power supply wire (or trace) should be connected directly to the power source.**

NC Pins (8, 9)

The "no connection" pins preferably should be grounded.

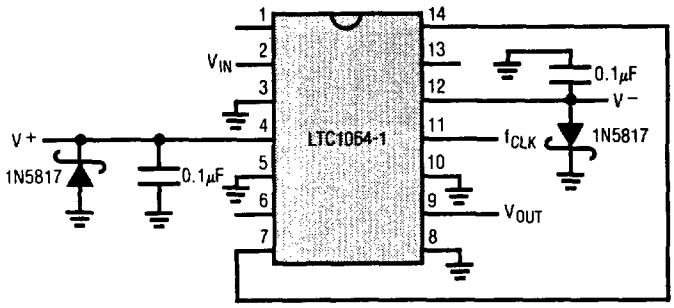


Figure 1. Using Schottky Diodes to Protect the IC from Power Supply Spikes.

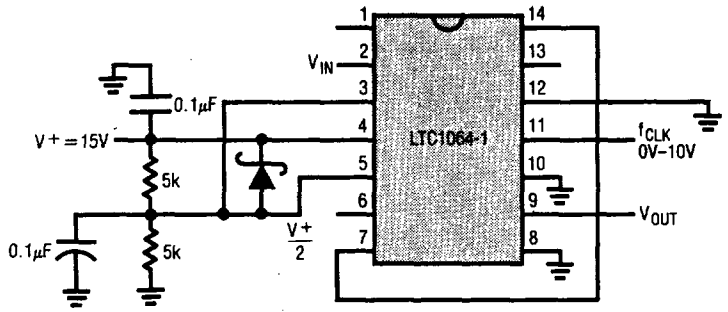


Figure 2. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5.

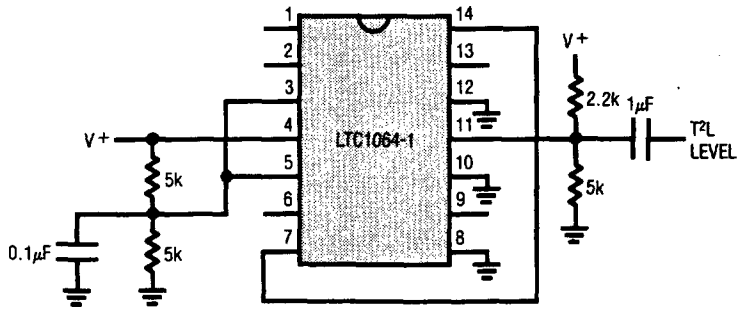


Figure 3. Level Shifting the Input T²L Clock for Single Supply Operation, V+ >6V

PIN DESCRIPTION

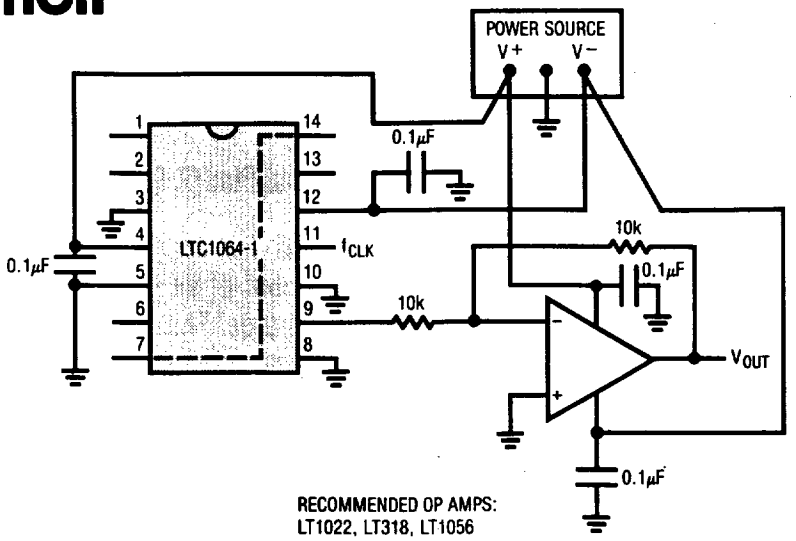
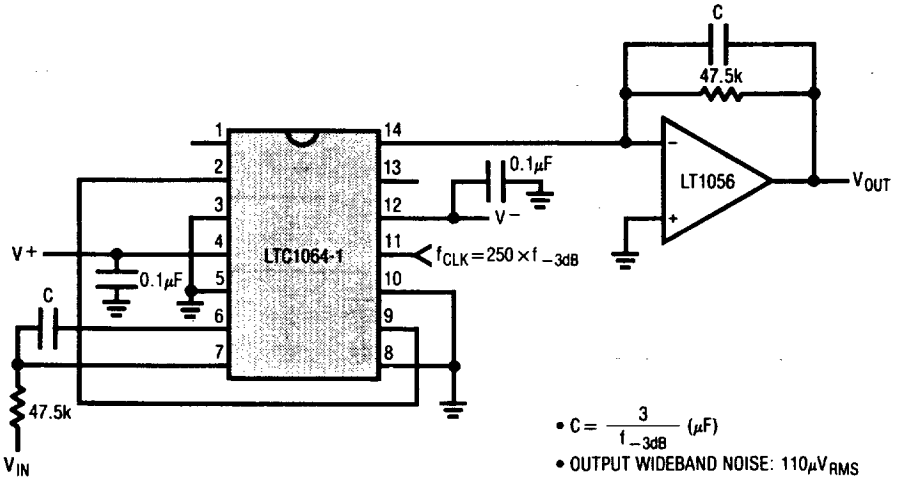


Figure 4. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-1 Power Lines.

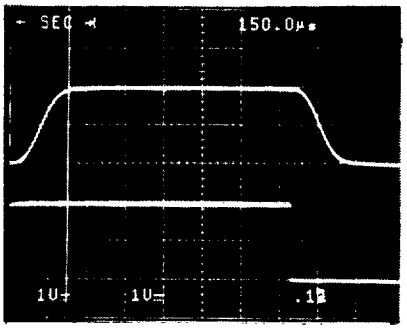
TYPICAL APPLICATIONS

Transitional Elliptic-Bessel 10th Order Lowpass Filter

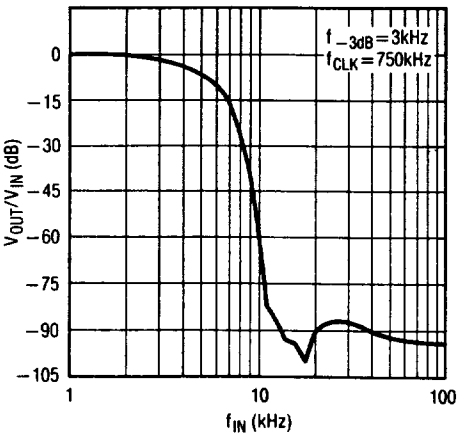


- $C = \frac{3}{f_{-3dB}}$ (μF)
- OUTPUT WIDEBAND NOISE: 110μV_{RMS}

Transient Response to a 2V Step Input
Horizontal: 0.1ms/Div
Vertical: 1V/Div

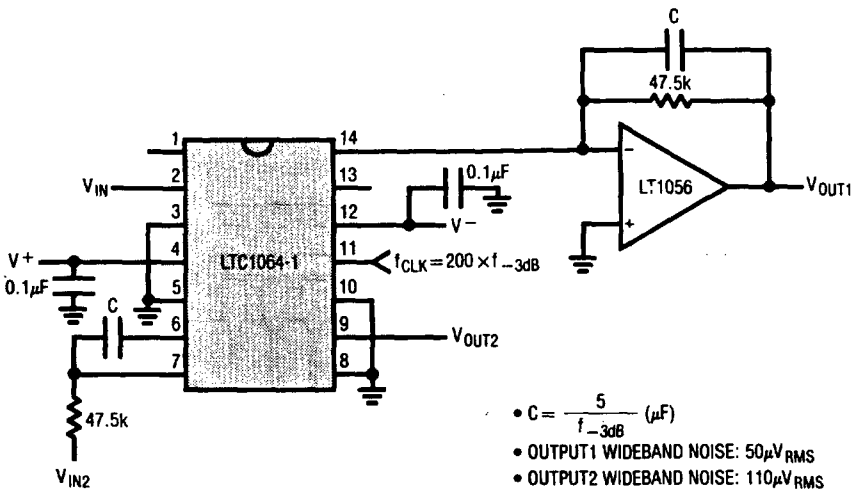


Amplitude Response



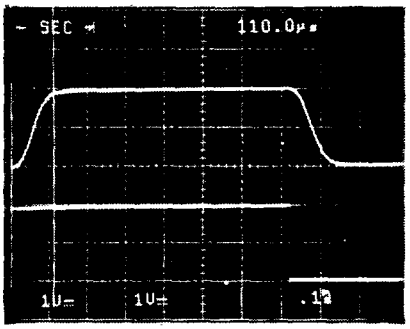
TYPICAL APPLICATIONS

Transitional Elliptic-Bessel Dual 5th Order Lowpass Filter

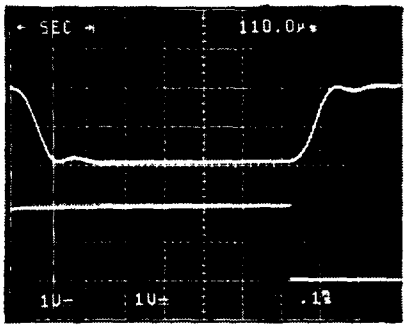


- $C = \frac{5}{f_{-3dB}}$ (μF)
- OUTPUT1 WIDEBAND NOISE: 50μV_{RMS}
- OUTPUT2 WIDEBAND NOISE: 110μV_{RMS}

Transient Reponse to a 2V Step Input
Horizontal: 0.1ms/Div
Vertical: 1V/Div

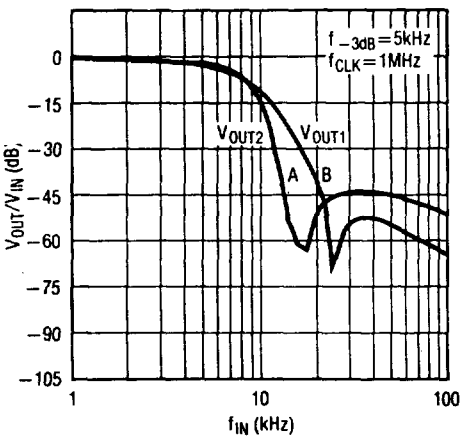


V_{OUT2}

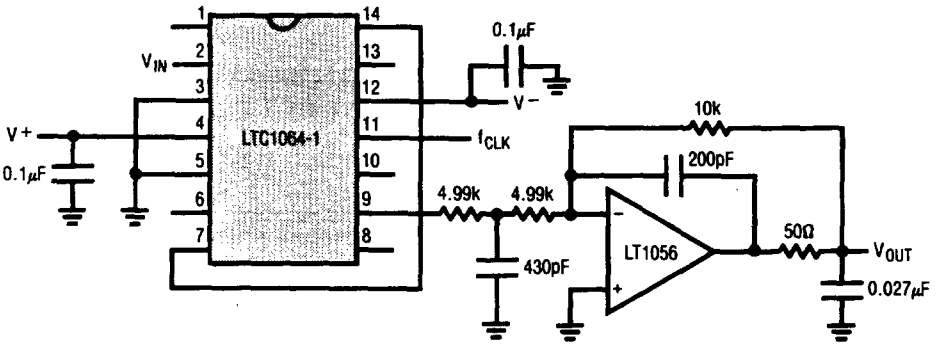


V_{OUT1}

Amplitude Response

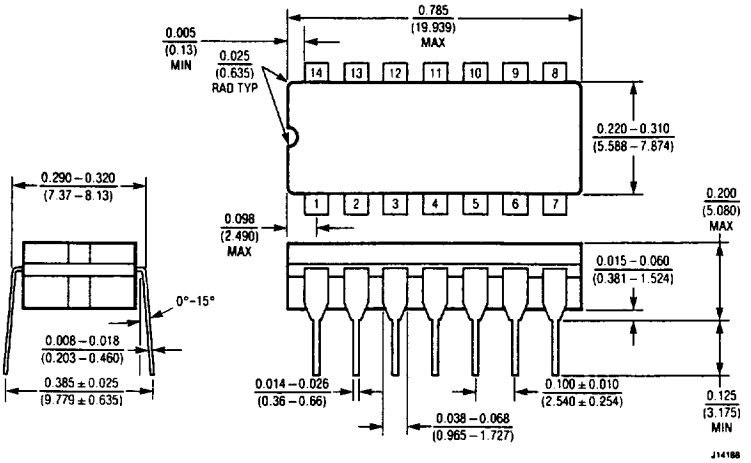


Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough Over a 10:1 Clock Range, for f_C = 2kHz to 20kHz

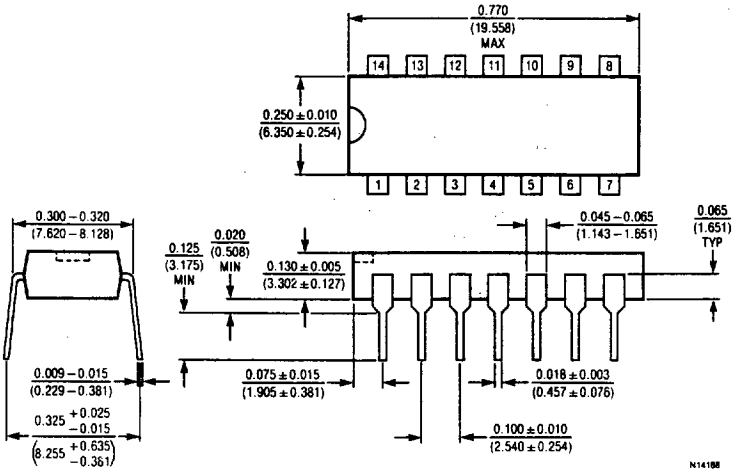


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOL

NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.