

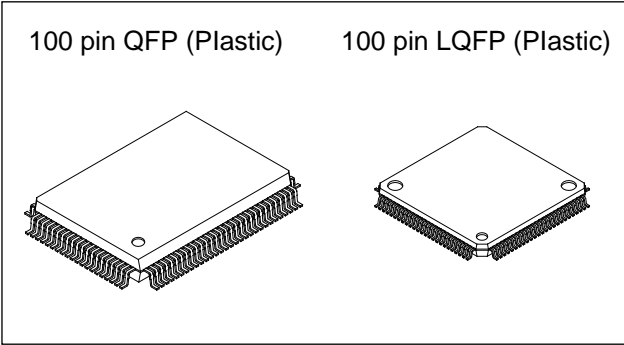
CXP87240A/87248A

CMOS 8-bit Single Chip Microcomputer

Description

The CXP87240A/87248A is a CMOS 8-bit micro-computer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, general purpose prescaler, HSYNC counter, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also CXP87240A/87248A provides sleep/stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.



Structure

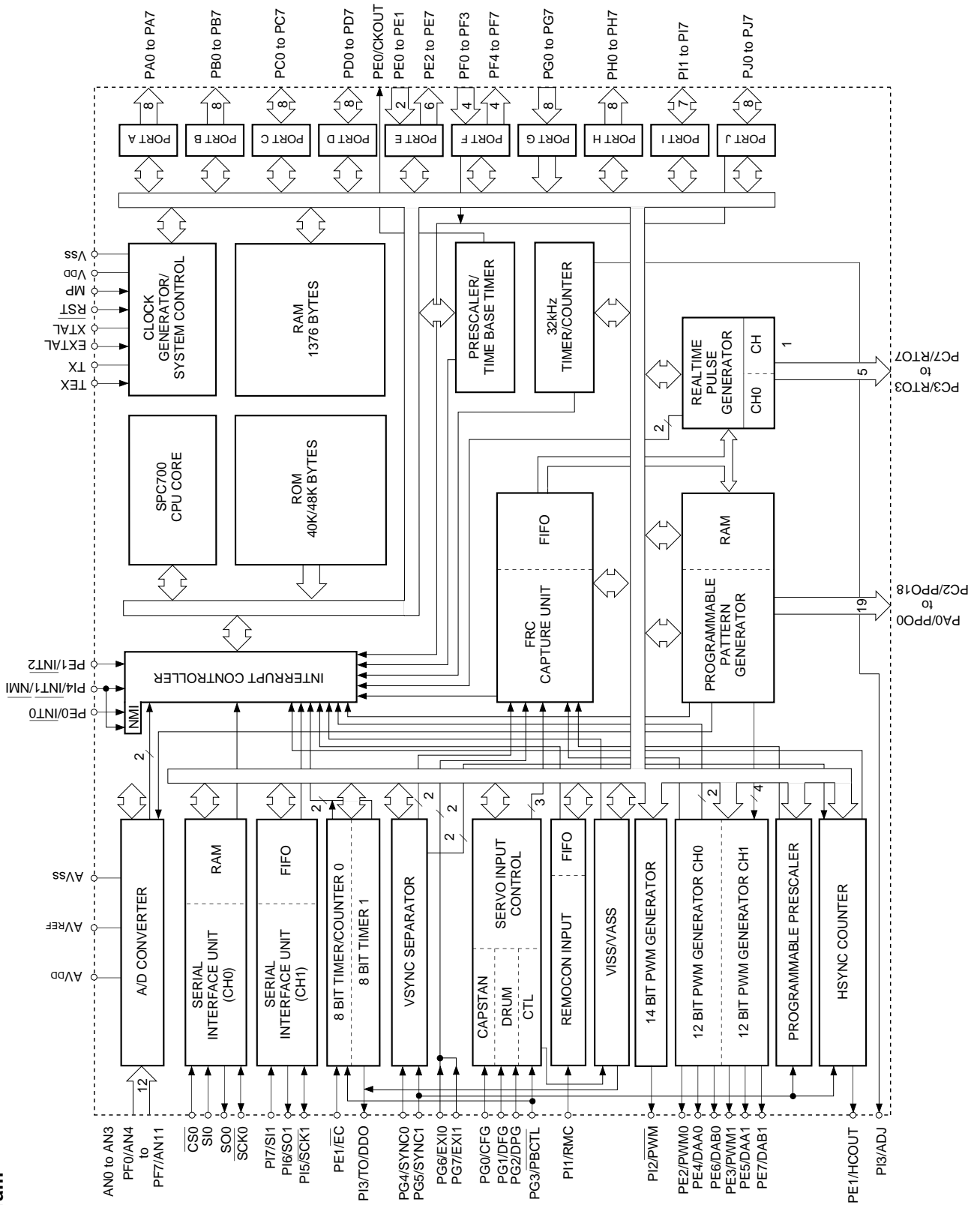
Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle
 - During operation 333ns/12MHz (3.0 to 5.5V)
 - During operation 250ns/16MHz (4.5 to 5.5V)
 - During operation 122µs/32kHz
- Incorporated ROM capacity 40Kbytes (CXP87240A), 48Kbytes (CXP87248A)
- Incorporated RAM capacity 1376bytes
- Peripheral functions
 - A/D converter 8-bit, 12-channel, successive approximation system (Conversion time 20.0µs/16MHz)
 - Serial interface Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel
Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer) 1-channel
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
 - High precision timing pattern generator PPG 19-pin 32-stage programmable
RTG 5-pin 2-channel
 - PWM/DA gate output PWM 12-bit, 2-channel (Repetitive frequency 62kHz/16MHz)
DA gate pulse output 13-bit, 4-channel
Capstan FG, Drum FG/PG, CTL input
 - Servo input control Incorporated 26-bit and 8-stage FIFO
 - VSYNC separator 14-bit, 1-channel
 - FRC capture unit Pulse duty auto detection circuit
 - PWM output 8-bit pulse measuring counter, 6-stage FIFO
 - VISS/VASS circuit 7-bit (SYNC1 input frequency divided, FRC capture possible)
 - Remote control receiving circuit 12-bit event counter (counts the SYNC1 input.)
 - General purpose prescaler 22 factors, 15 vectors, multi-interruption possible
 - HSYNC counter SLEEP/STOP
- Interruption 100-pin plastic QFP/LQFP
- Standby mode CXP87200A 100-pin ceramic QFP/LQFP
- Package
- Piggyback/evaluation chip

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Description

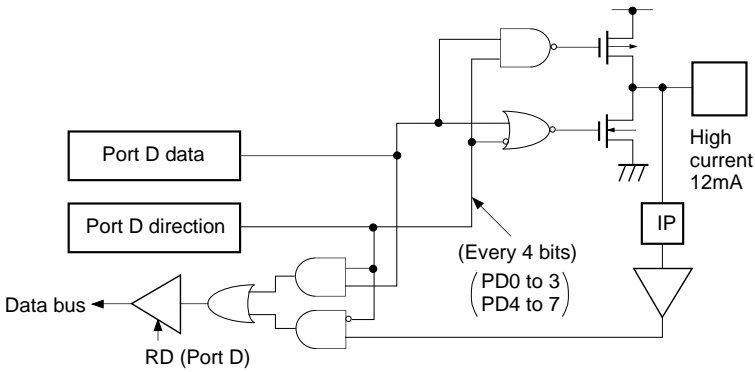
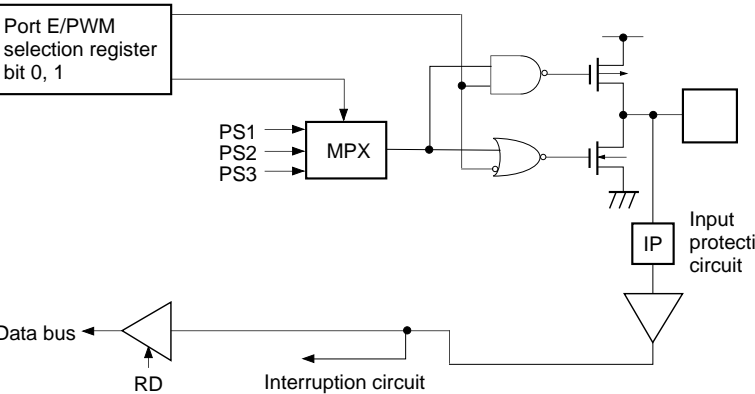
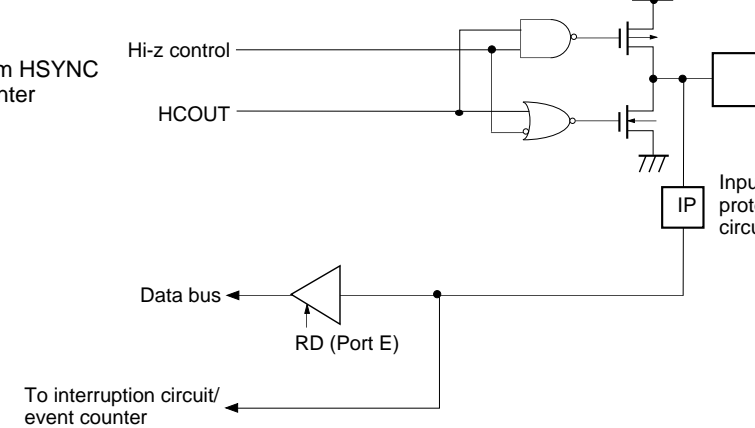
Symbol	I/O	Description			
PA0/PPO0 to PA7/PPO7	Output/Real time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins) PB0 and PB2 can be 3-state controlled with PPG.		
PB0/PPO8 to PB7/PPO15	Output/Real time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)			
PC0/PPO16 to PC2/PPO18	I/O/Real time output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)			
PC3/RTO3 to PC7/RTO7	I/O/Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)		
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)			
PE0/ $\overline{\text{INT0}}$ /CKOUT	Input/Input/Output	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.		
			PC3 can be 3-state controlled with RTG. System clock frequency division output.		
PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$ /HCOUT	Input/Input/Input/Output		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.	Coincidence signal output pin for HSYNC counter.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)		
PE3/PWM1	Output/Output				
PE4/DAA0	Output/Output				
PE5/DAA1	Output/Output		DA gate pulse output pins. (4 pins)		
PE6/DAB0	Output/Output				
PE7/DAB1	Output/Output				
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)			
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)			
PF4/AN8 to PF7/AN11	Output/Input				
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.			
SO0	Output	Serial data (CH0) output pin.			
SI0	Input	Serial data (CH0) input pin.			
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.			

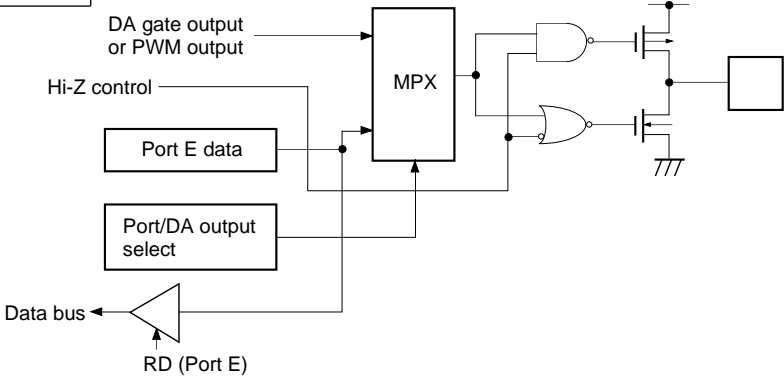
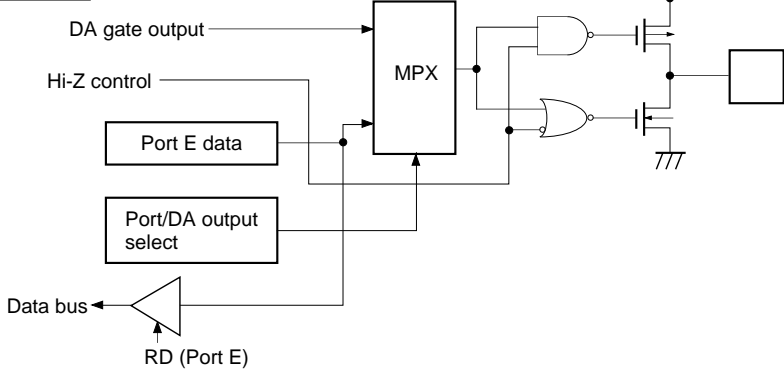
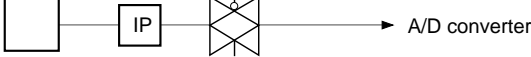
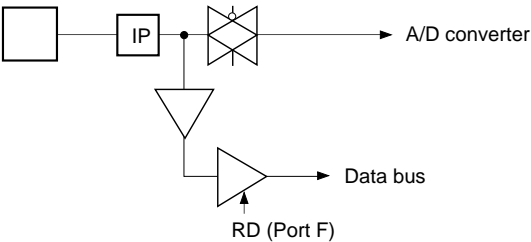
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/Input		Drum FG input pin.
PG2/DPG	Input/Input		Drum PG input pin.
PG3/ $\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input pin. External event input pin of timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input pin.
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input pin to FRC capture unit.
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/ $\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active when falling edge.
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.	
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV _{DD}		Positive power supply pin of A/D converter.	
AV _{REF}	Input	Reference voltage input pin of A/D converter.	
AV _{SS}		GND pin of A/D converter.	
V _{DD}		Positive power supply pin.	
V _{SS}		GND pin. Connect both V _{SS} pins to GND.	

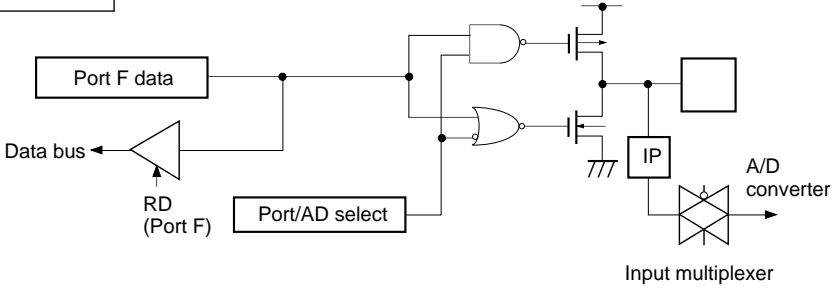
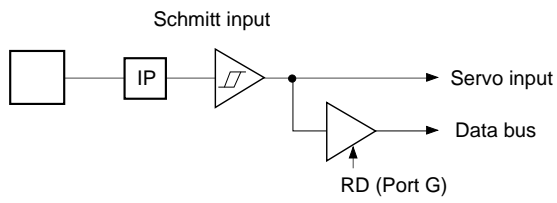
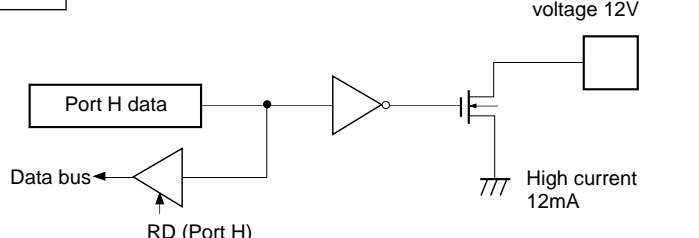
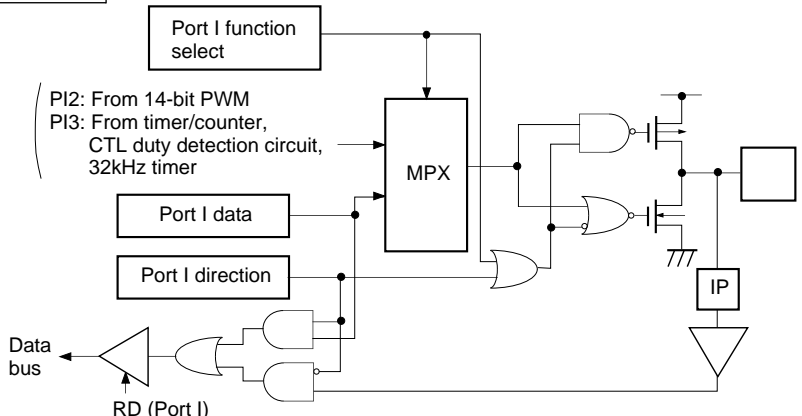
Input/Output Circuit Formats for Pins

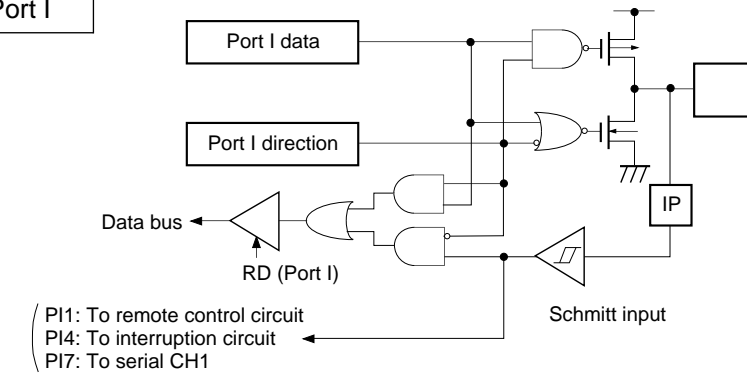
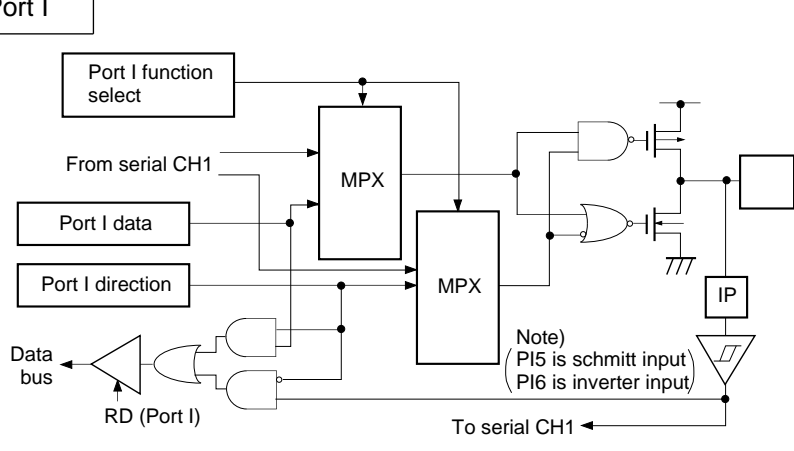
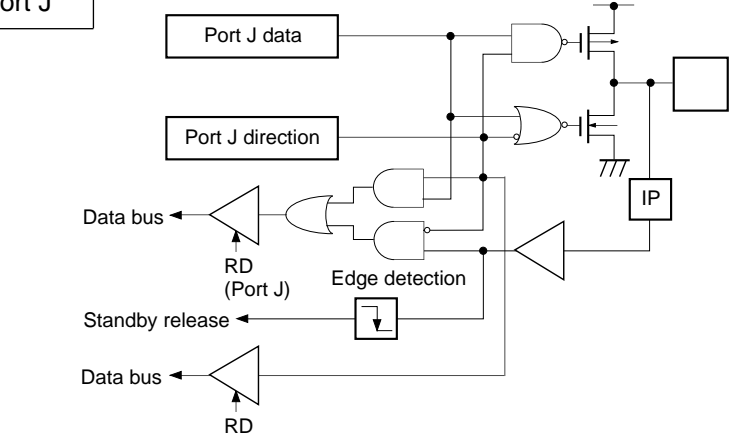
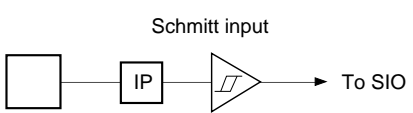
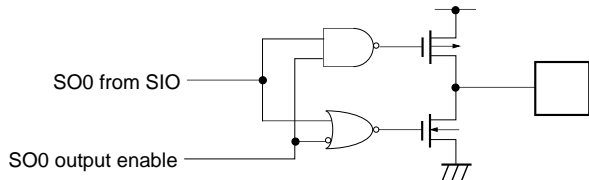
Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0 /PPO0 to PA7/PPO7</p> <p>PB4/PPO12 to PB7/PPO15</p> <p>12 pins</p>	<p>PPO data</p> <p>Port A or Port B</p> <p>Data bus ← RD</p> <p>Output becomes active from Hi-Z by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB0 /PPO8 PB2/PPO10</p> <p>2 pins</p>	<p>PPO8 or PPO10</p> <p>PB0 or PB2 data</p> <p>RD</p> <p>Data bus ←</p> <p>Output becomes active from Hi-Z by data writing to port register.</p>	<p>Hi-Z</p>
<p>PB1/PPO9 PB3/PPO11</p> <p>2 pins</p>	<p>PPG control status register bit 0 3-state control selection</p> <p>PPO9 or PPO11</p> <p>PB1 or PB3 data</p> <p>Data bus ← RD</p> <p>Output becomes active from Hi-Z by data writing to port register.</p>	<p>Hi-Z</p>

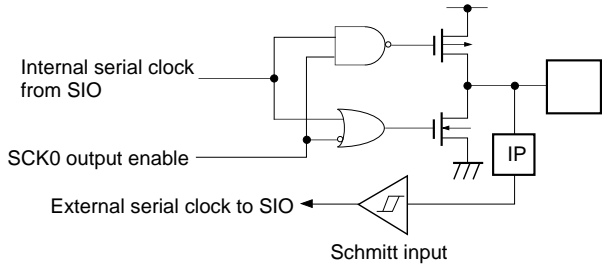
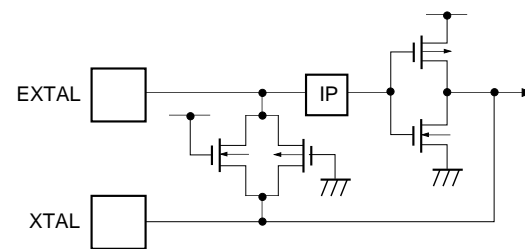
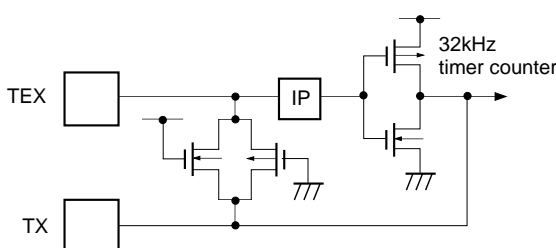
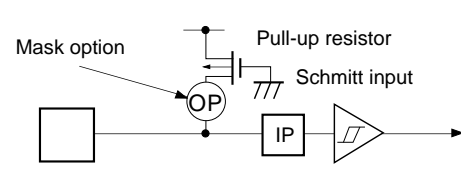
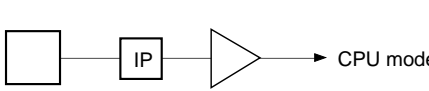
Pin	Circuit format	When reset
<p>PC0/PPO16 to PC2/PPO18</p> <p>PC5/RTO5 to PC7/RTO7</p> <p>6 pins</p>	<p>Port C</p>	<p>Hi-Z</p>
<p>PC3/RTO3</p> <p>1 pins</p>		<p>Hi-Z</p>
<p>PC4/RTO4</p> <p>1 pins</p>		<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PD0 to PD7</p> <p>8 pins</p>	<p>Port D</p> 	<p>Hi-Z</p>
<p>PE0/$\overline{\text{INT0}}$/ CKOUT</p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$/ HCOUT</p> <p>1 pin</p>	<p>Port E</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p> 	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p> 	<p>H level</p>
<p>AN0 to AN3</p> <p>4 pins</p>	<p>Input multiplexer</p> 	<p>Hi-Z</p>
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p> <p>Input multiplexer</p> 	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>The diagram shows the internal circuit for Port F. It includes a 'Port F data' register connected to a 'Data bus'. A read signal 'RD (Port F)' is used to enable a multiplexer that selects between the 'Port F data' and an 'Input multiplexer'. The 'Input multiplexer' is controlled by 'Port/AD select' and provides input to an 'A/D converter'. The circuit also features two NPN transistors connected to the data bus and ground, controlled by AND gates that receive signals from the 'Port F data' register and 'RD (Port F)'. An internal pull-up resistor is connected to the input multiplexer output.</p>	<p>Hi-Z</p>
<p>PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1</p> <p>8 pins</p>	<p>Port G</p>  <p>Note) For PG4/SYNC0, PG5/SYNC1, CMOS schmitt input and TTL schmitt input can be selected with the mask option.</p> <p>The diagram shows the internal circuit for Port G. It features a 'Schmitt input' block followed by an 'IP' (input pull-up) resistor. The output of the Schmitt input is connected to a 'Servo input' and a 'Data bus'. A read signal 'RD (Port G)' is used to enable a multiplexer that selects between the 'Schmitt input' and the 'Data bus'. The circuit also includes two NPN transistors connected to the data bus and ground, controlled by AND gates that receive signals from the 'Schmitt input' and 'RD (Port G)'.</p>	<p>Hi-Z</p>
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Medium withstand voltage 12V</p> <p>High current 12mA</p> <p>The diagram shows the internal circuit for Port H. It includes a 'Port H data' register connected to a 'Data bus'. A read signal 'RD (Port H)' is used to enable a multiplexer that selects between the 'Port H data' and a 'High current 12mA' output. The 'High current 12mA' output is connected to a 'Medium withstand voltage 12V' source. The circuit also features two NPN transistors connected to the data bus and ground, controlled by AND gates that receive signals from the 'Port H data' register and 'RD (Port H)'.</p>	<p>Hi-Z</p>
<p>PI2/PWM PI3/TO/ DDO/ADJ</p> <p>2 pins</p>	<p>Port I</p>  <p>PI2: From 14-bit PWM PI3: From timer/counter, CTL duty detection circuit, 32kHz timer</p> <p>The diagram shows the internal circuit for Port I. It includes a 'Port I function select' register connected to a multiplexer ('MPX'). The 'MPX' also receives inputs from 'Port I data' and 'Port I direction' registers. The output of the 'MPX' is connected to a 'Data bus'. A read signal 'RD (Port I)' is used to enable a multiplexer that selects between the 'MPX' output and the 'Data bus'. The circuit also features two NPN transistors connected to the data bus and ground, controlled by AND gates that receive signals from the 'MPX' output and 'RD (Port I)'. An internal pull-up resistor is connected to the 'MPX' output.</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PI1/RMC PI4/INT1/NMI PI7/S11</p> <p>3 pins</p>	<p>Port I</p>  <p>Data bus ← RD (Port I)</p> <p>Schmitt input</p> <p>(PI1: To remote control circuit PI4: To interruption circuit PI7: To serial CH1</p>	<p>Hi-Z</p>
<p>PI5/SCK1 PI6/SO1</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus ← RD (Port I)</p> <p>Note) PI5 is schmitt input PI6 is inverter input</p> <p>To serial CH1</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p>  <p>Port J data</p> <p>Port J direction</p> <p>Data bus ← RD (Port J)</p> <p>Edge detection</p> <p>Standby release</p> <p>Data bus ← RD</p>	<p>Hi-Z</p>
<p>CS0 SIO</p> <p>2 pins</p>	<p>Schmitt input</p>  <p>To SIO</p>	<p>Hi-Z</p>
<p>SO0</p> <p>1 pin</p>	 <p>SO0 from SIO</p> <p>SO0 output enable</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>$\overline{\text{SCK0}}$</p> <p>1 pin</p>	 <p>Internal serial clock from SIO</p> <p>SCK0 output enable</p> <p>External serial clock to SIO</p> <p>Schmitt input</p>	<p>Hi-Z</p>
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. 	<p>Oscillation</p>
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>	 <p>Mask option</p> <p>Pull-up resistor</p> <p>Schmitt input</p>	<p>L level</p>
<p>MP</p> <p>1 pin</p>	 <p>CPU mode</p>	<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS}=0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium withstand output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than high current output pins: per pin
	I _{OLC}	20	mA	High current port pin* ³ : per pin
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*¹ AV_{DD} and V_{DD} should be set to a same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ The high current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5		Guaranteed range during low speed mode. (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
			5.5	V	CMOS schmitt input*7
	V _{IHTS}	2.2	5.5	V	TTL schmitt input*4
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5, *8 TEX pin*6, *8
V _{DD} + 0.2			V	EXTAL pin*5, *9 TEX pin*6, *9	
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *8
			0.2V _{DD}	V	*2, *9
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
	V _{ILTS}	0	0.8	V	TTL schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5, *8 TEX pin*6, *8
0.2			V	EXTAL pin*5, *9 TEX pin*6, *9	
Operating temperature	T _{opr}	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$, PI1/ $\overline{\text{RMC}}$, PI4/ $\overline{\text{INT1}}$ / $\overline{\text{NMI}}$, PI5/ $\overline{\text{SCK1}}$ and PI7/SI1.

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 It specifies only when the external clock is input.

*6 It specifies only when the external event count clock is input.

*7 Each pin of $\overline{\text{CS0}}$, SI0, and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option.)

*8 When the range of supply voltage (V_{DD}) is within 4.5 to 5.5V.

*9 When the range of supply voltage (V_{DD}) is within 3.0 to 3.6V.

Electrical Characteristics

DC Characteristics

Supply Voltage (V_{DD}) 4.5 to 5.5V

(T_a = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V _{OL} only) PI1 to PI7	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output voltage	V _{OL}	PJ, SO0, SCK0	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PD, PH	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{ILE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
	I _{ILT}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.1		-10	μA
	I _{ILR}		RST*1	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400
I/O leakage current	I _{IZ}	PA to PG, PI, PJ, MP AN0 to AN3, CS0, SI0, SO0 SCK0, RST*1	V _{DD} =5.5V, V _I =0, 5.5V			±10	μA
Open drain output leakage current (N-CH Tr OFF in state)	I _{LOH}	PH	V _{DD} = 5.5V V _{OH} = 12V			50	μA
Supply current*2	I _{DD1}	V _{DD}	16MHz crystal oscillation (C ₁ = C ₂ = 15pF)		28	45	mA
			V _{DD} = 5V ± 0.5V*3				
	I _{DDS1}		SLEEP mode		1.7	8	mA
			V _{DD} = 5V ± 0.5V				
	I _{DD2}		32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		40	100	μA
V _{DD} = 3V ± 0.3V							
I _{DDS2}	SLEEP mode		10	30	μA		
	V _{DD} = 3V ± 0.3V						
I _{DDS3}	STOP mode (EXTAL and TEX pins oscillation stop)			10	μA		
	V _{DD} = 5V ± 0.5V						
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

Supply Voltage (V_{DD}) 3.0 to 3.6V

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7,	$V_{DD} = 3.0V, I_{OH} = -0.15mA$	2.7			V
			$V_{DD} = 3.0V, I_{OH} = -0.5mA$	2.3			V
Low level output voltage	V_{OL}	PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	$V_{DD} = 3.0V, I_{OL} = 1.2mA$			0.3	V
			$V_{DD} = 3.0V, I_{OL} = 1.6mA$			0.5	V
		PD, PH	$V_{DD} = 3.0V, I_{OL} = 5mA$			1.0	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 3.6V, V_{IH} = 3.6V$	0.3		20	μA
	I_{ILE}		$V_{DD} = 3.6V, V_{IL} = 0.3V$	-0.3		-20	μA
	I_{IHT}	TEX	$V_{DD} = 3.6V, V_{IH} = 3.6V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 3.6V,$ $V_{IL} = 0.3V$	-0.1		-10	μA
	I_{ILR}		\overline{RST}^{*1}	-0.9		-200	μA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, $\overline{CS0}$, SI0, SO0, $\overline{SCK0}$, \overline{RST}^{*1}	$V_{DD} = 3.6V,$ $V_I = 0, 3.6V$			± 10	μA
Open drain output leakage current	I_{LOH}	PH	$V_{DD} = 3.6V,$ $V_{OH} = 12V$			50	μA
Supply current*2	I_{DD1}	V_{DD}	12MHz crystal oscillation ($C_1 = C_2 = 15pF$) $V_{DD} = 3.3V \pm 0.3V^{*3}$		13	25	mA
	I_{DDS1}		SLEEP mode $V_{DD} = 3.3V \pm 0.3V$		0.8	2.5	mA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) $V_{DD} = 3.3V \pm 0.3V$			10	μA
Input capacity	C_{IN}	Other than V_{DD} , V_{SS} , AV_{DD} , and AV_{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 \overline{RST} pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	VDD = 4.5 to 5.5V	28		ns
					37.5		
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (external clock drive)		200	ns	
Event count clock input pulse width	tEH, tEL	\overline{EC}	Fig. 3		$t_{sys} \times 4^*$	ns	
Event count clock input rise and fall times	tER, tEF	\overline{EC}	Fig. 3		20	ms	
System clock frequency	fc	TEX TX	Fig. 2 VDD = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz	
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs	
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms	

* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

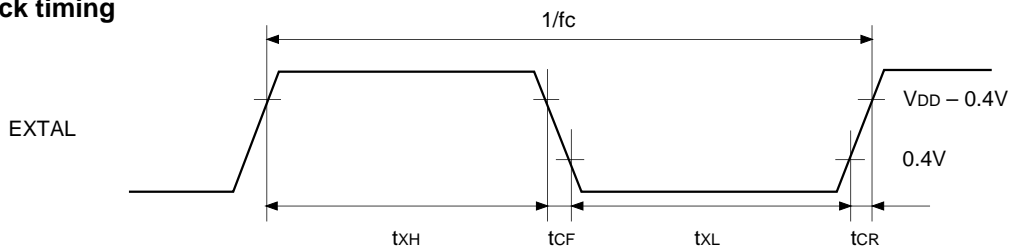


Fig. 2. Clock applied condition

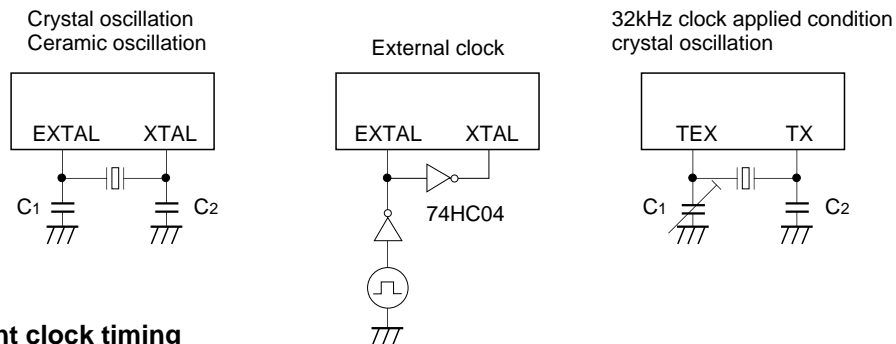
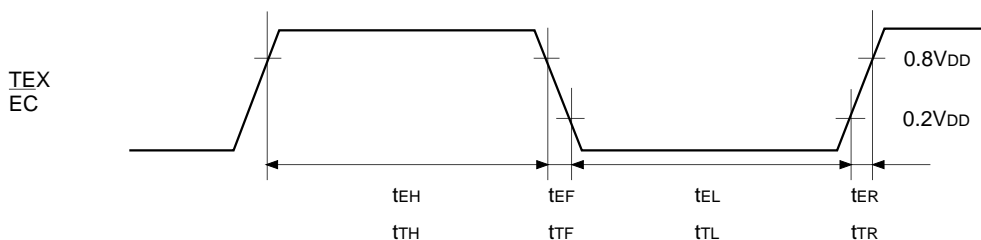


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
\overline{CS} high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
\overline{SCK} cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$8000/fc$		ns
\overline{SCK} high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/fc - 100$		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t_{SIK}	SI0	\overline{SCK} input mode	$-t_{sys} + 100$		ns
			\overline{SCK} output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t_{KSI}	SI0	\overline{SCK} input mode	$2t_{sys} + 100$		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	\overline{SCK} input mode		$2t_{sys} + 200$	ns
			\overline{SCK} output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI \rightarrow SI0, and SO \rightarrow SO0 respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF + 1TTL.

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		$t_{sys} + 250$	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		$t_{sys} + 200$	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{sys} + 250$	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{sys} + 200$	ns
\overline{CS} high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	$t_{sys} + 200$		ns
\overline{SCK} cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	$2t_{sys} + 200$		ns
			Output mode	$8000/fc$		ns
\overline{SCK} high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/fc - 150$		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t_{SIK}	SI0	\overline{SCK} input mode	$-t_{sys} + 100$		ns
			\overline{SCK} output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t_{KSI}	SI0	\overline{SCK} input mode	$2t_{sys} + 100$		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t_{KSO}	SO0	\overline{SCK} input mode		$2t_{sys} + 250$	ns
			\overline{SCK} output mode		125	ns

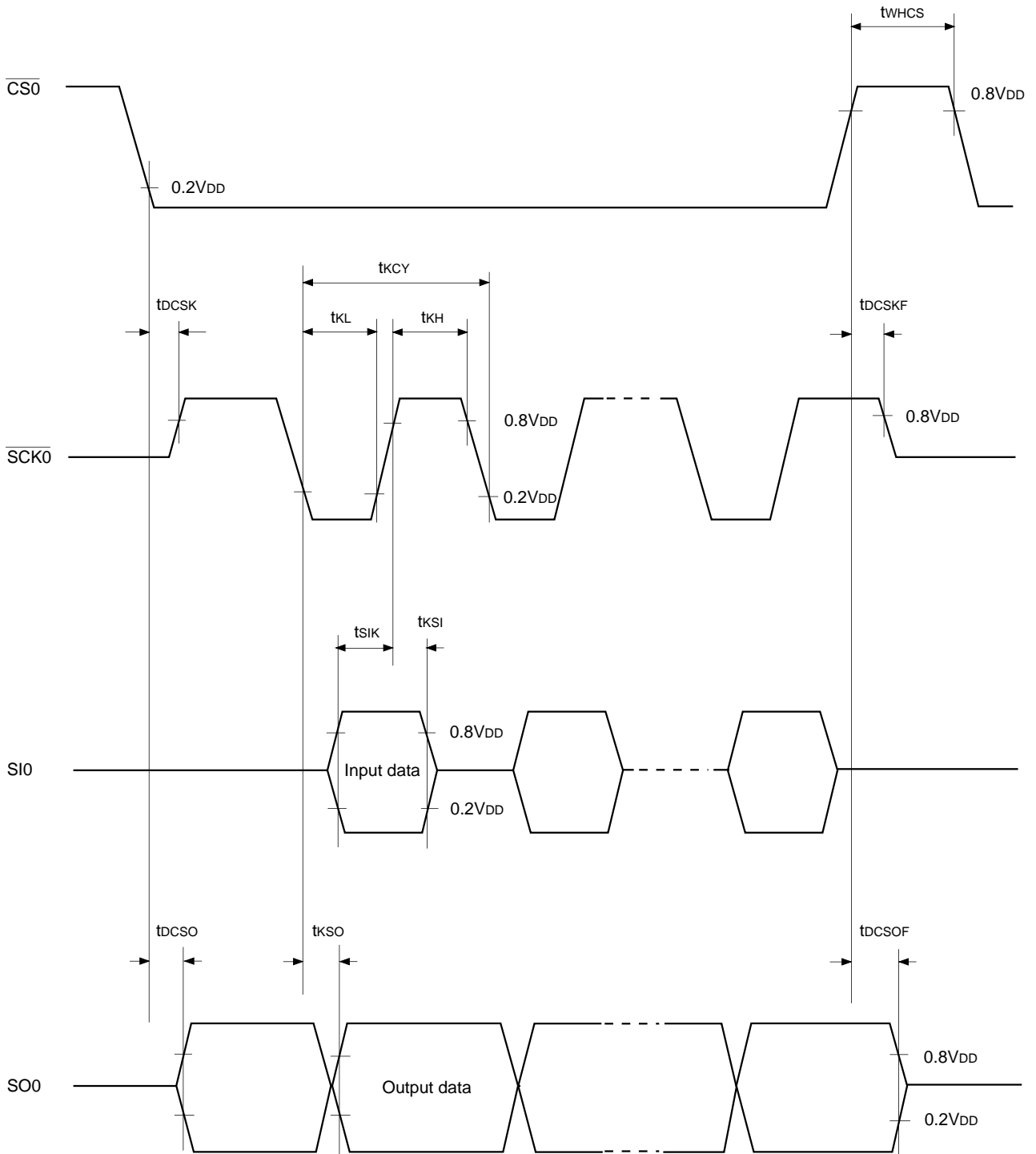
Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI \rightarrow SI0, and SO \rightarrow SO0 respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (SIO mode)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, Vss = 0V)

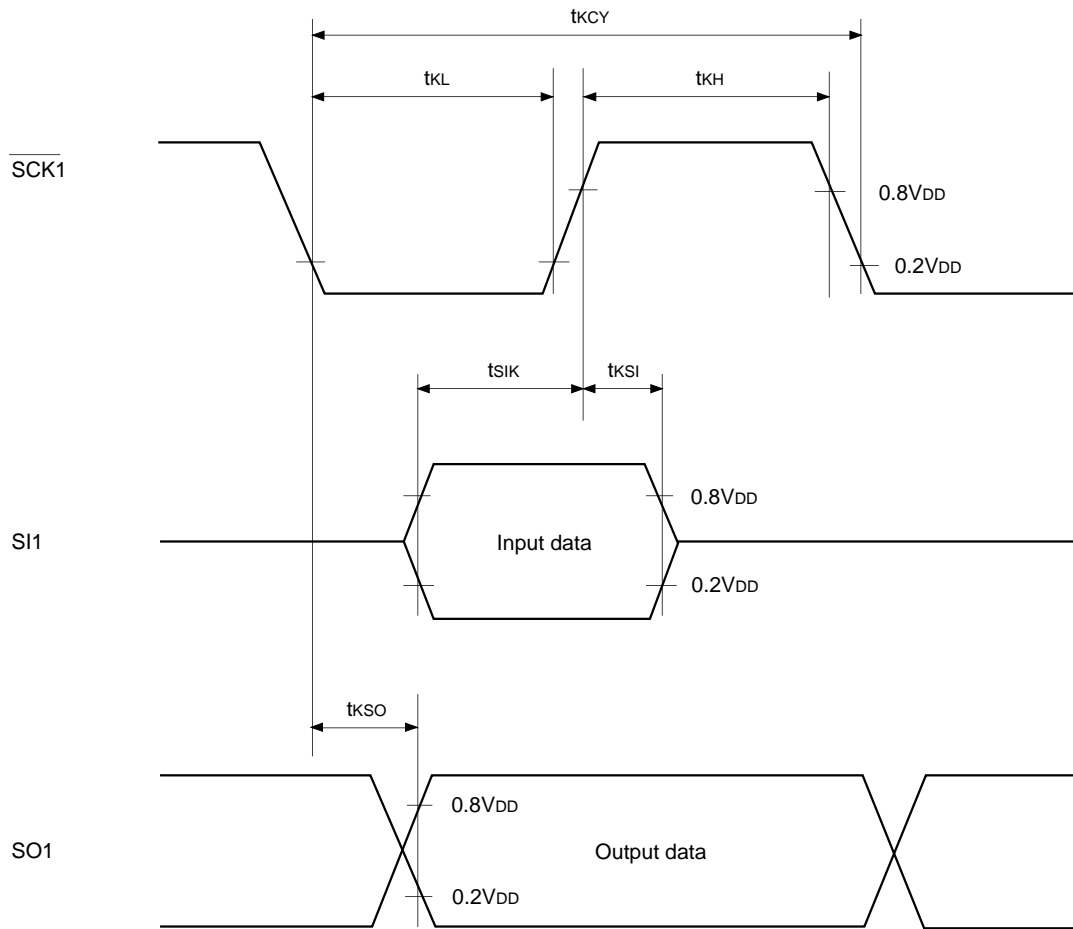
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 150$		ns
SI1 input setup time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode) (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO1 cycle time	t _{LCY}	SO1 SI1	Note 1)		104		μs
SI1 data setup time	t _{LSU}	SI1		2			μs
SI1 data hold time	t _{LHD}	SI1		2			μs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at 104μs.

Note 2) The load of SO1 pin is 50pF + 1TTL.

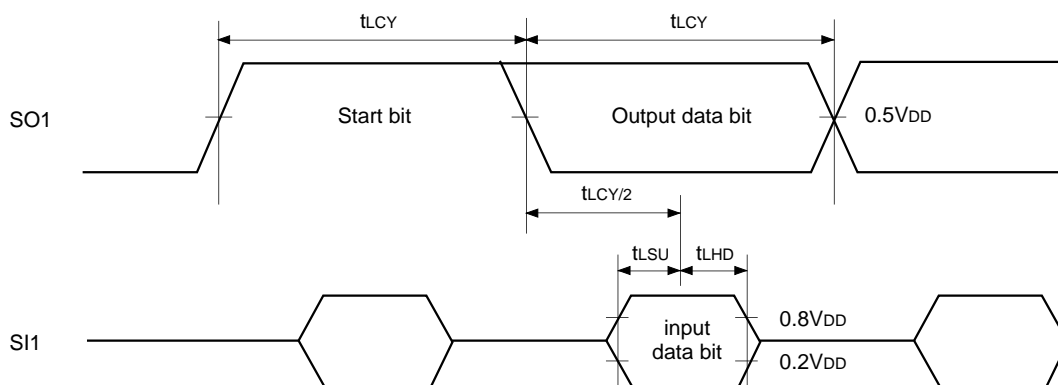
Serial transfer (CH1) (Special mode) (Ta = -20 to +75°C, VDD = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
SO1 cycle time	t _{LCY}	SO1 SI1	Note 1)		104		μs
SI1 data setup time	t _{LSU}	SI1		2			μs
SI1 data hold time	t _{LHD}	SI1		2			μs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FAH) lower 2 bits (SO1 clock selection) has been set at 104μs.

Note 2) The load of SO1 pin is 50pF.

Fig. 6. Serial transfer CH1 timing (Special mode)

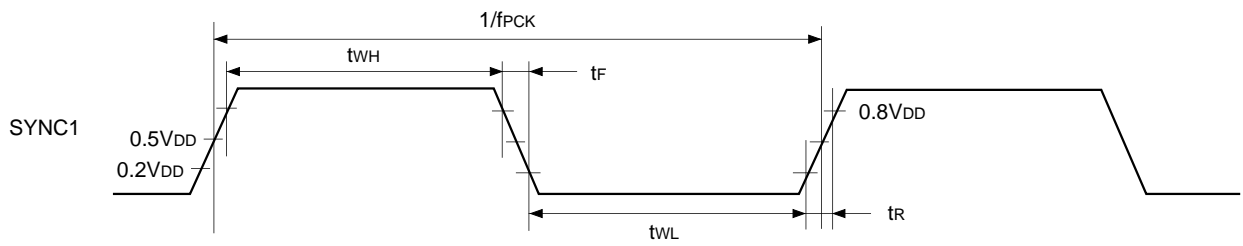


(3) General purpose prescaler

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	SYNC1				12	MHz
External clock input pulse width	t_{WH} , t_{WL}	SYNC1		33			ns
External clock input rise and fall times	t_R , t_F	SYNC1				200	ns

Fig. 7. General purpose prescaler timing



(4) HSYNC counter

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

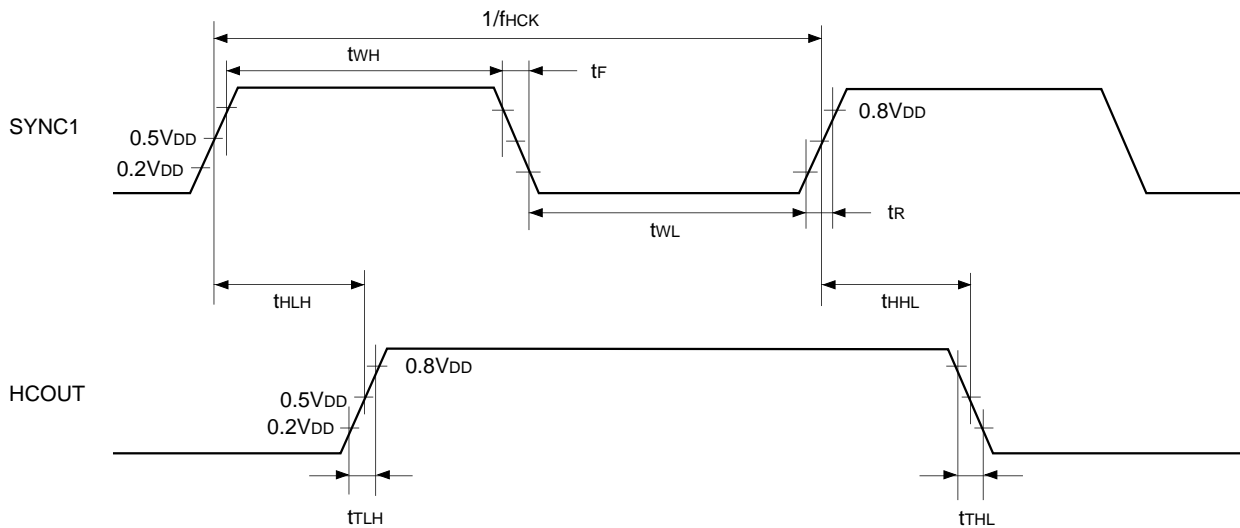
Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	unit
External clock input frequency	f_{HCK}	SYNC1				12	MHz
External clock input pulse width	t_{WH} , t_{WL}	SYNC1		33			ns
External clock input rise/fall time	t_R t_F	SYNC1				200	ns
HCOUT output delay time (against SYNC1 \uparrow)	t_{HLH}	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$		$t_{sys} + 130$	$t_{sys} + 220$	ns
	t_{HHL}				$t_{sys} + 90$	$t_{sys} + 150$	ns
HCOUT output rise/fall time	t_{TLH}	HCOUT	External clock input SYNC1 $t_R = t_F = 6\text{ns}$		100	280	ns
	t_{THL}				30	70	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{sys} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Note 2) The load of HCOUT pin is 50pF.

Fig. 8. HSYNC counter timing



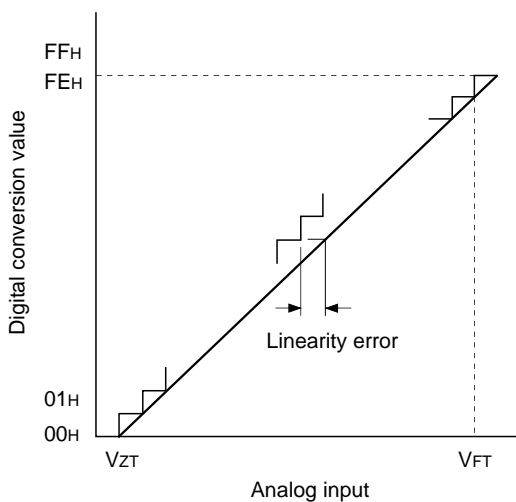
(5) A/D converter characteristics (Ta = -20 to +75°C, VDD = AVDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, VSS = AVSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 5.0V VSS = AVSS = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t _{CONV}			160/f _{ADC} *			µs
Sampling time	t _{SAMP}			12/f _{ADC} *			µs
Reference input voltage	V _{REF}	AV _{REF}	VDD = AVDD = 4.5 to 5.5V	AVDD - 0.5		AVDD	V
Analog input voltage	V _{IAN}	AN0 to AN11		0			V
AV _{REF} current	I _{REF}	AV _{REF}	Operating mode		0.6	1.0	mA
	I _{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

(Ta = -20 to +75°C, VDD = AVDD = 3.0 to 3.6V, AVREF = 2.7 to AVDD, VSS = AVSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 3.0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t _{CONV}			160/f _{ADC} *			µs
Sampling time	t _{SAMP}			12/f _{ADC} *			µs
Reference input voltage	V _{REF}	AV _{REF}	VDD = AVDD = 3.0 to 3.6V	AVDD - 0.3		AVDD	V
Analog input voltage	V _{IAN}	AN0 to AN11		0			V
AV _{REF} current	I _{REF}	AV _{REF}	Operating mode		0.4	0.7	mA
	I _{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	µA

Fig. 9. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
 When PS2 is selected, f_{ADC} = fc/2
 When PS1 is selected, f_{ADC} = fc

(6) Interruption, reset input

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ NMI PJ0 to PJ7		1		μs
Reset input low level width	t_{RSL}	$\overline{\text{RST}}$		$32/f_c$		μs

Fig. 10. Interruption input timing

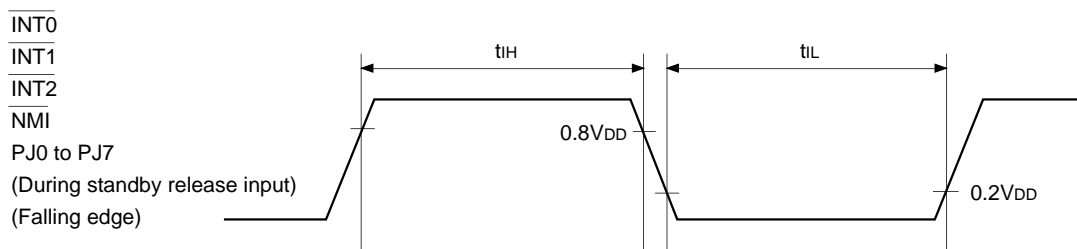
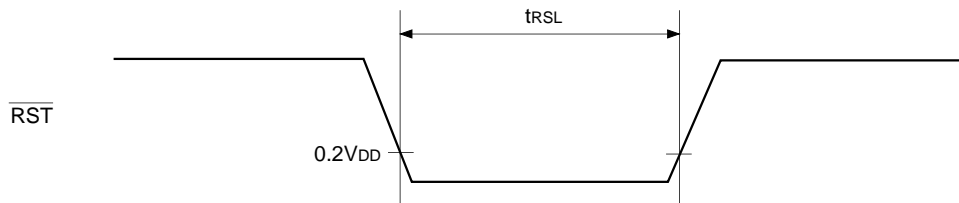


Fig. 11. Reset input timing



(7) Others

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

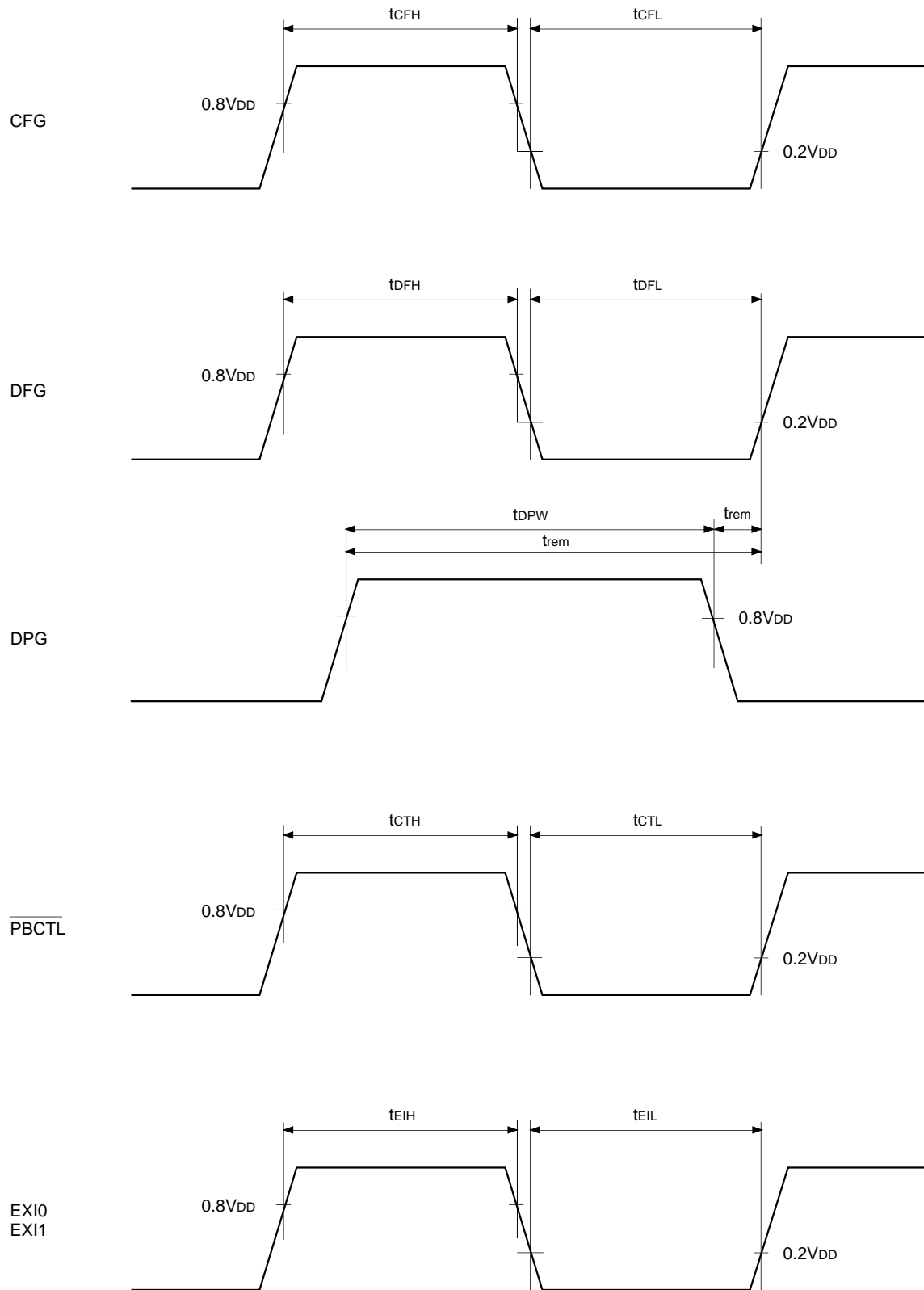
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 16 + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		$t_{FRC} \times 8 + 200$		ns
DPG minimum removal time	t_{rem}	DPG		$t_{FRC} \times 16 + 200$		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{\text{PBCTL}}$	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	$t_{sys} = 2000/f_c$	$t_{FRC} \times 8 + 200 + t_{sys}$		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

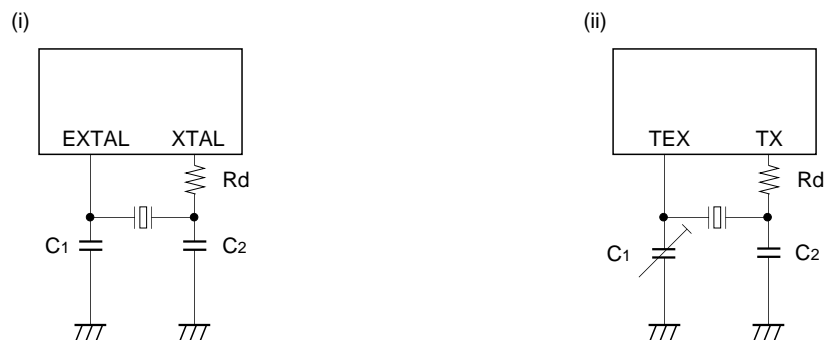
$t_{FRC} = 1000/f_c$ [ns]

Fig. 12. Other timings



Supplement

Fig. 13. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)

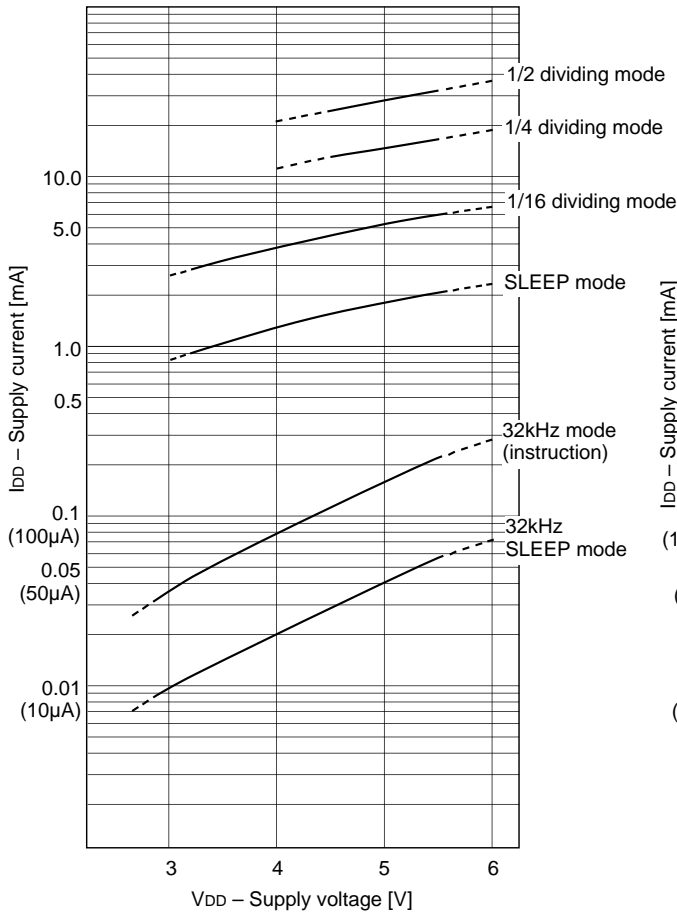
Mask option table

Item	Content	
	Reset pin pull-up resistor	Non-existent
Input circuit format*	C-MOS schmitt	TTL schmitt

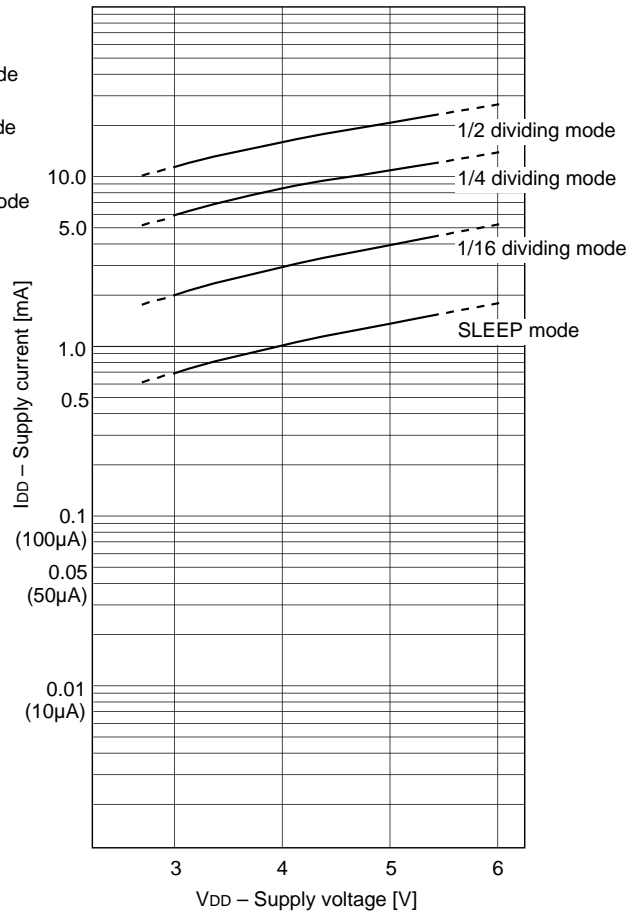
* In PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin. However, TTL schmitt can not be selected when the supply voltage (V_{DD}) ranges 3.0V to 5.5V.

Characteristics Curve

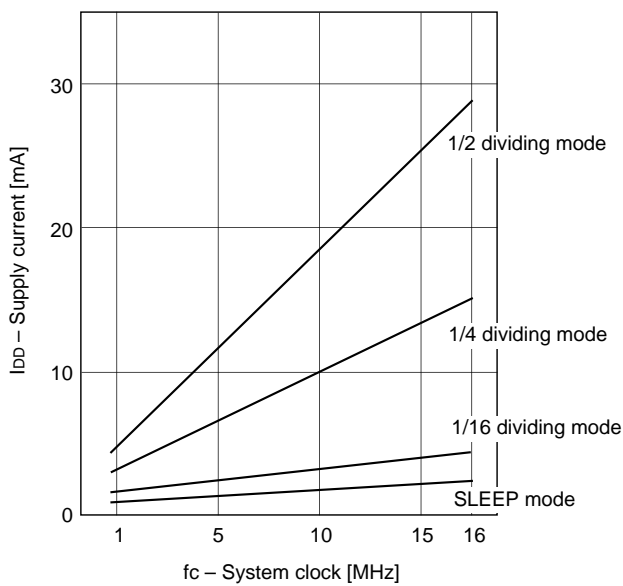
I_{DD} vs. V_{DD}
(f_c = 16MHz, T_a = 25°C, Typical)



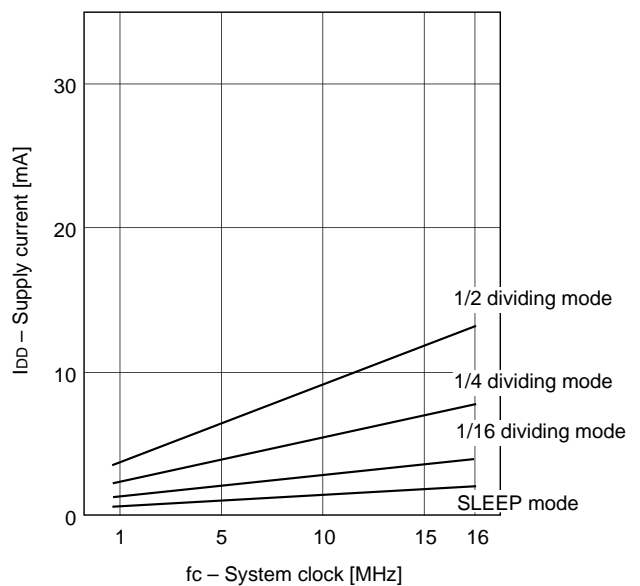
I_{DD} vs. V_{DD}
(f_c = 12MHz, T_a = 25°C, Typical)



I_{DD} vs. f_c
(V_{DD} = 5.0V, T_a = 25°C, Typical)



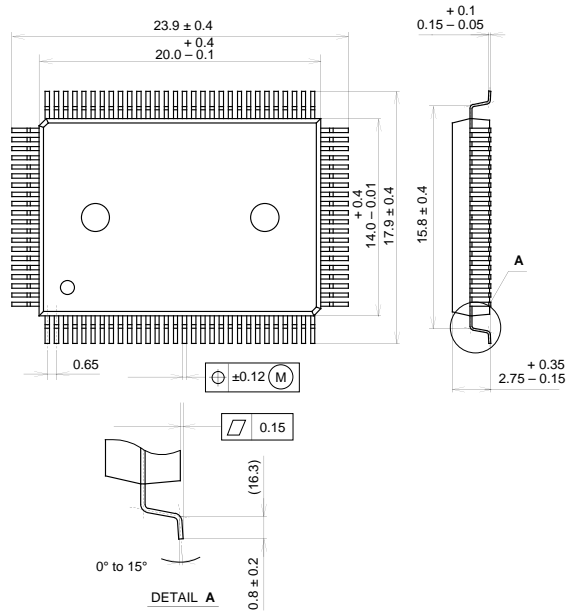
I_{DD} vs. f_c
(V_{DD} = 3.3V, T_a = 25°C, Typical)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

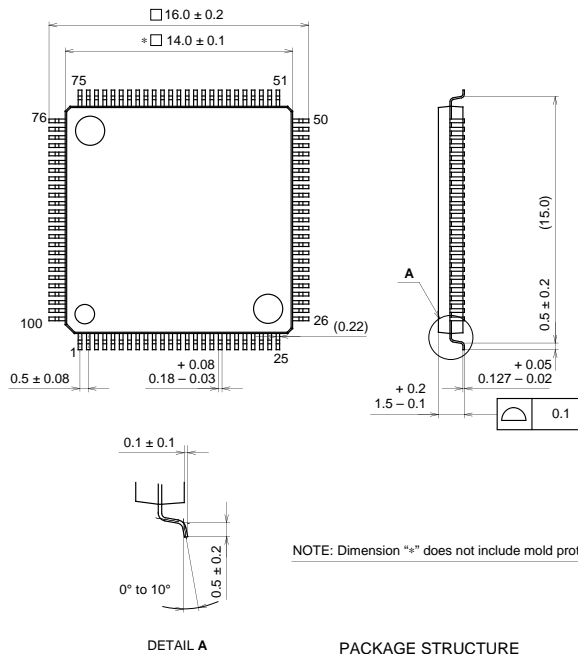


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	