

# DATA SHEET

## **TDA9859**

Universal hi-fi audio processor for  
TV

Preliminary specification  
File under Integrated Circuits, IC02

1997 Sep 01

# Universal hi-fi audio processor for TV

# TDA9859

## FEATURES

- Multi-source selector switches six AF inputs (three stereo sources or six mono sources)
- Each of the input signals can be switched to each of the outputs (crossbar switch)
- Outputs for loudspeaker channel and peri-TV connector (SCART)
- Switchable spatial stereo and pseudo stereo effects
- Audio surround decoder can be added externally
- Two general purpose logic output ports
- I<sup>2</sup>C-bus control of all functions.



## GENERAL DESCRIPTION

The TDA9859 provides control facilities for the main and the SCART channel of a TV set. Due to extended switching possibilities, signals from three stereo sources can be handled.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>P</sub>	positive supply voltage (pin 6)	7.2	8.0	8.8	V
I <sub>P</sub>	supply current	–	25	–	mA
V <sub>i(rms)</sub>	input signal levels for 0 dB gain (RMS value)	2	–	–	V
V <sub>o(rms)</sub>	output signal levels for 0 dB gain (RMS value)	2	–	–	V
G <sub>v</sub>	voltage gain in main channel				
	volume control (1 dB steps, balance included)	–63	–	+15	dB
	mute	–80	–	–	dB
	bass control (1.5 dB steps)	–12	–	+15	dB
	treble control (3 dB steps)	–12	–	+12	dB
THD	total harmonic distortion	–	0.1	–	%
S/N	signal-to-noise ratio	–	85	–	dB
T <sub>amb</sub>	operating ambient temperature	0	–	70	°C

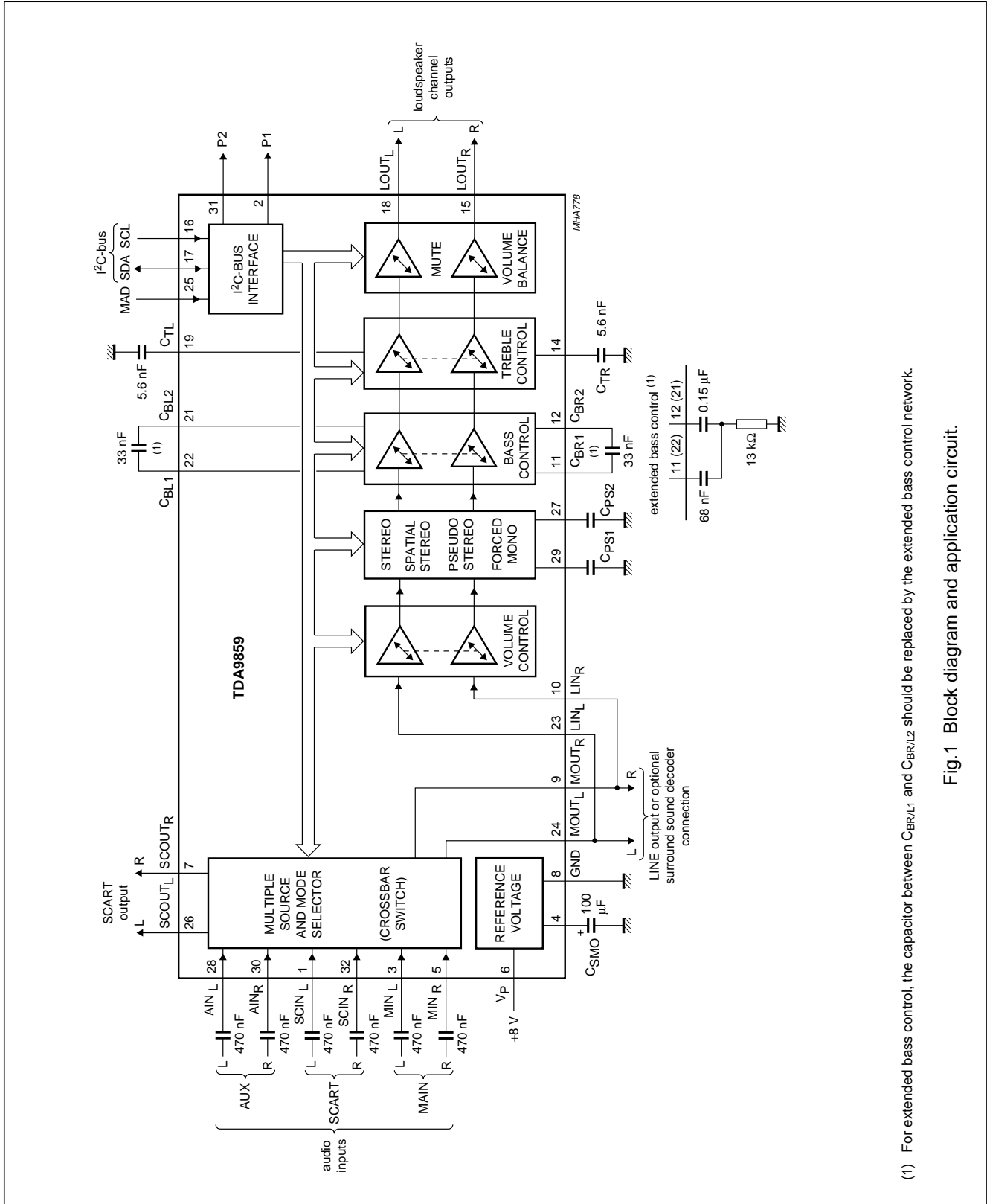
## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9859	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1

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## BLOCK DIAGRAM



(1) For extended bass control, the capacitor between CBR1/L1 and CBR2/L2 should be replaced by the extended bass control network.

Fig.1 Block diagram and application circuit.

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## PINNING

SYMBOL	PIN	DESCRIPTION
SCIN <sub>L</sub>	1	SCART input; left channel
P1	2	port 1 output
MIN <sub>L</sub>	3	MAIN input; left channel
C <sub>SMO</sub>	4	smoothing capacitor of reference voltage
MIN <sub>R</sub>	5	MAIN input; right channel
V <sub>P</sub>	6	supply voltage
SCOUT <sub>R</sub>	7	SCART output; right channel
GND	8	ground
MOU <sub>T</sub> R	9	MAIN output; right channel
LIN <sub>R</sub>	10	input to right loudspeaker channel
C <sub>BR1</sub>	11	bass capacitor connection 1; right channel
C <sub>BR2</sub>	12	bass capacitor connection 2; right channel
n.c.	13	not connected
C <sub>TR</sub>	14	treble capacitor connection; right channel
LOU <sub>T</sub> R	15	loudspeaker output; right channel
SCL	16	serial clock input; I <sup>2</sup> C-bus
SDA	17	serial data input/output; I <sup>2</sup> C-bus
LOU <sub>T</sub> L	18	loudspeaker output; left channel
C <sub>TL</sub>	19	treble capacitor connection; left channel
n.c.	20	not connected
C <sub>BL2</sub>	21	bass capacitor connection 2; left channel
C <sub>BL1</sub>	22	bass capacitor connection 1; left channel
LIN <sub>L</sub>	23	input to left loudspeaker channel
MOU <sub>T</sub> L	24	MAIN output; left channel
MAD	25	module address select input
SCOUT <sub>L</sub>	26	SCART output; left channel
C <sub>PS2</sub>	27	pseudo stereo capacitor 2
AIN <sub>L</sub>	28	AUX input; left channel
C <sub>PS1</sub>	29	pseudo stereo capacitor 1
AIN <sub>R</sub>	30	AUX input; right channel
P2	31	port 2 output
SCIN <sub>R</sub>	32	SCART input signal RIGHT

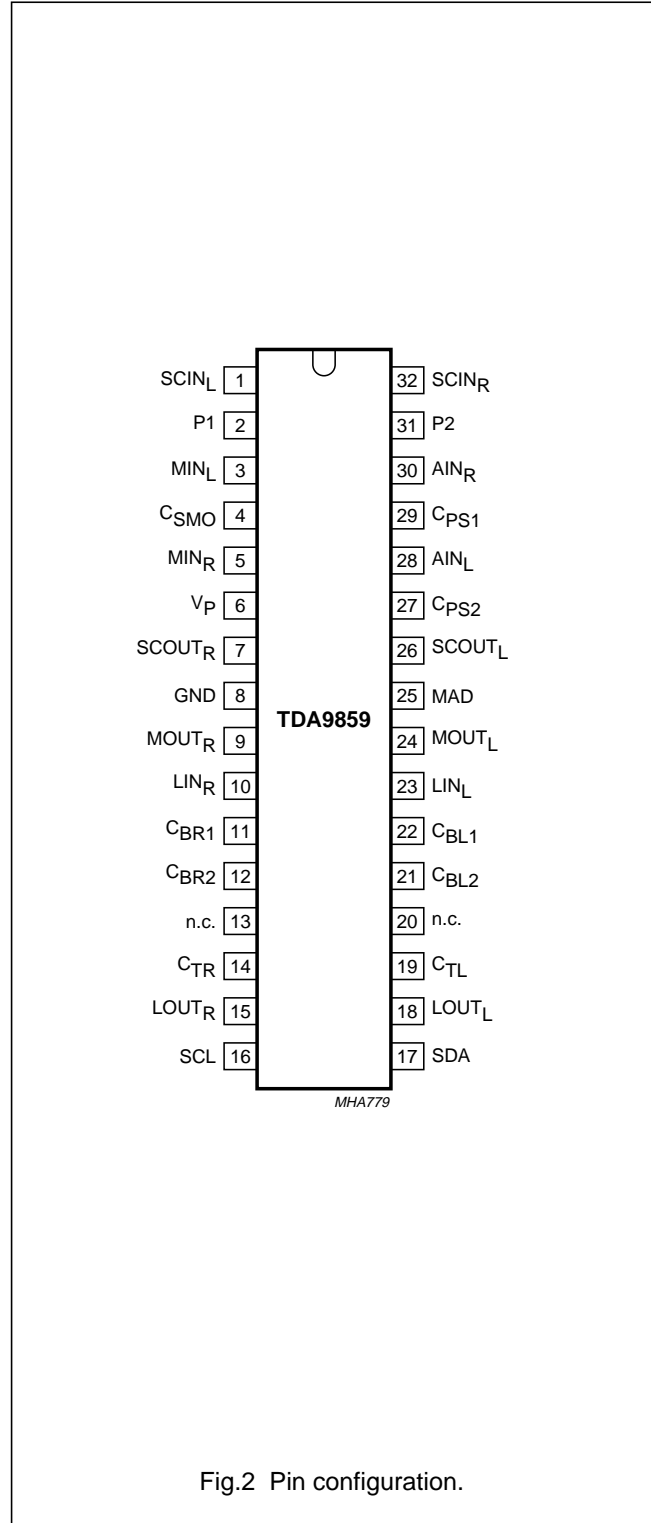


Fig.2 Pin configuration.

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## FUNCTIONAL DESCRIPTION

The TDA9859 consists of the following functions:

- Source select switching block
- Loudspeaker channel with effect controls
- Two port outputs for general purpose
- I<sup>2</sup>C-bus control.

### Source select switching block

The TDA9859 selects and switches the input signals from three stereo or six mono sources MAIN, AUX and SCART (see Fig.1) to the outputs SCART and loudspeaker (crossbar-switching; Table 4). The main channel (LINE outputs) is looped outside the circuit (from pins 9 and 24 to pins 10 and 23), so signals can be used as LINE output or a surround sound decoder can be inserted.

### Loudspeaker channel

Volume control is divided into volume control common and volume control left/right. The common part (–40 to +15 dB) controls the left and right channels

simultaneously; the left/right part (–23 to 0 dB) controls the volume of left and right channels independently. Treble control provides a control range from –12 to +12 dB and bass control from –12 to +15 dB. Extended bass control can be provided by an external T-network (see Fig.1) from –15 to +19 dB (2 dB steps).

### Effect controls

'Linear stereo', 'stereo with spatial effect (30% or 52% anti-phase crosstalk)' and 'forced mono with or without pseudo-stereo effect' are controlled by three bits. A muting of 85 dB is provided.

### I<sup>2</sup>C-bus control

All settings of control are stored in subaddress registers. Data transmission is simplified by auto-incrementing the subaddresses. The on-chip Power-on reset sets the mute bit to active, so both the SCART and the loudspeaker outputs are muted.

The muting can be switched off by writing a '0' (non-muted) into the mute control bits.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage (pin 6)	0	10	V
V <sub>n</sub>	voltage on all pins, ground excluded	0	V <sub>P</sub>	V
I <sub>O</sub>	output current			
	at LOUT and SCOUT pins	–	2.5	mA
	at port output pins	–	1.5	mA
P <sub>tot</sub>	total power dissipation	–	850	mW
T <sub>amb</sub>	operating ambient temperature	0	70	°C
T <sub>stg</sub>	storage temperature	–25	+150	°C
V <sub>es</sub>	electrostatic handling for all pins; note 1	–	±300	V
	electrostatic handling for all pins; note 2	–	±2000	V

### Notes

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (Machine Model).
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor (Human Body Model).

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	60	K/W

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**CHARACTERISTICS**

$V_P = 8\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; treble and bass in linear positions (0 dB); volume control left/right 0 dB; spatial function, pseudo-stereo function and forced-mono function in off position and measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pin 6)		7.2	8.0	8.8	V
$I_P$	supply current (pin 6)		–	25	–	mA
$V_{ref}$	internal reference voltage		–	$0.5V_P$	–	V
$V_4$	voltage at pin 4		–	$V_P - 0.1$	–	V
<b>DC voltage on pins</b>						
$V_I$	DC input voltage at pins 1, 3, 5, 10, 23, 28, 30 and 32 (inputs SCIN, MIN, LIN and AIN)		–	$0.5V_P$	–	V
$V_O$	DC output voltage at pins 7, 9, 15, 18, 24, 26 (outputs SCOUT, MOUT and LOU)		–	$0.5V_P$	–	V
$V_C$	DC voltage on capacitors (pins 11, 12, 14, 19, 21, 22, 27 and 29)		–	$0.5V_P$	–	V
<b>Audio select switch; line and SCART outputs (controlled via I<sup>2</sup>C-bus); see Table 4</b>						
$V_{i(rms)}$	maximum AF input signal on pins SCIN, MIN and AIN (RMS value)	THD $\leq 0.5\%$ on output pins	2	–	–	V
$R_i$	input resistance (pins SCIN, MIN and AIN)		20	30	40	k $\Omega$
$B_{-0.5\text{ dB}}$	–0.5 dB bandwidth for pins SCOUT, MOUT and LOU.		20	–	20 000	Hz
$V_{o(rms)}$	maximum AF output signal on pins SCOUT and MOUT (RMS value)	THD $\leq 0.5\%$	2	–	–	V
$R_L$	allowed external load resistance on output (pins MOUT)		10	–	–	k $\Omega$
	on output (pins SCOUT)		5	–	–	k $\Omega$
$G_v$	voltage gain from any input to SCART and MAIN outputs		–	0	–	dB
$\alpha_{cr}$	switch crosstalk on outputs between AF inputs at $f = 10\text{ kHz}$	unused inputs connected to ground	–	90	–	dB
<b>Volume control common (f = 1 kHz, 55 steps)</b>						
$V_{i(rms)}$	maximum input signal (RMS value; pins LIN)	$G_v = 0$ ; THD $\leq 0.5\%$ on output pins 15 and 18	2	–	–	V
$R_i$	input resistance (pins LIN)		7.5	10	–	k $\Omega$
$G_v$	volume control common voltage gain nominal		–40	–	+15	dB
	minimum		–38	–	+14	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_V$	volume control common voltage gain step width	$G_V = -32$ to $+15$ dB $G_V = -40$ to $-33$ dB	0.5 0.25	1.0 1.0	1.5 1.75	dB dB
	volume control common voltage gain set error	$G_V = -32$ to $+15$ dB $G_V = -40$ to $-33$ dB	– –	– –	1 2	dB dB
<b>Volume control left/right (f = 1 kHz, 24 steps)</b>						
$G_V$	volume control left/right voltage gain nominal		–24	–	0	dB
	minimum		–23	–	–1	dB
	mute position		–80	–85	–	dB
$\Delta G_V$	volume control left/right voltage gain step width		0.5	1.0	1.5	dB
	volume control left/right voltage gain tracking error		–	–	2	dB
<b>Bass control</b>						
$G_V$	bass control voltage gain maximum boost	$C_B = 33$ nF f = 40 Hz	14	15	16	dB
	maximum attenuation	f = 40 Hz	11	12	13	dB
$\Delta G_V$	bass control voltage gain step width		1	1.5	2	dB
$G_{V(\text{extended})}$	extended bass control voltage gain maximum boost	see Fig.1 f = 60 Hz	18	19	20	dB
	maximum attenuation	f = 60 Hz	14	15	16	dB
$\Delta G_{V(\text{extended})}$	extended bass control voltage gain step width		1	2	3	dB
<b>Treble control</b>						
$G_V$	treble control voltage gain maximum boost	f = 15 kHz	11	12	13	dB
	maximum attenuation	f = 15 kHz	11	12	13	dB
$\Delta G_V$	treble control voltage gain step width		2.5	3	3.5	dB
<b>Effect controls</b>						
$\alpha_{\text{ct}(\text{spat}1)}$	anti-phase crosstalk by spatial effect 1		–	52	–	%
$\alpha_{\text{ct}(\text{spat}2)}$	anti-phase crosstalk by spatial effect 2		–	30	–	%
$\varphi$	phase shift by pseudo-stereo		see Fig.3			
<b>Loudspeaker channel outputs (pins 15 and 18)</b>						
$V_{o(\text{max})}(\text{rms})$	maximum output signal (RMS value)	THD $\leq$ 0.5%; $R_L >$ 10 k $\Omega$ ; $C_L <$ 1.5 nF	2	–	–	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta V_{15,18}$	maximum DC offset voltage between adjoining step and any step to mute for volume control	$G_V = 0$ to +15 dB/mute	–	2	15	mV
		$G_V = -64$ to 0 dB/mute	–	0.5	10	mV
	for bass control	$G_V = 0$ to +15 dB/mute	–	2	15	mV
		$G_V = -12$ to 0 dB/mute	–	0.5	10	mV
		for treble control	$G_V = -12$ to +12 dB/mute	–	0.5	10
$R_o$	output resistance		–	–	100	$\Omega$
$R_{o(L)}$	allowed output load resistor		10	–	–	k $\Omega$
$C_{o(L)}$	allowed output load capacitor		–	–	1.5	nF
$V_{no(W)}$	weighted noise voltage at output (quasi-peak level)	CCIR 468-3 weighted				
		$G_V = +15$ dB	–	102	–	$\mu$ V
		$G_V = 0$ dB	–	32	–	$\mu$ V
		$G_V = -40$ dB	–	27	–	$\mu$ V
	$G_V = -80$ dB (mute)	–	20	–	$\mu$ V	
$B_{-1\text{ dB}}$	–1 dB bandwidth for loudspeaker channel		20	–	20000	Hz
THD	total harmonic distortion for $V_{i(rms)} = 0.2$ V for $V_{i(rms)} = 1$ V for $V_{i(rms)} = 2$ V	$f = 20$ to 12500 Hz				
		$G_V = -30$ to +15 dB	–	0.1	0.3	%
		$G_V = -30$ to 0 dB	–	0.1	0.3	%
	$G_V = -30$ to –6 dB	–	0.1	0.3	%	
$\alpha_{cs(l-r)}$	stereo channel separation	$f = 10$ kHz; $G_V = 0$ dB; opposite input grounded by 1 k $\Omega$ resistor	–	75	–	dB
$\alpha_{ct(bus)}$	crosstalk from I <sup>2</sup> C-bus to AF outputs $\alpha_{bus} = 20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$ ( $V_{bus}$ = spurious I <sup>2</sup> C-bus signal voltage on AF output).	$G_V = 0$ dB	–	100	–	dB
$PSRR_{100}$	power supply ripple rejection with 100 Hz ripple	$G_V = 0$ dB; $V_{R(rms)} < 200$ mV	–	55	–	dB
<b>SCART output (pins 7 and 26)</b>						
$V_{o(max)(rms)}$	maximum output signal (RMS value)	THD $\leq 0.5\%$ ; $R_L > 5$ k $\Omega$	2	–	–	V
$R_{o(L)}$	output load resistor		5	–	–	k $\Omega$
<b>Power-on reset</b>						
$V_{PONR}$	increasing supply voltage start of reset end of reset		–	–	2.5	V
			5.2	6.0	6.8	V
$V_{PONR}$	decreasing supply voltage start of reset		4.4	5.2	6.0	V
<b>I<sup>2</sup>C-bus, SCL and SDA (pins 16 and 17)</b>						
$V_{IH}$	HIGH-level input voltage		3	–	$V_P$	V



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IL}$	LOW-level input voltage		0	–	1.5	V
$I_I$	input current		–	–	$\pm 10$	$\mu\text{A}$
$V_{ACK}$	output voltage at acknowledge (pin 17)	$I_{17} = -3 \text{ mA}$	–	–	0.4	V
<b>Module address (pin 25)</b>						
$V_{IL}$	LOW-level input voltage		0	–	1.5	V
$V_{IH}$	HIGH-level input voltage		3	–	$V_P$	V
<b>Port outputs P1 and P2 (open-collector outputs pins 2 and 31)</b>						
$V_{OL}$	LOW-level output voltage	$I_{O(\text{sink})} = 1 \text{ mA}$	–	–	0.3	V
$I_{O(\text{sink})}$	port output sink current		–	–	1	mA

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**I<sup>2</sup>C-BUS PROTOCOL**

This circuit operates as a slave receiver only. For more information about the I<sup>2</sup>C-bus, see "The I<sup>2</sup>C-bus and how to use it", order number 9398 393 40011.

**I<sup>2</sup>C-bus format**

S	SLAVE ADDRESS	$\bar{W}$	A	SUBADDRESS	A	DATA <sup>(1)</sup>	A <sup>(1)</sup>	P
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**Note**

- Multiple DATA-A (acknowledge) sequences may occur.

**Table 1** Explanation of I<sup>2</sup>C-bus format

NAME	DESCRIPTION
S	START condition (SCL HIGH, SDA HIGH-to-LOW)
SLAVE ADDRESS	100 0000 ( $V_{25} = \text{LOW}$ ) or 100 0001 ( $V_{25} = \text{HIGH}$ )
$\bar{W}$	0
A	acknowledge (SDA = LOW); generated by the device
SUBADDRESS	subaddress (byte); see Table 2
DATA <sup>(1)</sup>	data byte; see Table 2
P	STOP condition (SCL = HIGH, SDA = LOW-to-HIGH)

**Note**

- If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed by the device.

**Table 2** I<sup>2</sup>C-bus transmission

FUNCTION	SUBADDRESS		DATA BITS							
	BINARY	HEX	D7	D6	D5	D4	D3	D2	D1	D0
<b>Loudspeaker channel</b>										
Volume control common	0000 0000	00	0	0	V05	V04	V03	V02	V01	V00
Volume control left	0000 0001	01	0	0	0	VL4	VL3	VL2	VL1	VL0
Volume control right	0000 0010	02	0	0	0	VR4	VR3	VR2	VR1	VR0
Bass control	0000 0011	03	0	0	0	BA4	BA3	BA2	BA1	BA0
Treble control	0000 0100	04	0	0	0	0	TR3	TR2	TR1	TR0
<b>Switching control byte</b>										
SCART output <sup>(1)</sup>	0000 1000	08	0	MU1	P1	P2	I13	I12	I11	I10
Loudspeaker output	0000 1001	09	EF2	MU2	EF1	ST	I23	I22	I21	I20

**Note**

- If auto-increment of the subaddress is used, it is necessary to insert three dummy data words between the treble control byte and the switching control bytes.

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**Table 3** Function of the bits in Table 2

<b>BITS</b>	<b>FUNCTION</b>
V00 to V05	volume control common for loudspeaker channel; see Table 9
VL0 to VL4	volume control for left loudspeaker channel; see Table 6
VR0 to VR4	volume control for right loudspeaker channel; see Table 6
BA0 to BA4	bass control for left and right loudspeaker channels; see Table 7
TR0 to TR3	treble control for left and right loudspeaker channels; see Table 8
I10 to I13	input selection for SCART channels; see Table 4
I20 to I23	input selection for loudspeaker channels; see Table 4
MU1 and MU2	mute control bits (MU1 for SCART channel, MU2 for loudspeaker channel) 0 = channel not muted 1 = channel muted
EF1, EF2 and ST	effect control bits for loudspeaker channel; see Table 5
P1 and P2	control bits for ports P1 (pin 2) and P2 (pin 31) control bit = 0: ports P1 = LOW control bit = 1: ports P1 = HIGH

**Table 4** Input selection

<b>INPUT</b>	<b>BITS OF DATA BYTE 8 AND 9</b>								
	<b>HEX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
AUX LEFT	XB <sup>(1)</sup>	(1)	MU	(1)	(1)	1	0	1	1
AUX RIGHT	X9 <sup>(1)</sup>	(1)	MU	(1)	(1)	1	0	0	1
AUX STEREO	X7 <sup>(1)</sup>	(1)	MU	(1)	(1)	0	1	1	1
SCART LEFT	XA <sup>(1)</sup>	(1)	MU	(1)	(1)	1	0	1	0
SCART RIGHT	X5 <sup>(1)</sup>	(1)	MU	(1)	(1)	0	1	0	1
SCART STEREO	X6 <sup>(1)</sup>	(1)	MU	(1)	(1)	0	1	1	0
MAIN LEFT	XC <sup>(1)</sup>	(1)	MU	(1)	(1)	1	1	0	0
MAIN RIGHT	XD <sup>(1)</sup>	(1)	MU	(1)	(1)	1	1	0	1
MAIN STEREO	X8 <sup>(1)</sup>	(1)	MU	(1)	(1)	1	0	0	0

**Note**

- Byte 8 (SCART channels): The value of X depends on MU1 and control bits P1 and P2.  
Byte 9 (loudspeaker channels): see Table 5 for the programming of these bits. The value of X depends on the selected effects and MU2.

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Table 5 Effect controls

SETTING SPECIAL EFFECTS	DATA BYTE TO SUBADDRESS 09								
	HEX	EF2	MU2	EF1	ST	I23	I22	I21	I20
Stereo with spatial effect 1 (52%)	BX <sup>(1)</sup>	1	0	1	1	(1)	(1)	(1)	(1)
Stereo with spatial effect 2 (30%)	3X <sup>(1)</sup>	0	0	1	1	(1)	(1)	(1)	(1)
Stereo without spatial effect	1X <sup>(1)</sup>	0	0	0	1	(1)	(1)	(1)	(1)
Forced mono with pseudo stereo	2X <sup>(1)</sup>	0	0	1	0	(1)	(1)	(1)	(1)
Forced mono without pseudo stereo	0X <sup>(1)</sup>	0	0	0	0	(1)	(1)	(1)	(1)

## Note

1. See Table 4. The value of X depends on the selected input.

Table 6 Volume control left/right

G <sub>v</sub> (dB)	DATA BITS					
	HEX	VL4	VL3	VL2	VL1	VL0
		VR4	VR3	VR2	VR1	VR0
0	1F	1	1	1	1	1
-1	1E	1	1	1	1	0
-2	1D	1	1	1	0	1
-3	1C	1	1	1	0	0
-4	1B	1	1	0	1	1
-5	1A	1	1	0	1	0
-6	19	1	1	0	0	1
-7	18	1	1	0	0	0
-8	17	1	0	1	1	1
-9	16	1	0	1	1	0
-10	15	1	0	1	0	1
-11	14	1	0	1	0	0
-12	13	1	0	0	1	1
-13	12	1	0	0	1	0
-14	11	1	0	0	0	1
-15	10	1	0	0	0	0
-16	0F	0	1	1	1	1
-17	0E	0	1	1	1	0
-18	0D	0	1	1	0	1
-19	0C	0	1	1	0	0
-20	0B	0	1	0	1	1
-21	0A	0	1	0	1	0
-22	09	0	1	0	0	1
-23	08	0	1	0	0	0
Mute	07	0	0	1	1	1

Table 7 Bass control

G <sub>v</sub> (dB)	DATA BITS					
	HEX	BA4	BA3	BA2	BA1	BA0
+15	19	1	1	0	0	1
+13.5	18	1	1	0	0	0
+12	17	1	0	1	1	1
+10.5	16	1	0	1	1	0
+9	15	1	0	1	0	1
+7.5	14	1	0	1	0	0
+6	13	1	0	0	1	1
+4.5	12	1	0	0	1	0
+3	11	1	0	0	0	1
+1.5	10	1	0	0	0	0
0	0F	0	1	1	1	1
0	0E	0	1	1	1	0
-1.5	0D	0	1	1	0	1
-3	0C	0	1	1	0	0
-4.5	0B	0	1	0	1	1
-6	0A	0	1	0	1	0
-7.5	09	0	1	0	0	1
-9	08	0	1	0	0	0
-10.5	07	0	0	1	1	1
-12	06	0	0	1	1	0

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Table 8 Treble control

G <sub>v</sub> (dB)	DATA BITS					
	HEX	0	TR3	TR2	TR1	TR0
+12	0A	0	1	0	1	0
+9	09	0	1	0	0	1
+6	08	0	1	0	0	0
+3	07	0	0	1	1	1
0	06	0	0	1	1	0
-3	05	0	0	1	0	1
-6	04	0	0	1	0	0
-9	03	0	0	0	1	1
-12	02	0	0	0	1	0

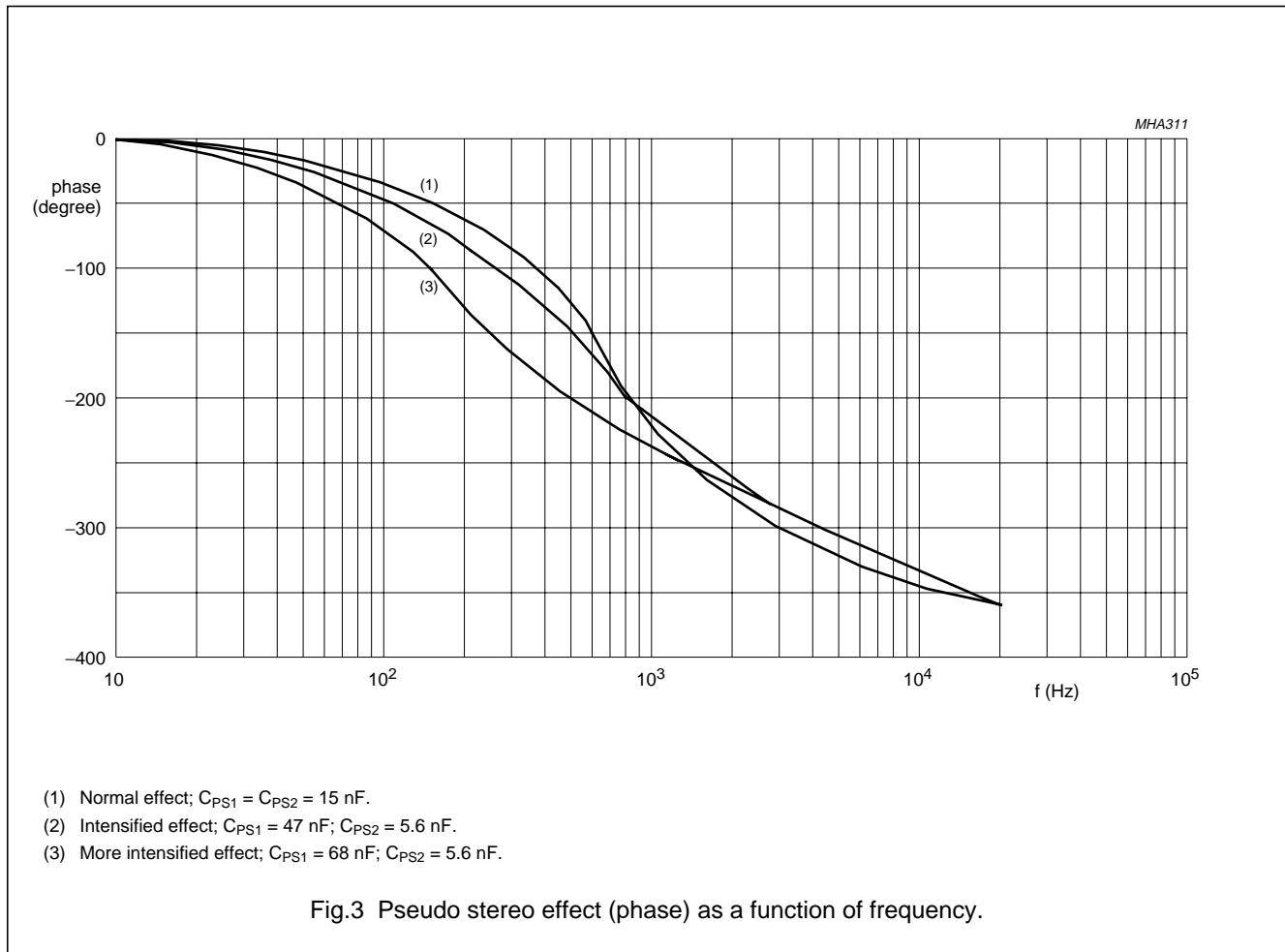
Table 9 Volume control common

G <sub>v</sub> (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
+15	3F	1	1	1	1	1	1
+14	3E	1	1	1	1	1	0
+13	3D	1	1	1	1	0	1
+12	3C	1	1	1	1	0	0
+11	3B	1	1	1	0	1	1
+10	3A	1	1	1	0	1	0
+9	39	1	1	1	0	0	1
+8	38	1	1	1	0	0	0
+7	37	1	1	0	1	1	1
+6	36	1	1	0	1	1	0
+5	35	1	1	0	1	0	1
+4	34	1	1	0	1	0	0
+3	33	1	1	0	0	1	1
+2	32	1	1	0	0	1	0
+1	31	1	1	0	0	0	1
0	30	1	1	0	0	0	0
-1	2F	1	0	1	1	1	1
-2	2E	1	0	1	1	1	0
-3	2D	1	0	1	1	0	1
-4	2C	1	0	1	1	0	0
-5	2B	1	0	1	0	1	1
-6	2A	1	0	1	0	1	0

G <sub>v</sub> (dB)	DATA BITS						
	HEX	V05	V04	V03	V02	V01	V00
-7	29	1	0	1	0	0	1
-8	28	1	0	1	0	0	0
-9	27	1	0	0	1	1	1
-10	26	1	0	0	1	1	0
-11	25	1	0	0	1	0	1
-12	24	1	0	0	1	0	0
-13	23	1	0	0	0	1	1
-14	22	1	0	0	0	1	0
-15	21	1	0	0	0	0	1
-16	20	1	0	0	0	0	0
-17	1F	0	1	1	1	1	1
-18	1E	0	1	1	1	1	0
-19	1D	0	1	1	1	0	1
-20	1C	0	1	1	1	0	0
-21	1B	0	1	1	0	1	1
-22	1A	0	1	1	0	1	0
-23	19	0	1	1	0	0	1
-24	18	0	1	1	0	0	0
-25	17	0	1	0	1	1	1
-26	16	0	1	0	1	1	0
-27	15	0	1	0	1	0	1
-28	14	0	1	0	1	0	0
-29	13	0	1	0	0	1	1
-30	12	0	1	0	0	1	0
-31	11	0	1	0	0	0	1
-32	10	0	1	0	0	0	0
-33	0F	0	0	1	1	1	1
-34	0E	0	0	1	1	1	0
-35	0D	0	0	1	1	0	1
-36	0C	0	0	1	1	0	0
-37	0B	0	0	1	0	1	1
-38	0A	0	0	1	0	1	0
-39	09	0	0	1	0	0	1
-40	08	0	0	1	0	0	0

Universal hi-fi audio processor for TV

TDA9859



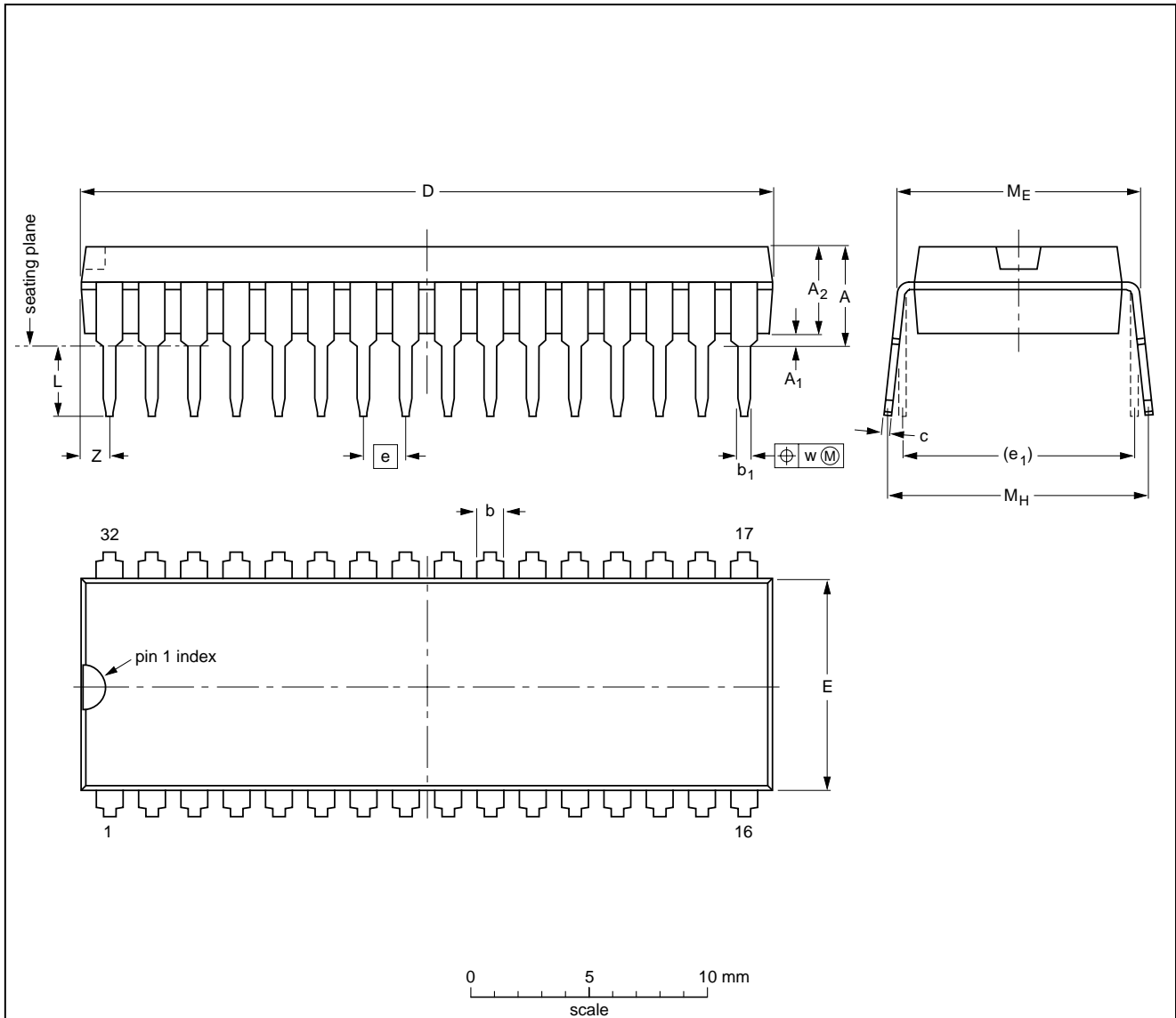
Universal hi-fi audio processor for TV

TDA9859

PACKAGE OUTLINE

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)

SOT232-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						92-11-17 95-02-04

## Universal hi-fi audio processor for TV

TDA9859

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact

with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.



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**NOTES**

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**NOTES**

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