

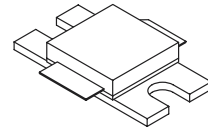
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF19030R3
MRF19030SR3

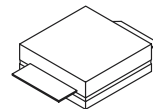
Designed for class AB PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- CDMA Performance @ 1990 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
885 kHz — -47 dBc @ 30 kHz BW
1.25 MHz — -55 dBc @ 12.5 kHz BW
2.25 MHz — -55 dBc @ 1 MHz BW
Output Power — 4.5 Watts Avg.
Power Gain — 13.5 dB
Efficiency — 17%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

2.0 GHz, 30 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-03, STYLE 1
NI-400
MRF19030R3



CASE 465F-03, STYLE 1
NI-400S
MRF19030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	83.3 0.48	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 20\ \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 300\text{ mA}$)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1960.0\text{ MHz}$, $f_2 = 1960.1\text{ MHz}$)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1960.0\text{ MHz}$, $f_2 = 1960.1\text{ MHz}$)	η	—	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1960.0\text{ MHz}$, $f_2 = 1960.1\text{ MHz}$)	IMD	—	–31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1960.0\text{ MHz}$, $f_2 = 1960.1\text{ MHz}$)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$ and $f_1 = 1990.0\text{ MHz}$, $f_2 = 1990.1\text{ MHz}$)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$ and $f_1 = 1990.0\text{ MHz}$, $f_2 = 1990.1\text{ MHz}$)	η	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$ and $f_1 = 1990.0\text{ MHz}$, $f_2 = 1990.1\text{ MHz}$)	IMD	—	–31	–28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 300\text{ mA}$, $f_1 = 1930.0\text{ MHz}$, $f_2 = 1930.1\text{ MHz}$ and $f_1 = 1990.0\text{ MHz}$, $f_2 = 1990.1\text{ MHz}$)	IRL	—	–13	–9	dB
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 30\text{ W CW}$, $I_{DQ} = 300\text{ mA}$, $f = 1930\text{ MHz}$, $V_{SWR} = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

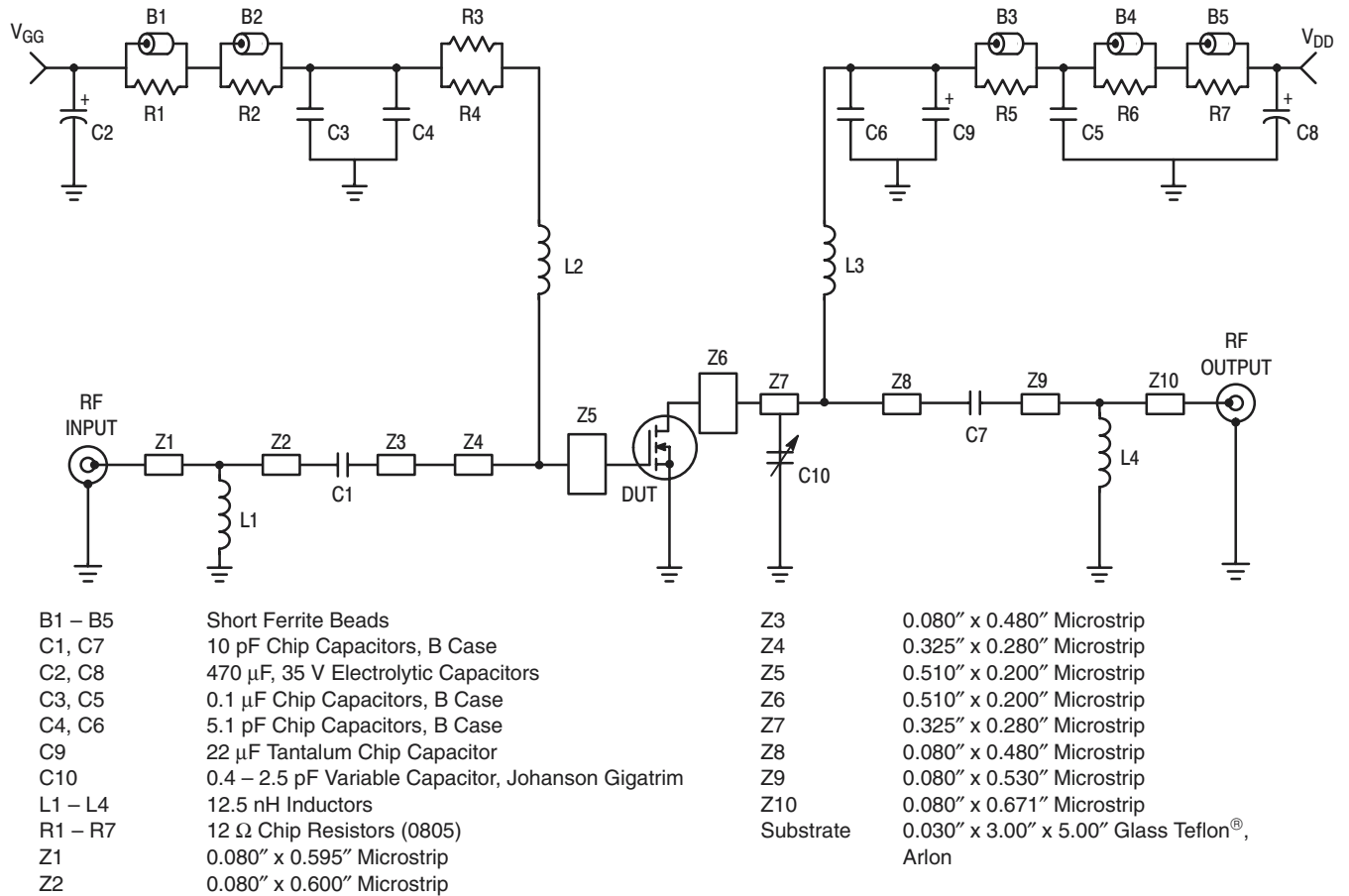


Figure 1. MRF19030 Test Circuit Schematic

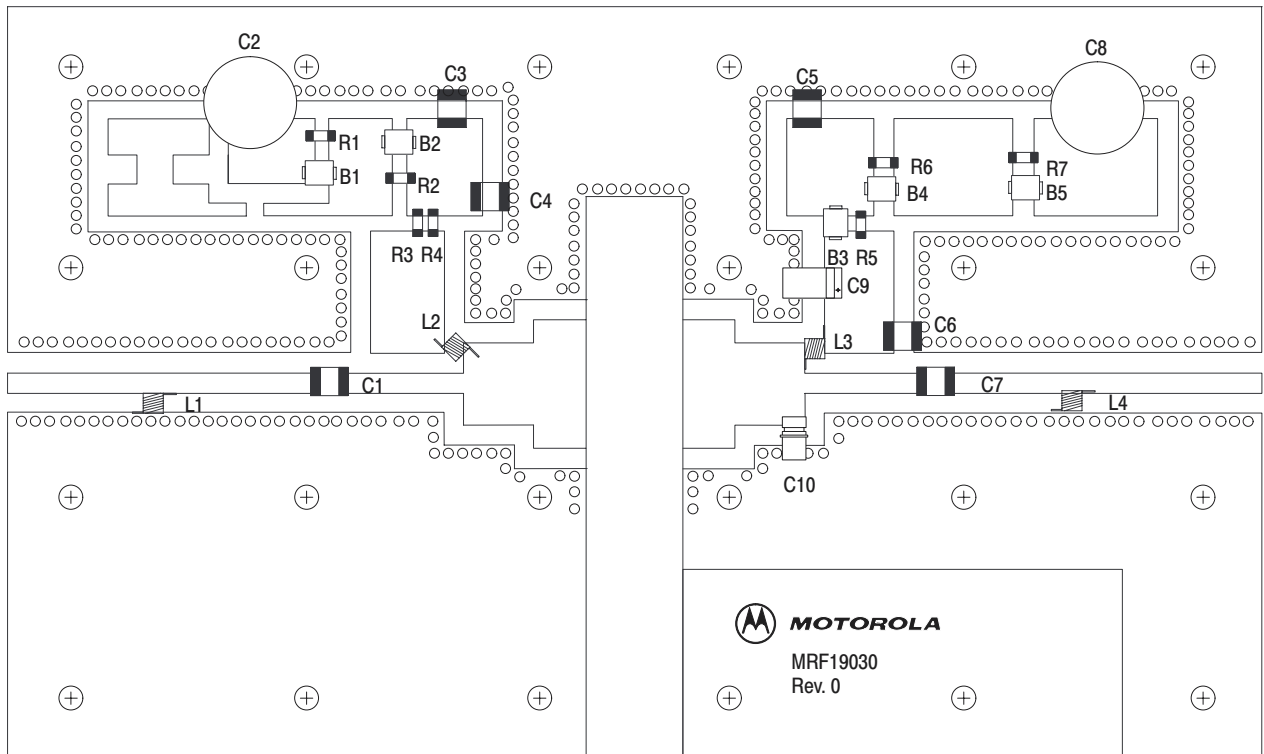


Figure 2. MRF19030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

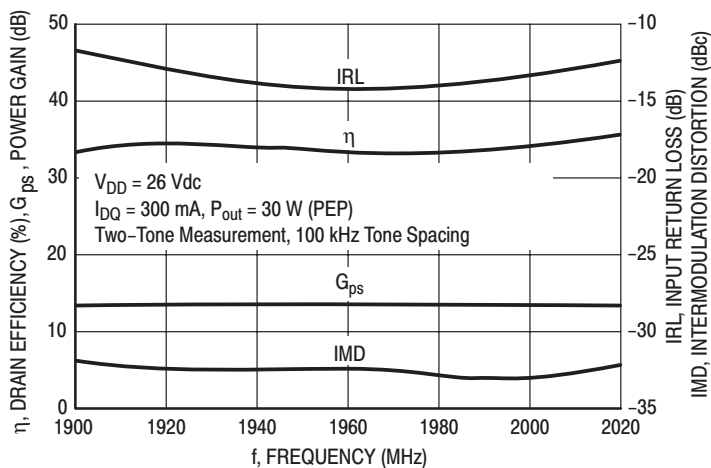


Figure 3. Class AB Broadband Circuit Performance

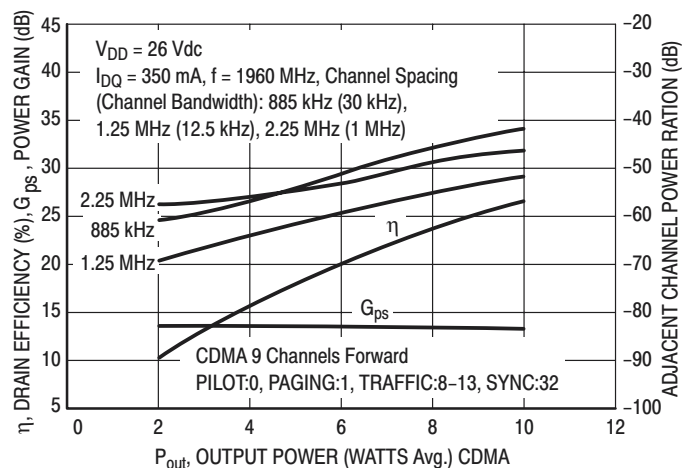


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

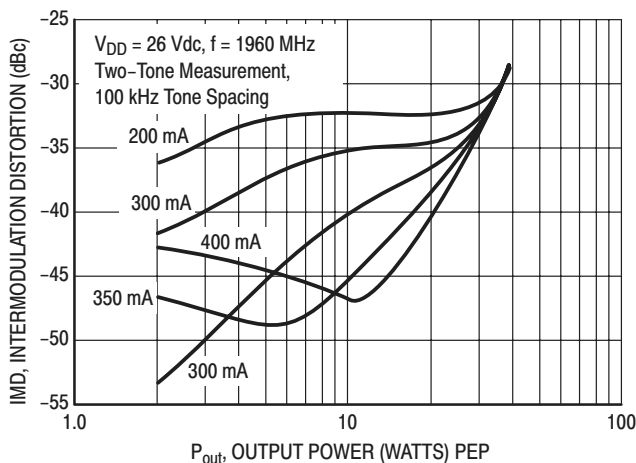


Figure 5. Intermodulation Distortion versus Output Power

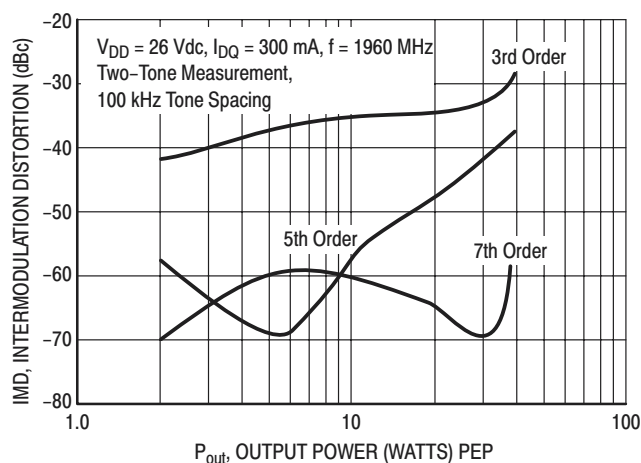


Figure 6. Intermodulation Distortion Products versus Output Power

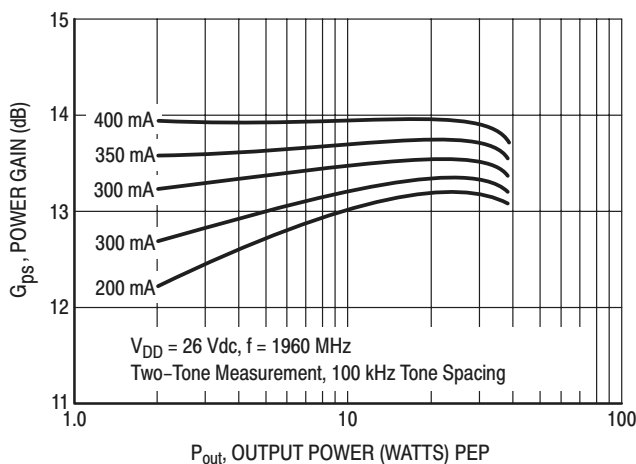


Figure 7. Power Gain versus Output Power

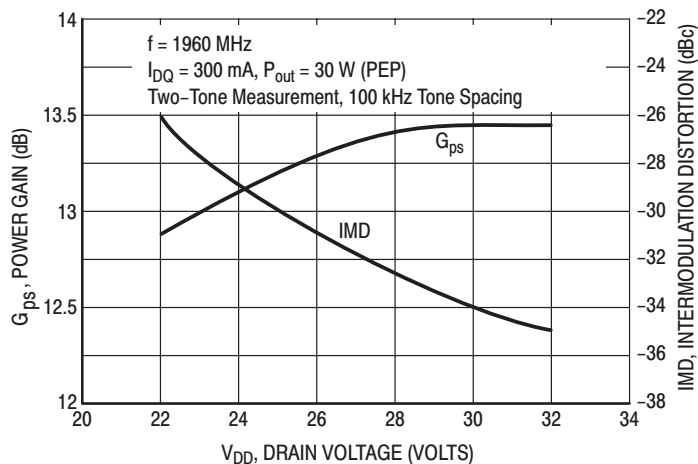
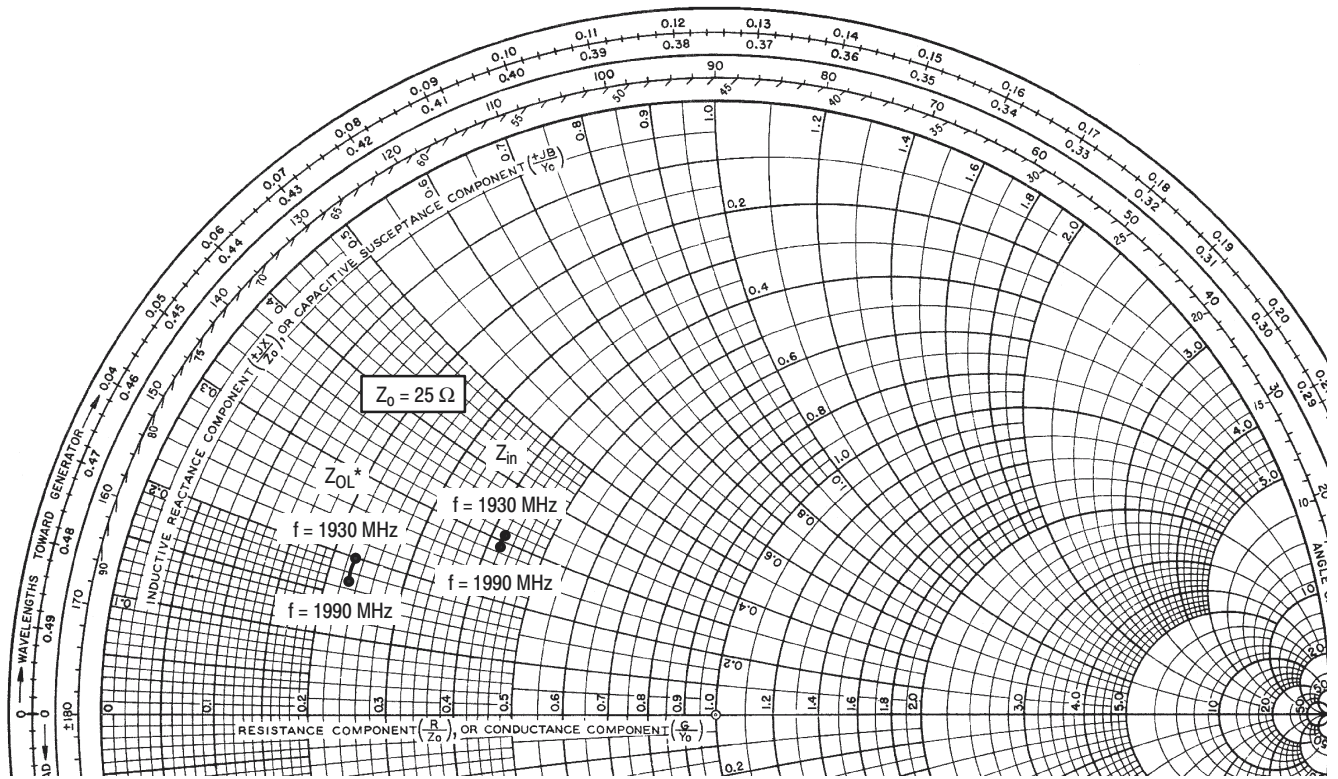


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 26\text{ V}$, $I_{DQ} = 300\text{ mA}$, $P_{out} = 30\text{ W PEP}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	$10.57 + j7.69$	$5.81 + j5.01$
1960	$10.54 + j7.43$	$5.84 + j4.67$
1990	$10.47 + j7.21$	$5.84 + j4.35$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

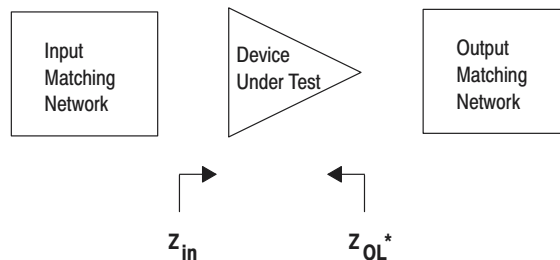
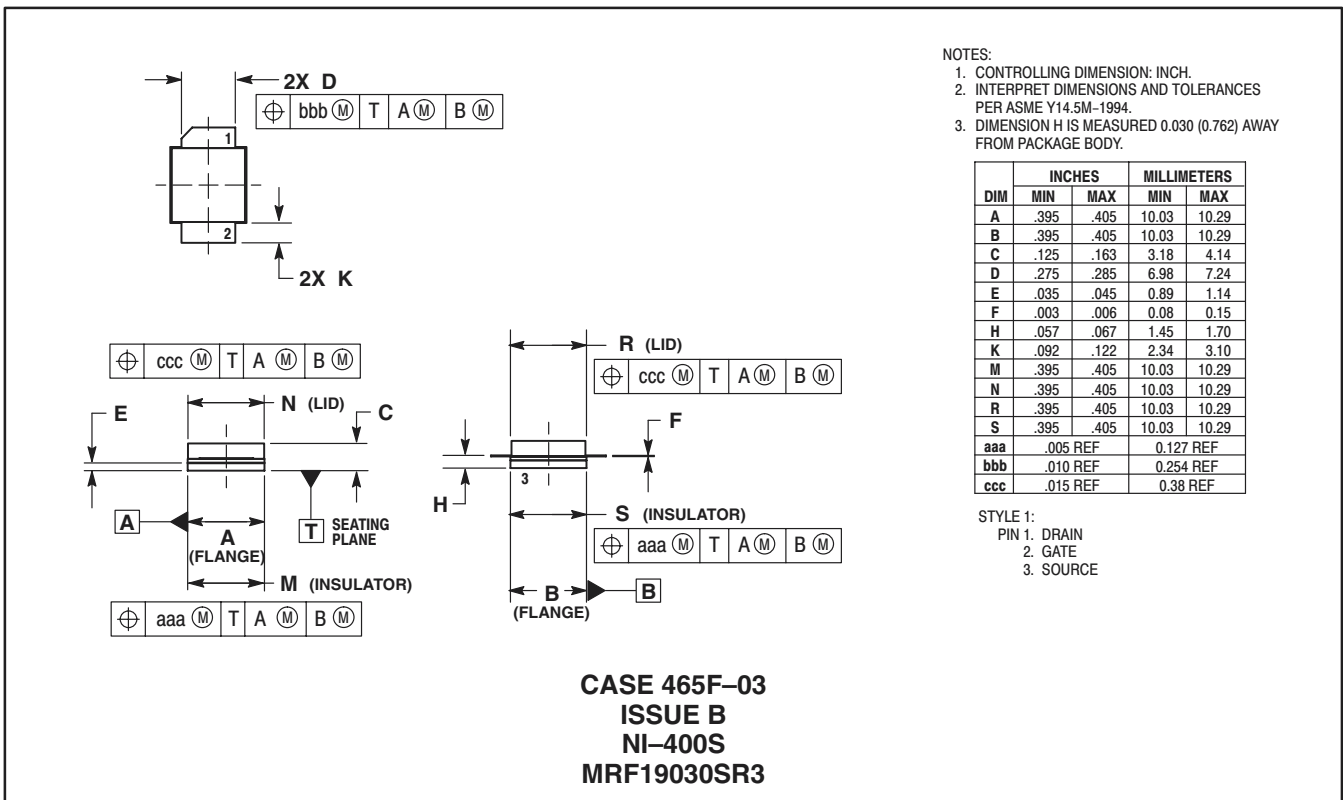
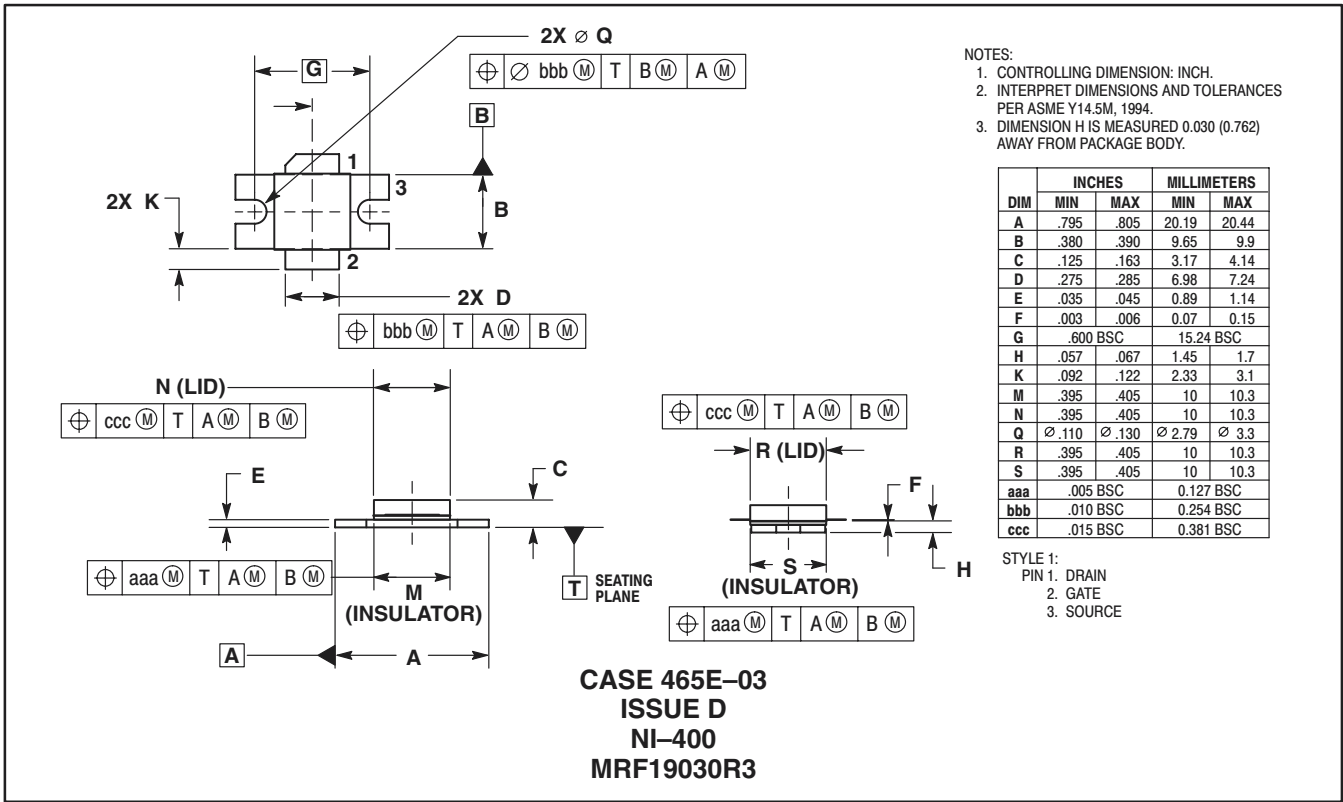



Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS



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