ACS8515 LC/P

Line Card Protection Switch
for SONET or SDH Network Elements

ADVANCED COMMUNCIATIONS **FINAL**

Description

The ACS8515 is a highly integrated, single-chip solution for “hit-less” protection switching of SEC clocks from Master and Slave SETS clockcards in a SONET or SDH Network Element. The ACS8515 has fast activity monitors on the inputs and will implement automatic system protection switching against master clock failure. A further input is provided for an optional standby SEC clock. The ACS8515 is fully compliant with the required specifications and standards.

The ACS8515 can perform frequency translation from a SEC input clock distributed along a back plane to a different local line card clock, e.g. 8 kHz distributed on the back plane and 19.44 MHz generated on the line cards.

An SPI serial port is incorporated, providing access to the configuration and status registers for device setup.

The ACS8515 can utilise either a low cost XO oscillator module, or a TCXO with full temperature calibration - as required by the application.

Features

- Suitable for Stratum 3, 4E and 4 SONET or SDH Equipment Clock (SEC) applications
- Meets AT&T, ITU-T, ETSI and Telcordia specifications
- Three SEC input clocks, from 2 kHz to 155.52 MHz
- Generates two SEC output clocks, up to 311.04 MHz
- Frequency translation of SEC input clock to a different local line card clock
- Robust input clock source frequency and activity monitoring on all inputs
- Supports Free-Run, Locked and Holdover modes of operation
- Automatic “hit-less” source switchover on loss of input
- External force fast switch between SEC inputs
- Phase build-out for output clock phase continuity during input switchover
- SPI compatible serial microprocessor interface
- Programmable wander and jitter tracking/ attenuation 0.1 Hz to 20 Hz
- Single 3.3 v operation. 5 v I/O compatible
- Operating temperature (ambient) -40°C to +85°C
- Available in 64 pin LQFP package

Block Diagram

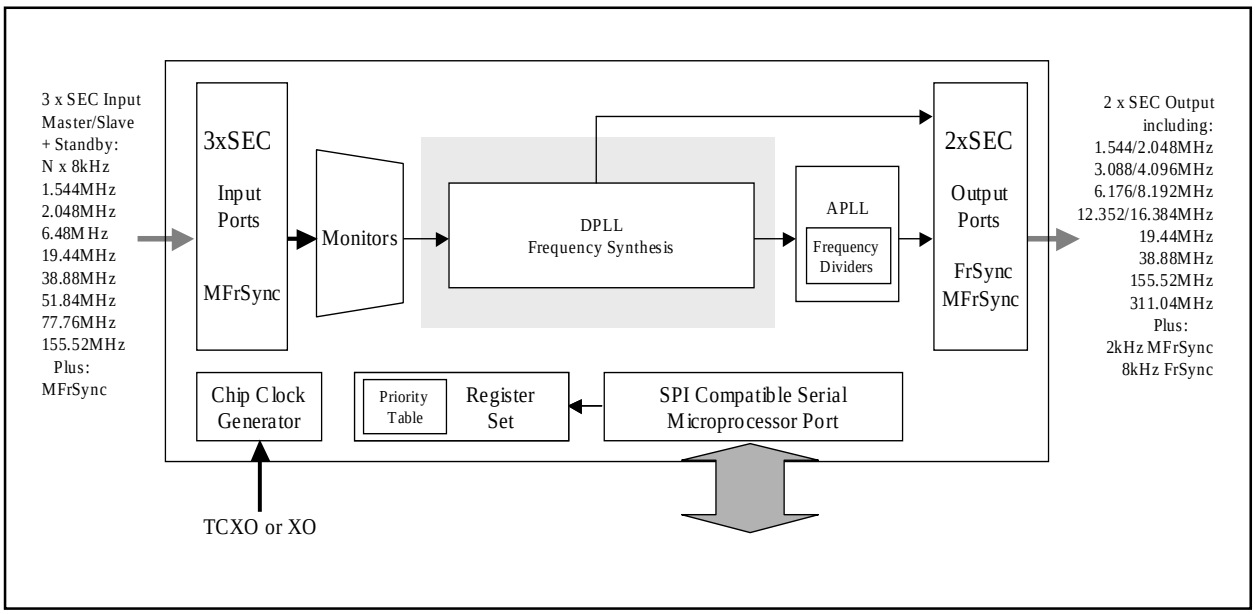
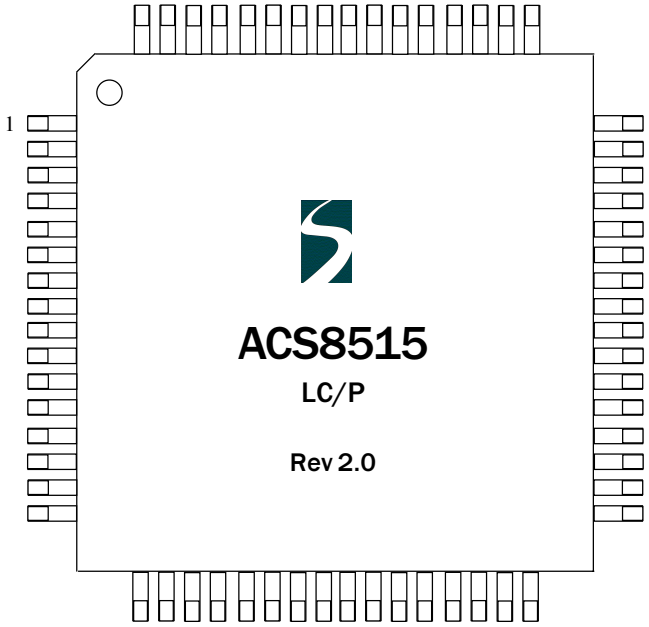


Table of Contents

Pin Diagram

1	AGND	64	SONSDHB
2	IC	63	IC
3	AGND	62	IC
4	VA1+	61	IC
5	INTREQ	60	IC
6	REFCLK	59	NC
7	DGND	58	DGND
8	VD+	57	VDD
9	VD+	56	O2
10	DGND	55	NC
11	DGND	54	VDD
12	VD+	53	DGND
13	SRCSW	52	SDO
14	VA2+	51	IC
15	AGND	50	IC
16	IC	49	IC
17	FrSync	48	PORB
18	MFrSync	47	SCLK
19	O1POS	46	VDD
20	O1NEG	45	VDD
21	GND_DIFF	44	CSB
22	VDD_DIFF	43	SDI
23	SEC1_POS	42	CLKE
24	SEC1_NEG	41	IC
25	SEC2_POS	40	DGND
26	SEC2_NEG	39	VDD
27	VDD5	38	VDD
28	Sync2k	37	IC
29	SEC1	36	VDD
30	SEC2	35	IC
31	DGND	34	SEC3
32	VDD	33	IC



Top view of 64 pin LQFP package.
NC - Not Connected, IC - Internally Connected

Pin Descriptions

Power

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
8, 9, 12	VD+	P	-	Supply voltage: Digital supply to gates in analog section, +3.3 Volts. +/- 10%
22	VDD_DIFF	P	-	Supply voltage: Digital supply for differential output pins 19 & 20, +3.3 Volts. +/- 10%
27	VDD5	P	-	VDD5: Digital supply for +5 Volts tolerance to input pins. Connect to +5 volts (+/- 10%) for clamping to +5 v. Connect to VDD for clamping to +3.3 v. Leave floating for no clamping, input pins tolerant up to +5.5 v.
32, 36, 38, 39, 45, 46, 54, 57	VDD	P	-	Supply voltage: Digital supply to logic, +3.3 Volts. +/- 10%
4	VA1+	P	-	Supply voltage: Analog supply to clock multipying APLL, +3.3 Volts. +/- 10%
14	VA2+	P	-	Supply voltage: Analog supply to output APLL, +3.3 Volts. +/- 10%
7, 10, 11, 31, 40, 53, 58	DGND	P	-	Supply Ground: Digital ground for logic
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential output pins 19 & 20
1, 3, 15	AGND	P	-	Supply Ground: Analog ground

No connections

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
55, 59	NC	-	-	Not Connected: Leave to Float
2, 16, 60, 61, 62, 63	IC	-	-	Internally Connected: Leave to Float
37	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG control reset input on next revision
41	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG test mode select input on next revision
49	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG boundary scan clock input on next revision
50	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG serial test data output on next revision
51	IC	-	-	Internally connected: Leave to Float. Reserved for JTAG serial test data input on next revision

Others

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
5	INTREQ	O	-	Interupt request: Software Interrupt enable
6	REFCLK	I	TTL	Reference clock: 12.8 MHz (refer to section headed Local Oscillator Clock)
13	SRCSW	I	TTL_D	Source switching: Force fast source switching on SEC1 and SEC2
17	FrSync	O	TTL	Output reference: 8 kHz Frame Sync, 50:50 mark/space ratio output
18	MFrSync	O	TTL	Output reference: 2 kHz Multi-Frame Sync, 50:50 mark/space ratio output
19 20	O1POS O1NEG	O	LVDS/ PECL	Output reference: Programmable, default 38.88 MHz LVDS
23 24	SEC1_POS SEC1_NEG	I	LVDS/ PECL	Input reference: Programmable, default 19.44 MHz LVDS
25 26	SEC2_POS SEC2_NEG	I	PECL/ LVDS	Input reference: Programmable, default 19.44 MHz PECL
28	Sync2k	I	TTL_D	Multi-Frame Sync 2 kHz: Multi-Frame Sync input
29	SEC1	I	TTL_D	Input reference: Programmable, default 8 kHz
30	SEC2	I	TTL_D	Input reference: Programmable, default 8 kHz
33	IC	-	-	Internally connected: Connect to GND. Reserved for Slave Multi-frame sync 2 kHz input on next revision.
34	SEC3	I	TTL_D	Input reference: External standby reference clock source, programmable, default 19.44 MHz
35	IC	-	-	Internally connected: Connect to GND. Reserved for external standby 2 kHz Multi-frame sync input on next revision.
42	CLKE	I	TTL_D	SCLK edge select: SCLK active edge select, CLKE=1 selects falling edge of SCLK to be active
43	SDI	I	TTL_D	Microprocessor interface address: Serial data input
44	CSB	I	TTL^U	Chip select (active low): This pin is asserted Low by the microprocessor to enable the microprocessor interface
47	SCLK	I	TTL_D	Address Latch Enable: default Serial data clock. When this pin transitions from high to low, the address bus inputs are latched into the internal registers
48	PORB	I	TTL^U	Power on reset: Master reset. If PORB is forced Low, all internal states are reset back to default values

Note: I = input, O = output, P = power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor

PIN	SYMBOL	IO	TYPE	NAME/DESCRIPTION
52	SDO	O	TTL_D	Microprocessor interface address: Serial data output
56	O2	O	TTL	Output reference: 19.44 MHz fixed
64	SONSDHB	I	TTL_D	SONETSDHB: SONET or SDH frequency select: sets the initial power up state (or state after a PORB) of the SONET/SDH frequency selection registers, addr 34h, bit 2 and addr 38, bit 5. When low SDH rates are selected (2.048 MHz etc) and when set high SONET rates are selected (1.544 MHz etc). The register states can be changed after power up by software

Functional description

The ACS8515 is a highly integrated, single-chip solution for “hit-less” protection switching of SEC clocks from Master and Slave SETS clock cards in a SONET or SDH Network Element. The ACS8515 has fast activity monitors on the inputs and will implement automatic system protection switching for Master/Slave SEC clock failure. The standby SEC clock will be selected if both the Master and Slave input clocks fail. The selection of the Master/Slave input can also be forced by a Force Fast Switch pin.

The ACS8515 can perform frequency translation from a SEC input clock distributed along a back plane to a different local line card - e.g. 8 kHz distributed on the back plane and 19.44 MHz generated on the line cards.

The ACS8515 has three SEC clock inputs (Master, Slave and Standby) and a single Multi-Frame Sync input, for synchronising the frame and multi-frame sync outputs.

The ACS8515 generates two SEC clock outputs via PECL/LVDS and TTL ports, with spot frequencies from 1.544/2.048 MHz up to 311.04 MHz. The ACS8515 also provides an 8 kHz Frame Sync and 2 kHz Multi-Frame Sync output clock.

The ACS8515 has a high tolerance to input jitter and wander. The output jitter and wander are low, where the wander transfer is programmable (0.1 Hz up to 20 Hz cut-off points).

The ACS8515 includes an SPI compatible serial microprocessor port, providing access to the configuration and status registers for device setup.

Local Oscillator Clock

The Master system clock on the ACS8515 should be provided by an external clock oscillator of frequency 12.80 MHz. The exact clock specification is dependent on the quality of Holdover performance required in the application.

In most Line Card protection switching applications where there is a high chance that at least one SEC reference input will be available, the long term stability requirement for Holdover is not appropriate and an inexpensive crystal local oscillator can be used. In other applications where there may be a requirement for longer term Holdover stability to meet the ITU standards for Stratum 3, a higher quality oscillator can be used.

Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less

important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. +/- 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8 bit register locations. The setting of the *conf_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.02 ppm for each LSB step. The default value (in decimal) is 39321. The minimum being 0 and the maximum 65535, gives a +500 ppm to -700 ppm adjustment range of the output frequencies.

For example, if the crystal was oscillating at 12.8 MHz + 5ppm, then the calibration value in the register to give a -5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be : 39321 - (5 / 0.02) = 39071 (decimal).

Input Interfaces

The ACS8515 supports up to three individual input reference clock sources via TTL/CMOS and PECL/LVDS technologies. These interface technologies support 3.3 V and 5 V operation.

Input Reference Clock Ports

The input reference clock ports are arranged in groups. Group one comprises a TTL port (SEC1) and a PECL/LVDS port (SEC1POS and SEC1NEG). Group two comprises a TTL port (SEC2) and a PECL/LVDS port (SEC2POS and SEC2NEG). Group three comprises a TTL port (SEC3). For group one and group two, only one of the two input ports types must be active at any time, the other must not be driven by a reference input. Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other low (GND), or set in LVDS mode and left floating (in which case one input is internally pulled high and the other low).

SDH and SONET networks use different default frequencies; the network type is selectable using the *config_mode* register 34 Hex, bit 2. For SONET, *config_mode* register 34 Hex, bit 2 = 1, for SDH *config_mode* register 34 Hex, bit 2 = 0. On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 64). Specific frequencies and priorities are set by configuration.

The TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. Clock speeds above 100 MHz should not be applied to the TTL ports. The PECL/LVDS ports support the full range of clock speeds, up to 155.52 MHz.

The actual spot frequencies supported are; 8 kHz (and N x 8 kHz), 1.544 MHz/2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, and 155.52 MHz. The frequency selection is programmed via the *cnfg_ref_source_frequency* register. The internal DPLL will normally lock to the selected input at the frequency of the input, eg. 19.44 MHz will lock the DPLL phase comparisons at 19.44 MHz. It is, however, possible to utilise an internal pre-divider to the DPLL to divide the input frequency before it is used for phase comparisons in the DPLL. This pre-divider can be used in one of 2 ways;

(i) any of the supported spot frequencies can be divided to 8 kHz by setting the "lock8K" bit (bit 6) in the appropriate cnfg_ref_source_frequency register location

(ii) any multiple of any supported frequency can be supported by using the "DivN" feature (bit 7 of the cnfg_ref_source_frequency register). Any reference input can be set to lock at 8 kHz independently of the frequencies and configurations of the other inputs.

Any reference input with the "DivN" bit set in the cnfg_ref_source_frequency register will employ the internal pre-divider prior to the DPLL

Port Name	Input Port Technology	Frequencies Supported	SEC Source Group	Default Priority (Note 3)
SEC1	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	1	1 (4)
SEC2	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET): 8kHz Default (SDH): 8kHz	2	3 (5)
SEC1	LVDS/PECL LVDS default	Up to 155.52MHz (Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	1	2 (6)
SEC2	PECL/LVDS PECL default	Up to 155.52MHz (Note 2) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	2	4 (7)
SEC3	TTL/CMOS	Up to 100MHz (Note 1) Default (SONET): 19.44MHz Default (SDH): 19.44MHz	3	5 (10)
SYNC1	TTL/CMOS	2kHz Multi Frame Sync	-	-

Table 1: Input Reference Source Selection and Group allocation

Notes for Table 1.

Note 1. TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are 8 kHz (N x 8 kHz), 1.544/2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz and 77.76 MHz.

Note 2. PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz. There are different output clock frequencies available for SONET and SDH applications. F_1/F_2 means that the output frequency is F_1 for SONET mode selection and F_2 for SDH mode selection.

Note 3. The default priority values in brackets are the default numbers reported in the register map, which match up with the ACS8510.

On power up, or by reset, the default will be set by the SONSDHB pin. Specific frequencies and priorities are set by configuration. For SONET, *config_mode* register 34 Hex, bit 2 = 1. For SDH *config_mode* register 34 Hex, bit 2 = 0.

locking. The cnfg_freq_divn register contains the divider ratio N where the reference input will get divided by (N+1) where $0<N<2^{14}-1$. The cnfg_ref_source_frequency register must be set to the closest supported spot frequency to the input frequency, but must be lower than the input frequency. When using the “DivN” feature the post-divider frequency must be 8 kHz, which is indicated by setting the ‘lock8k’ bit high (bit 6 in cnfg_ref_source_frequency register). Any input set to DivN must have the frequency monitors disabled (if the frequency monitors are disabled, they are disabled for all inputs regardless of the input configurations, in this case only activity monitoring will take place). Whilst any number of inputs can be set to use the “DivN” feature, only one N can be programmed, hence all inputs using the “DivN” feature must require the same division to get to 8 kHz.

PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz. The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register.

Unused PECL/LVDS differential inputs should be fixed with one input high (VDD) and the other input low (GND), or set in LVDS mode and left floating, in which case one input is internally pulled high and the other low.

Input Wander and Jitter Tolerance

The ACS8515 is compliant to the requirements of all relevant standards, principally ITU Recommendation G.825, ANSI T1.101-1994 and ETS 300 462-5 (1997).

All reference clock inputs have a tight frequency tolerance but a generous jitter tolerance. Pull-in, hold-in and pull-out ranges are specified for each input port in Table 2. Minimum jitter tolerance masks are specified in Figures 1 and 2, and Tables 3 and 4, respectively. The ACS8515 will tolerate wander and jitter components greater than those shown in Figure 1 and Figure 2, up to a limit determined by a combination of the apparent long-term frequency offset caused by wander and the eye-closure caused by jitter (the input source will be rejected if the offset pushes the frequency outside the hold-in range for long enough to be detected, whilst the signal will also be rejected if the eye closes sufficiently to affect the signal purity). The '8klocking' mode should be engaged for high jitter tolerance according to these masks.

All reference clock ports are monitored for quality, including frequency offset and general activity. Single short-term interruptions in selected reference clocks may not cause rearrangements, whilst longer interruptions, or multiple, short-term interruptions, will cause rearrangements, as will frequency offsets which are sufficiently large or sufficiently long to cause loss-of-lock in the phase-locked loop. The failed reference source will be removed from the priority table and declared as unserviceable, until its perceived quality has been restored to

Jitter Tolerance	Frequency Monitor Acceptance Range	Frequency Acceptance Range (Pull-in)	Frequency Acceptance Range (Hold-in)	Frequency Acceptance Range (Pull-out)
G.703	+/- 16.6 ppm	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)	+/- 4.6 ppm (see Note 1) +/- 9.2 ppm (see Note 2)
G.783				
G.823				
GR-1244-CORE				

Table 2: Input Reference Source Jitter Tolerance.

Notes for Table 2.

Note 1. The frequency acceptance and generation range will be +/-4.6 ppm around the required frequency when the external crystal frequency accuracy is within a tolerance of +/- 4.6 ppm.

Note 2. The fundamental acceptance range and generation range is +/- 9.2 ppm with an exact external crystal frequency of 12.8 MHz.

Note 3. The power up default PDLL range is as stated in note 2, but the range is also programmable from 0 to 80 ppm in 0.08 ppm steps.

an acceptable level.

The registers reg sts_curr_inc_offset (address 0C, 0D, 07) report the frequency of the DPLL with respect to the external TCXO frequency. This is a 19 bit signed number with one LSB representing 0.0003 ppm (range of +/- 80 ppm). Reading this regularly can show how the currently locked source is varying in value e.g. due to wander on its input.

The ACS8515 performs automatic frequency monitoring with an acceptable input frequency offset range of +/- 16.6 ppm. The ACS8515 DPLL has a programmable frequency limit of +/- 80 ppm. If the range is programmed to be > 16.6 ppm, the activity monitors should be disabled so the input reference source is not automatically rejected as out of frequency range.

Output Clock Ports

The ACS8515 supports two SEC output clocks on both TTL and PECL/LVDS ports and a pair of secondary output clocks, 'Frame-Sync' and 'Multi-Frame-Sync'. The two output clocks are individually controllable. The 'Frame-Sync' and 'Multi-Frame-Sync' are derived from the main SEC clock. The frequencies of the output clock are selectable from a range of pre-defined spot frequencies, and a variety of output technologies are supported, as defined in Table 5.

Figure 1: Minimum Input Jitter Tolerance for inputs supporting G.783 compliant sources

STM level	Peak to peak amplitude (unit Interval)					Frequency (Hz)									
	A0	A1	A2	A3	A4	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9
STM-1	2800	311	39	1.5	0.15	12u	178u	1.6m	15.6m	0.125	19.3	500	6.5k	65k	1.3m

Table 3: Amplitude and Frequency values for Jitter Tolerance for inputs supporting G.783 compliant sources

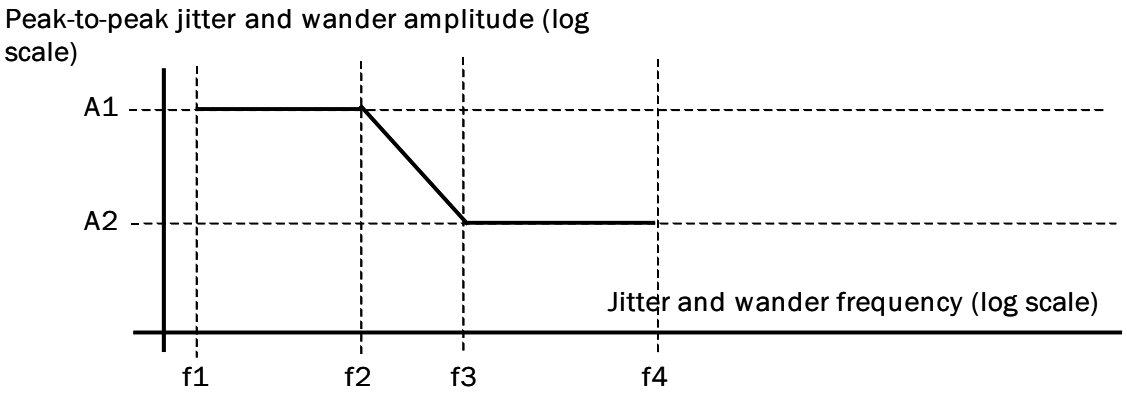


Figure 2: Minimum Input Jitter Tolerance for inputs supporting G.703 compliant sources

Type	Spec.	Amplitude (UI pk-pk)		Frequency (Hz)			
		A1	A2	F1	F2	F3	F4
DS1	GR-1244-CORE	5	0.1	10	500	8k	40k
E1	ITU G.823	1.5	0.2	20	2.4k	18k	100k

Table 4: Amplitude and Frequency values for Jitter Tolerance for inputs supporting G.703 compliant sources

Low-speed Output Clock

The O2 SEC clock is supplied on a TTL port with a fixed frequency of 19.44 MHz.

High-speed Output Clock

The O1 SEC clock is supplied on a PECL/LVDS port with spot frequencies of 19.44 MHz, 38.88 MHz, 155.52 MHz, 311.04 MHz and Dig 1 (where Dig 1 is 1.544/2.048 MHz and multiples of 2, 4 and 8 depending on SONET/SDH mode setting). The actual frequency is selectable via the *cnfg_differential_outputs* register. The O1 port can also support 311.04 MHz, which is enabled via the *cnfg_T0_output_enable* register. The O1 port can be made LVDS or PECL compatible via the *cnfg_differential_outputs* register.

Frame Sync and Multi-Frame Sync Clocks

Frame Sync (8 kHz) and Multi-Frame Sync (2 kHz) clocks will be provided on outputs FrSync and MFrSync. The FrSync and MFrSync clocks have a 50:50 mark space ratio.

Output Wander and Jitter

Wander and jitter present on the output clocks are dependent on:

The magnitude of wander and jitter on the selected input reference clock (in locked mode);

The internal wander and jitter transfer characteristic (in locked mode);

The jitter on the local oscillator clock;

The wander on the local oscillator clock (in Hold-Over mode).

Wander and jitter are treated in different ways to reflect their differing impacts on network design. Jitter is always strongly attenuated, whilst wander attenuation can be varied to suit the application and operating state. Wander and jitter attenuation is performed by using a digital phase locked loop (DPLL) with a programmable bandwidth. This gives a transfer characteristic of a low pass filter, with a programmable pole. It is sometimes necessary to change the filter dynamics to suit particular circumstances - one example being when locking to a new source, the filter can be opened up to reduce locking time and can then be gradually tightened again to remove wander. Since wander represents a relatively long-term deviation from the nominal operating frequency, it affects the rate of supply of data to the network element. Strong wander attenuation limits the rate of consumption of data to within a smaller range, so a larger buffer store is required to prevent data loss. But, since any buffer store potentially increases latency, wander may often only need to be removed at specific points within a network where buffer stores are acceptable, such as at digital cross connects. Otherwise, wander is sometimes not required to be attenuated and can be passed through transparently. The ACS8515 has programmable wander transfer characteristics in a range from 0.1 Hz to 20 Hz. The wander and jitter transfer characteristic is shown in Figure 3.

Wander on the local oscillator clock will not have significant effect on the output clock whilst in locked mode, so long as the DPLL bandwidth is set high enough so that the DPLL can compensate quickly enough for any frequency changes in the crystal. In free-running or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator, as specified in the section 'Local Oscillator Clock'.

Port Name	Output Port Technology	Frequencies Supported (Note 1)
O1	LVDS/PECL LVDS default	19.44 MHz, 38.88 MHz (default), 155.52 MHz, 311.04 MHz, Dig1 Dig1 is 1.544 MHz/2.048 MHz and multiples of 2, 4 and 8
O2	TTL/CMOS	19.44MHz fixed
FrSync	TTL/CMOS	FrSync, 8kHz. 50:50 mark/space ratio
MFrSync	TTL/CMOS	MFrSync, 2kHz. 50:50 mark/space ratio

Table 5: Output Reference Source Selection table

Notes for Table 5.

Note 1. There are different output clock frequencies available for SONET and SDH applications. Dig 1 can be configured for either frequency F_1/F_2, where the output frequency is F_1 when the SONET mode is selected, and F_2 when the SDH mode is selected.

On power up, or by reset, the default will be set by the SONSDHB pin. Specific frequencies and priorities are set by configuration. For SONET, *config_mode* register 34 Hex, bit 2 = 1. For SDH *config_mode* register 34 Hex, bit 2 = 0.

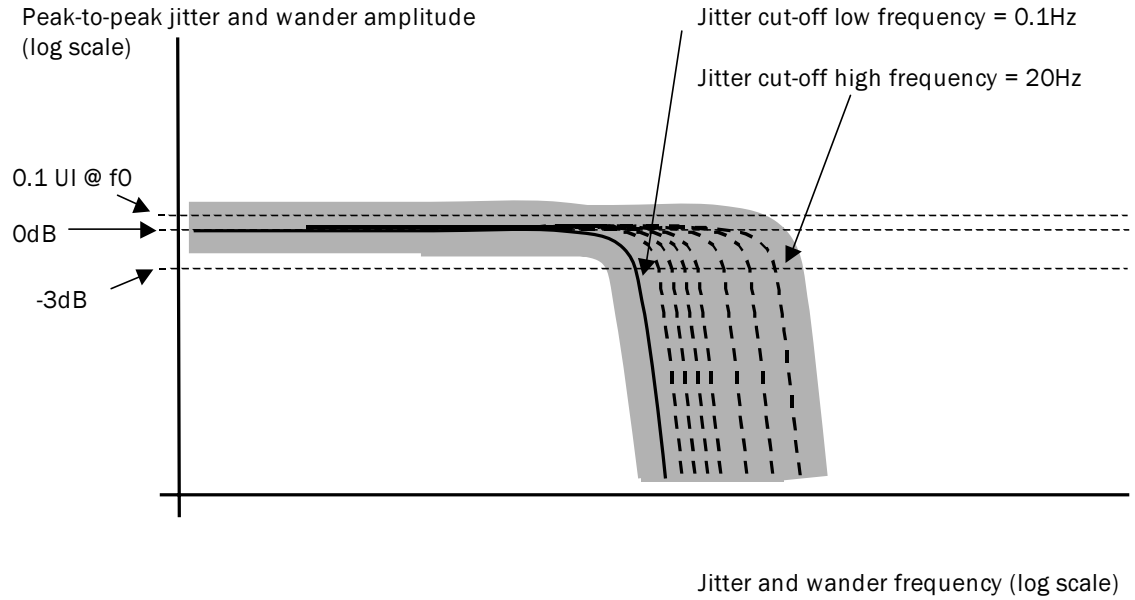


Figure 3: Wander and Jitter Transfer Characteristsics

Phase Variation

There will be a phase shift across the ACS8515 between the selected input reference source and the output clock. This phase shift may vary over time but will be constrained to lie within specified limits. The phase shift is characterised using two parameters, MTIE (Maximum Time Interval Error), and TDEV (Time Deviation), which, although being specified in all relevent specifications, differ in acceptable limits in each one. Typical measurements for the ACS8515 are shown in Figures 4 and 5, for locked mode operation. Figure 6 shows a typical measurement of Phase Error accumulation in Holdover mode operation.

The required performance for phase variation during Holdover is specified in several ways depending upon the particular circumstances pertaining:

1. ETSI 300 462-5, Section 9.1, requires that the short-term phase error during switchover (i.e., Locked to Holdover to Locked) be limited to an accumulation rate no greater than 0.05 ppm during a 15 second interval.

2. ETSI 300 462-5, Section 9.2, requires that the long-term phase error in the Holdover mode should not exceed $\{(a1+a2)S+0.5bS^2+c\}$, where

a1 = 50 ns/s (allowance for initial frequency offset)

a2 = 2000 ns/s (allowance for temperature variation)

b = 1.16×10^{-4} ns/s^2 (allowance for ageing)

c = 120 ns (allowance for entry into Holdover mode).

3. ANSI Tin1.101-1994, Section 8.2.2, requires that the phase variation be limited so that no more than 255 slips (of 125 µs each) occur during the first day of Holdover. This requires a frequency accuracy better than:

((24x60x60)+(255x125µs))/(24x60x60) = 0.37 ppm.

Temperature variation is not restricted, except to within the normal bounds of 0 to 50 Celsius.

4. Bellcore GR.1244.CORE, Section 5.2. Table 4. shows that an initial frequency offset of 50 ppb is permitted on entering Holdover, whilst a drift over temperature of 280 ppb is allowed; an allowance of 40 ppb is permitted for all other effects.

5. ITU G.822, Section 2.6, requires that the slip rate

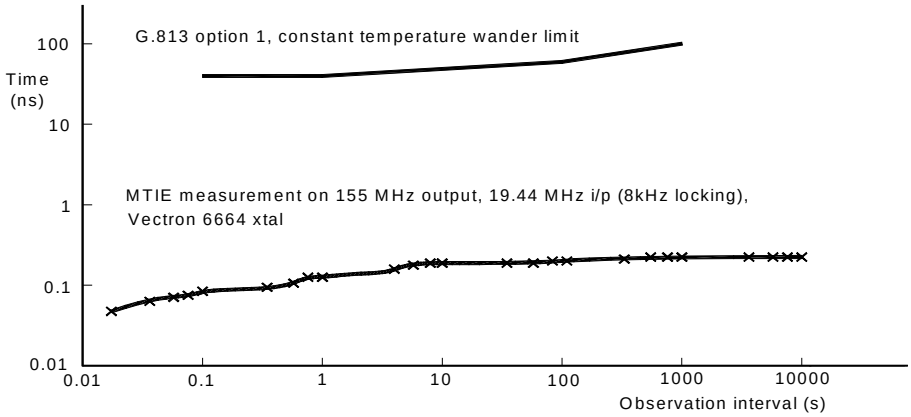


Figure 4: Maximum Time Interval Error of T_{OUT0} output port

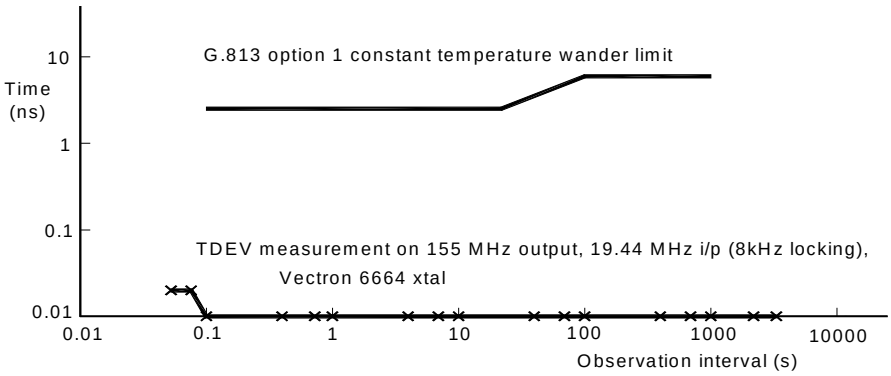


Figure 5: Time Deviation of T_{OUT0} output port

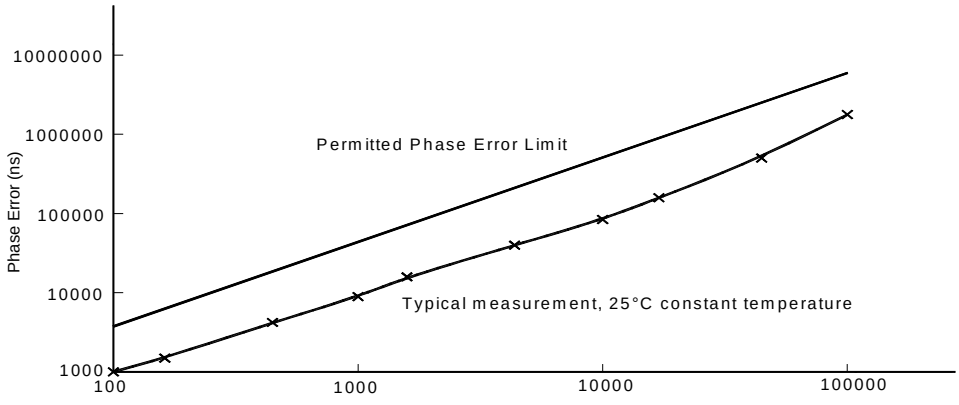


Figure 6: Phase error accumulation of T_{OUT0} output port in Holdover mode

during category(b) operation (interpreted as being applicable to Holdover mode operation) be limited to less than 30 slips (of 125 µs each) per hour

((((60 x 60)/30)+125µs)/(60x60)) = 1.042 ppm.

Phase Build Out

Phase Transient response and Holdover

Phase Build Out (PBO) is the function to minimise phase transients on the output SEC clock during input reference switching or mode switching. If the currently selected input reference clock source is lost (due to a short interruption, out of frequency detection, or complete loss of reference), the second, next highest priority reference source will be selected. During this transition, the Lost_Phase mode is entered.

The typical phase disturbance on clock reference source switching will be less than 10 ns on the ACS8515. For clock reference switching caused by the main input failing or being disconnected, then the phase disturbance on the output will still be less than the 120 ns allowed for in the G.813 spec. The actual value is dependant on the frequency being locked to.

The PBO requirement, as specified in Telcordia GR1244-CORE, Section 5.7, in that a phase transient of greater than 3.5 µs occuring in less than 0.1 seconds should be absorbed, will be implemented on a future version. ITU-T G.813 states that the max allowable short term phase transient response, resulting from a switch from one clock source to another, with Holdover mode entered in between, should be a maximum of 1 µs over a 15 second interval. The maximum phase transient or jump should be less than 120 ns at a rate of change of less than 7.5 ppm and the Holdover performance should be better than 0.05 ppm.

On the ACS8515, PBO can be enabled, disabled or frozen using the µP interface. By default, it is enabled. When PBO is enabled, it can also be frozen, which will disable the PBO operation on the next input reference switch, but will remain with the current offset. If PBO is disabled while the device is in the Locked mode, there will be a phase jump on the output SEC clocks as the DPLL locks back to 0 degree phase error.

Micro-Processor Interface

The ACS8515 incorporates a serial microprocessor interface that is compatible with the Serial Peripheral Interface (SPI) for device setup.

Register Set

All registers are 8-bits wide, organised with the most-significant bit positioned in the left-most bit, with bit-significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g., flags) upwards. Several data fields are spread across multiple registers; their organisation is shown in the register map.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the Chip_revision register. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the 'sts_interrupts' register), any individual data field may be cleared by writing a "1" into each bit of the field (writing a "0" value into a bit will not affect the value of the bit). Details of each register are given in the Register Map and Register Description sections.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ (active High).

Bits in the interrupt status register are set (high) by the following conditions;

(i) any reference source becoming valid or going invalid

(ii) a change in the operating state (eg. Locked, Holdover etc.)

(iii) brief loss of the currently selected reference source

All interrupt sources are maskable via the mask register (cnfg_interrupt_mask), each one being enabled by writing a '1' to the appropriate bit.

Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted (high).

All interrupts are cleared by writing a '1' to the bit(s) to be cleared in the status register.

When all pending unmasked interrupts are cleared the interrupt pin will go inactive (low).

The loss of the currently selected reference source will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the leaky bucket configuration of the activity monitors. The very fastest leaky bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected reference source is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the reference source. Some applications require the facility to switch downstream devices based on the status of the reference sources. In order to provide extra flexibility, it is possible to flag the "main reference failed" interrupt (addr 06, bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to bit 6 of register 48Hex.

Register map

Shaded areas in the map are ‘don’t care’ and writing either 0 or 1 will not affect any function of the device.

Bits labelled ‘Set to 0’ or ‘Set to 1’ must be set as stated during initialisation of the device, either following power up, or after a power on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

Some registers do not appear in this list, for example 07 and 08. These are either not used, or have test functionality. Do not write to any undefined registers as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
02	chip_revision (read only)	Chip revision number (7:0)							
03	cnfg_control1 (read/write)			Set to '0'	Analog div sync	Set to '0'	Set to '0'	Set to '0'	Set to '0'
04	cnfg_control2 (read/write)			Phase loss flag limit			Set to '0'	Set to '1'	Set to '0'
05	sts_interrupts (read/write)			SEC2DIFF	SEC1DIFF	SEC2	SEC1		
06		Operating mode	Main ref failed						SEC3
09	sts_operating_mode (read only)						Operating mode (2:0)		
0A	sts_priority_table (read only)	Highest priority valid source				Currently selected reference source			
0B		3rd highest priority valid source				2nd highest priority valid source			
0C	sts_curr_inc_offset (read only)	Current increment offset (7:0)							
0D		Current increment offset (15:8)							
07							Current increment offset (18:16)		
0E	sts_sources_valid (read only)			SEC2DIFF	SEC1DIFF	SEC2	SEC1		
0F									SEC3
11	sts_reference_sources (read/write)	status <SEC2>				status <SEC1>			
12		status <SEC2DIFF>				status <SEC1 DIFF>			
14						status <SEC3>			

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
18	cnfg_ref_selection_priority (read/write)	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
19		programmed _priority <SEC2>				programmed _priority <SEC1>			
1A		programmed _priority <SEC2DIFF>				programmed _priority <SEC1DIFF>			
1B		Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
1C		Set to '0'	Set to '0'	Set to '0'	Set to '0'	programmed _priority <SEC3>			
1D		Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
1E		Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
22	cnfg_ref_source_frequency (read/write)	divn	lock8k	bucket_id <SEC1> (1:0)		reference_source_frequency <SEC1> (3:0)			
23		divn	lock8k	bucket_id <SEC2> (1:0)		reference_source_frequency <SEC2> (3:0)			
24		divn	lock8k	bucket_id <SEC1DIFF> (1:0)		reference_source_frequency <SEC1DIFF> (3:0)			
25		divn	lock8k	bucket_id <SEC2DIFF> (1:0)		reference_source_frequency <SEC2DIFF> (3:0)			
28		divn	lock8k	bucket_id <SEC3> (1:0)		reference_source_frequency <SEC3> (3:0)			
32	cnfg_operating_mode (read/write)						Forced operating mode		
33	cnfg_ref_selection (read/write)					force_select_reference_source			
34	cnfg_mode (read/write)	Auto external 2k enable	Phase alarm timeout enable	Clock edge	Holdover offset enable	External 2k Sync enable	SONET/ SDH I/P		reversion mode
35	cnfg_control3 (read/write)			Set to '0'	Set to '0'				
36	cnfg_differential_inputs (read/write)							SEC2DIFF PECL	SEC1DIFF PECL
38	cnfg_output_enable (read/write)	311.04 MHz on O1		1=SONET 0=SDH for Dig1	Set to '0'	Set to '0'	O2	Set to '0'	Set to '0'
39	cnfg_O1_output_frequencies (read/write)			Digital 1					
3A	cnfg_differential_output (read/write)			O1 frequency selection		Set to '0'	Set to '0'	O1 LVDS enable	O1 PECL enable
3B	cnfg_bandwidth (read/write)	Auto b/w switch acq/lock	Acquistion bandwidth			Set to '0'	Normal/locked bandwidth		
3C	cnfg_nominal_frequency (read/write)	Nominal frequency (7:0)							
3D		Nominal frequency (15:8)							

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
3E	cnfg_holdover_offset (read/write)	Holdover offset (7:0)							
3F		Holdover offset (15:8)							
40		Auto Holdover Averaging					Holdover offset (18:16)		
41	cnfg_freq_limit (read/write)	DPLL Frequency offset limit (7:0)							
42								DPLL Frequency offset limit (9:8)	
43	cnfg_interrupt_mask (read/write)	Set to '0'	Set to '0'	status SEC2DIFF	status SEC1DIFF	status SEC2	status SEC1	Set to '0'	Set to '0'
44		Oper. mode	Main ref	Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'	status SEC3
45					Set to '0'	Set to '0'	Set to '0'	Set to '0'	Set to '0'
46	cnfg_freq_divn (read/write)	Divide-input-by-n ratio (7:0)							
47				Divide-input-by-n ratio (13:8)					
48	cnfg_monitors (read/write)		Flag ref lost on TDO	Ultra-fast switching	External source switch enable	Freeze phase buildout	Phase buildout enable	Frequency monitors configuration (1:0)	
50	cnfg_activ_upper_threshold 0 (read/write)	Configuration 0: Activity alarm set threshold (7:0)							
51	cnfg_activ_lower_threshold 0 (read/write)	Configuration 0: Activity alarm reset threshold (7:0)							
52	cnfg_bucket_size 0 (read/write)	Configuration 0: Activity alarm bucket size (7:0)							
53	cnfg_decay_rate 0 (read/write)							Configuration 0: decay_rate (1:0)	
54	cnfg_activ_upper_threshold 1 (read/write)	Configuration 1: Activity alarm set threshold (7:0)							
55	cnfg_activ_lower_threshold 1 (read/write)	Configuration 1: Activity alarm reset threshold (7:0)							
56	cnfg_bucket_size 1 (read/write)	Configuration 1: Activity alarm bucket size (7:0)							
57	cnfg_decay_rate 1 (read/write)							Configuration 1: decay_rate (1:0)	
58	cnfg_activ_upper_threshold 2 (read/write)	Configuration 2: Activity alarm set threshold (7:0)							
59	cnfg_activ_lower_threshold 2 (read/write)	Configuration 2: Activity alarm reset threshold (7:0)							

Addr. (Hex)	Parameter Name	Data Bit							
		7 (msb)	6	5	4	3	2	1	0 (lsb)
5A	cnfg_bucket_size 2 (read/write)	Configuration 2: Activity alarm bucket size (7:0)							
5B	cnfg_decay_rate 2 (read/write)							Configuration 2: decay_rate (1:0)	
5C	cnfg_activ_upper_threshold 3 (read/write)	Configuration 3: Activity alarm set threshold (7:0)							
5D	cnfg_activ_lower_threshold 3 (read/write)	Configuration 3: Activity alarm reset threshold (7:0)							
5E	cnfg_bucket_size 3 (read/write)	Configuration 3: Activity alarm bucket size (7:0)							
5F	cnfg_decay_rate 3 (read/write)							Configuration 3: decay_rate (1:0)	

Register map description

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
02	chip_revision	This read only register contains the chip revision number	00000001
03	cnfg_control1	Bits (3:0) & 5 are test controls and must be either set at '0' during initialisation or left unchanged. Bit 4, when set high, synchronises the dividers in the output APLL section to the dividers in the DPLL section such that their phases align. This is necessary to have the phase alignment between the inputs and output clocks at OC3 derived rates (6.48 MHz to 77.76 MHz). By default, synchronisation occurs for 2 seconds after power up and is then turned off. Setting this bit high keeps synchronisation on, which may be necessary to avoid the dividers getting out of sync when quick changes in frequency occur such as a force into freerun mode.	XX000000
04	cnfg_control2	Bits (2:0) are test controls and must be set at '010' during initialisation or left unchanged. Bits (5:3) define the phase loss flag limit. By default set to 4 (100) which corresponds to approximately 140°. A lower value sets a corresponding lower phase limit. The flag limit determines the value at which the DPLL indicates phase lost as a result of input jitter, a phase jump, or a frequency jump on the input	XX100010
	sts_interrupts	This 16 bit register contains one bit for each bit of sts_sources_valid, one for loss of reference the device was locked to, and another for the operating mode. All bits are active high. All bits except the 'main ref failed' bit (bit 14) are set on a "change" in the state of the relevent status bit, i.e. if a source becomes valid, or goes invalid it will trigger an interrupt. If the Operating Mode (register 9) changes state the interrupt will be generated. Bit 14 (main ref failed) of the interrupt status register is used to flag inactivity on the reference that the device is locked to much more quickly than the activity monitors can support. If bit 6 of the cnfg_monitors register (register 48) (flag ref loss on TDO) is set, then the state of this bit is driven onto the TDO pin of the device. All bits are maskable by the bits in the cnfg_interrupt_mask register. Each bit may be cleared individually by writing a '1' to that bit, thus resetting the interrupt. Any number of bits can be cleared with a single write operation. Writing '0's will have no effect.	
05		Bits (7:6) unused Least significant byte (5:2) Bits (1:0) unused.	XX0000XX
06		Most significant byte (7:6) and 0 Bits (5:1) unused	00XXXXX0

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
09	sts_operating_mode	This read-only register holds the current operating state of the main state machine. Figure 7 show how the values of the 'operating state' variable match with the individual states. Bit Content 2:0 Operating state (2:0) Bits (2:0) State 001 freerun 010 holdover 100 locked 110 pre-locked 101 pre-locked2 111 phase lost 3:7 unused	XXXXX001
	sts_priority_table	This is a 16-bit read-only register, taking two addresses. Currently-selected reference source: this is the channel number of the input reference source which is currently connected to the SETG function. Highest-priority valid source: this is the channel number of the input reference source which is valid and has the highest priority; it may not be the same as the currently-selected reference source (due to failure history or changes in programmed priority). Second-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the highest-priority valid source. Third-highest priority valid source: this is the channel number of the input reference source which is valid and has the next-highest priority to the second-highest-priority valid source. Note that these registers are updated by the state machine in response to the contents of the cnfg_ref_selection_priority register and the ongoing status of individual channels; channel number '0000', appearing in any of these registers, indicates that no channel is available for that priority. Bit Content	
0A		(7:4) Highest-priority valid source (3:0) Currently selected reference source	00000000
0B		(7:4) 3rd-highest-priority valid source (3:0) 2nd-highest-priority valid source	00000000
	sts_curr_inc_offset	This read-only register contains a signed-integer value representing the 19 significant bits of the current increment offset of the digital PLL. The register may be read periodically to build up a historical database for later use during holdover periods (this would only be necessary if an external oscillator which did not meet the stability criteria described in Local Oscillator Clock section is used). The register will read 00000000 immediately after reset.	
0C		Least significant byte of offset value	00000000
0D		Next significant byte of offset value	00000000
07		Bits (2:0) 3 most significant bits of offset value, bits (7:4) unused	XXXXX000
0E	sts_sources_valid	This 8 bit register contains copies of bit 3 from all the status_reference_sources bytes. This allows the user to get the 'validity' of all sources in just 2 reads.	00000000
0F		This register only indicates whether or not a source has passed all criteria.	XX000000
	sts_reference_sources	This is a 5-byte register which holds the status of each of the 8 input reference sources. The status of each reference source is shown in a 4-bit field. Each bit is active high.To aid status checking, a copy of each status bit 3 is provided in the sts_sources_valid register. The status is reported as follows: (Each bit may be cleared individually) Status bit 0 = phase lock alarm Status bit 1 = no activity alarm Status bit 2 = out-of-band alarm Status bit 3 = Source valid (no alarms) (bit 3 is combination of bits 0-2)	
11		(3:0) Status of input reference source SEC1 (7:4) Status of input reference source SEC2	01100110
12		(3:0) Status of input reference source SEC1DIFF (7:4) Status of input reference source SEC2DIFF	01100110

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
14	sts_reference_sources	(3:0) Status of input reference source SEC3 (7:4) Unused	XXXX0110
	cnfg_ref_selection_priority	This is a 7-byte register which holds the priority of each of the 3 input reference sources. The priority values are all relative to each other, with lower-valued numbers taking higher priorities. Only the values 1 to 15(dec) are valid - '0' disables the reference source. Each reference source must be given a unique priority. It is recommended to reserve the priority value '1' as this is used when forcing reference selection via the cnfg_ref_selection register. If the user does not intend to use the cnfg_ref_selection register then priority value '1' need not be reserved. Bit Content	
18		(7:0) Must be set to 00000000 during initialisation	00110010
19		(3:0) Programmed priority of input reference source SEC1 (7:4) Programmed priority of input reference source SEC2	01010100
1A		(3:0) Programmed priority of input reference source SEC1DIFF (7:4) Programmed priority of input reference source SEC2DIFF	01110110
1B		(7:0) Must be set to 00000000 during initialisation	10011000
1C		(3:0) Programmed priority of input reference source SEC3 (7:4) Must be set to 0000 during initialisation	10111010
1D		(7:0) Must be set to 00000000 during initialisation	11010001
1E		(7:0) Must be set to 00000000 during initialisation	11111110
	cnfg_ref_source_frequency	This is a 5-byte register which holds the keys to the frequencies of each of the 5 input reference sources, as listed below. Bits (3:0) define the frequency of the reference source in accordance with the following key: Value (3:0) Frequency 0000 8 kHz 0001 1544 kHz(SONET)/2048 kHz(SDH) (As defined by Register 34, bit 2) 0010 6.48 MHz 0011 19.44 MHz 0100 25.92 MHz 0101 38.88 MHz 0110 51.84 MHz 0111 77.76 MHz 1000 155.52 MHz 1001 2 kHz 1010 4 kHz Bits (5:4) together define which leaky bucket settings (0-3) are used, as defined in registers 50 (hex)to 5F (hex). Bits (7:6) of each byte define the operation undertaken on the input frequency, in accordance with the following key: 00 The input frequency is fed directly into the DPLL 01 The input frequency is internally divided down to 8 kHz, before being fed into the DPLL. This gives excellent jitter tolerance. 10 Unsupported configuration - do not use 11 Uses the division coefficient stored in register cnfg_freq_divn to divide the input by this value prior to going to the DPLL. The frequency monitors must be disabled. The divided down frequency should equal 8 kHz. The frequency (3:0) should be set to the nearest spot frequency just below the actual input frequency. The DivN feature works for input frequencies between 1.544 MHz and 100 MHz.	
22		Frequency of reference source SEC1	00000000
23		Frequency of reference source SEC2	00000000
24		Frequency of reference source SEC1DIFF	00000011
25		Frequency of reference source SEC2DIFF	00000011
28		Frequency of reference source SEC3	00000011
32	cnfg_operating_mode	This 3-bit register is used to force the device into a desired operating state, represented by the binary values shown in Figure 8. Value 0 (hex) allows the control state machine to operate automatically. Bit Reference source (2:0) Desired operating state (as per Figure 8) (7:3) Unused	XXXXX000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
33	cnfg_ref_selection	This 4-bit register occupies the entire 8-bit space at address 33(hex). It is used to force the device to select a particular input reference source, irrespective of its priority. Writing to this register temporarily raises the selected input to priority '1'. Provided no other input is already programmed with priority '1', and revertive mode is on, this source will be selected, if it has been validated by the frequency and activity monitors. Bit (3:0) define the source that is selected in accordance with the following key. Bits (7:4) are unused. Writing X0(hex) or XF(hex) will disable all input reference sources. * The default is XF. Value (3:0) Selected source 0011 SEC1 0100 SEC2 0101 SEC1DIFF 0110 SEC2DIFF 1001 SEC3	XXXX1111*
34	cnfg_mode	This 6-bit register occupies the address 34(hex). It contains several individual configuration fields, as detailed below: Bit 0 = 0 Non-revertive Mode: The device will retain the presently selected source. This is the default state. = 1 Revertive Mode: The device will switch to the highest priority source shown in sts_priority_table register(7:4) (at address 0A(hex)). Bits 1 is unused. Bit 2 =0 SDH mode: The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 2048 kHz. This bit is writeable. =1 SONET mode: The device expects the input frequency of any input channel given the value '0001' in the cnfg_ref_source_frequency register to be 1544 kHz. This bit is writeable. Bit 3 =0 External 2 kHz Sync Disable. The device will ignore the Sync2k pin. =1 External 2 kHz Sync Enable. The device will align the phase of its internally generated Frame Sync signal (8 kHz) and Multi-Frame Sync signal (2 kHz) with that of the signal supplied to the Sync2k pin. The device should be locked to a 6.48 MHz output from an ACS8510. This is the default state. Bit 4 =0 Holdover offset disable: The device will ignore the value and holdover will use the current PLL integral path value. This is the default state. =1 Holdover offset enable: The device will adopt the Holdover offset value stored in the cngf_holdover_offset register. This value is then used to set the frequency in holdover mode. Bit 5 =0 Falling Clock Edge selected: The device will reference to the falling edge of the external oscillator signal. This is the default state. =1 Rising Clock Edge selected: The device will reference to the rising edge of the external oscillator signal. Bit 6 =0 Phase Alarm Timeout disable: The phase alarm will not timeout and must be reset by software. =1 Phase Alarm Timeout enable: The phase alarm will timeout after 100 seconds. This is the default state. Bit 7 =0 Auto 2 kHz Sync Disable. The user controls this function using bit 3 of this register, as described above. =1 Auto 2 kHz Sync Enable. External 2 kHz Sync will be enabled only when the source is locked to 6.38 MHz. Otherwise it will be disabled. This is the default state.	11001000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
36	cnfg_differential_inputs	This 2-bit register occupies the entire 8-bit space at address 36(hex). It contains two individual configuration fields, as detailed below: Bit — Configuration field 0 — '1' = Input SEC1DIFF is PECL-compatible '0' = Input SEC1DIFF is LVDS-compatible (Default) 1 — '1' = Input SEC2DIFF is PECL-compatible (Default) '0' = Input SEC2DIFF is LVDS-compatible (7:2) — Unused	XXXXXX10
38	cnfg_output_enable	This 8-bit register occupies the entire 8-bit space at address 38(hex). It contains several individual configuration fields, as detailed below: Bit — Configuration field 0, 1, 3, 4, 6 are unused, and should be set to '0' 2 — '1' = Output port O2 enabled '0' = Output port O2 disabled 5 — '1' = Sonet mode selected for Dig1 '0' = SDH mode selected for Dig1 7 — '1' = O1 output frequency set to 311.04 MHz '0' = O1 output frequency set by Address 3A (5:4) Note: "Disabled" means that the output port holds a static logic value (the port is not Tri-stated).	00011111
39	cnfg_01_output_frequencies	This register holds the frequency selections for the 01 output port, as detailed below. Bit — Configuration field (0:3) and (6:7) are unused (5:4) — Dig1 frequency 00 — 1544 kHz/2048 kHz* 01 — 3088 kHz/4096 kHz 10 — 6176 kHz/8192 kHz 11 — 12352 kHz/16384 kHz * = default For Dig1 the left most frequency values are for Sonet mode and the others are for SDH mode. They are selected via the SONET/SDH bits in register cnfg_output_enable.	00001000
3A	cnfg_differential_outputs	This register holds the frequency selections and the port-technology type for the differential output 01, as detailed below. Bits 7, 6, 3 and 2 are unused. Bit (1:0) — Configuration field: 00 Port disabled; 01 PECL-compatible; 10 LVDS-compatible (default); 11 unused Bit (5:4) — O1 frequency: 00 38.88 MHz (default); 01 19.44 MHz; 10 155.52 MHz; 11 Dig1.	XX00XX10
3B	cnfg_bandwidth	This register contains information used to control the operation of the digital PLL. When bandwidth selection is set to automatic, the DPLL will use the acquisition bandwidth setting when out of lock, and the normal/locked bandwidth setting when in lock. When set to manual, the DPLL will alway use the normal/locked bandwidth setting. Bit (2:0) — Loop bandwidth: 000 0.1 Hz; 001 0.3 Hz; 010 0.6 Hz; 011 1.2 Hz; 100 2.5 Hz; 101 5.0 Hz; 110 10 Hz; 111 20 Hz; 3 unused (6:4) — Acquisition bandwidth: 000 0.1 Hz; 001 0.3 Hz; 010 0.6 Hz; 011 1.2 Hz; 100 2.5 Hz; 101 5.0 Hz; 110 10 Hz; 111 20 Hz; 7 Bandwidth selection '0'= Manual operation '1'= Automatic operation	0111X101

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
	cnfg_nominal_frequency	This register holds a 16 bit unsigned integer representing the desired nominal frequency. This is available to optionally calibrate the nominal output frequency to compensate against variation in the external crystal frequencies.	
3C		Least significant byte.	10011001
3D		Most significant byte.	10011001
	cnfg_holdover_offset	This 19-bit register uses addresses 3E(hex) to 40(hex). It holds a 19 bit signed integer, representing the holdover offset value, which can be used to set the holdover mode frequency when enabled via the holdover offset enabled bit in the cnfg_mode register.	
3E		Least significant byte.	00000000
3F		Next significant byte	00000000
40		Most significant bits. Bit 7 is Auto Holdover Averaging enable - default 1. This enables the frequency average to be taken from 32 samples. One sample taken every 32 seconds, after the frequency has been confirmed to be in-band by the frequency monitors, giving a 17 minute history of the currently locked to reference source for use in Holdover.	1XXXX000
	cnfg_freq_limit	This register holds a 10 bit unsigned integer representing the pull-in range of the DPLL. It should be set according to the accuracy of crystal implemented in the application, using the following formula; Frequency range +/- (ppm) = (cnfg_freq_limit x 0.0785)+0.01647 or cnfg_freq_limit = (Frequency range - 0.01647) / 0.0785 Default value when SRCSW is left unconnected or tied low is ±9.2 ppm. Default value when SRCSW is high is the full range of around ±80 ppm.	
41		Least significant byte	01110110 (SRCSW low) 11111111 (SRCSW high)
42		(7:2) unused (1:0) Most significant bits	XXXXXX00 (SRCSW low) XXXXXX11 (SRCSW high)
43	cnfg_interrupt_mask	Each bit of this 21 bit register, if set to zero, will disable the appropriate interrupt source in the interrupt status register.	11111111
44			11111111
45			XXX11111
	cnfg_freq_divn	This 15 bit integer is used as the divisor for any input to get the phase locking frequency desired. Only active for inputs with the divn bit set to '1'. This will cause the input frequency to be divided by (n+1) prior to phase comparison. The reference_source_frequency bits should reflect the source frequency after the division by (n+1).	
46		least-significant byte.	00000000
47		most-significant bits.	XX000000

Addr. (Hex)	Parameter Name	Description	Default Value (bin)
48	cnfg_monitors	This 7 bit register allows global configuration of monitors and control of phase build out. Bits (1:0) are for configuring frequency monitors- 00 = off, 01 = 15ppm, others are reserved for future use. Bit 2 Phase buildout en enables phasebuildout. If disabled, the DPLL will always lock to 0 degrees. Bit 3 Freeze phase buildout (when phase buildout is enabled) will effectively disable any future phase buildout events but remain with the current phase offset. Bit 4 External protection switching enables the SrcSwit pin to force the locking to either input 4 or 3. Bit 5 Ultra-fast switching enables the dpll to raise an inactivity alarm on the currently selected source after missing only a few cycles. This will enable very fast switching away from the selected source in a protection type application. This is triggered by the main_ref_failed interrupt mechanism. Bit 6 Flag reference loss on TDO will enable the value of the main_ref_failed interrupt to be driven out of the TDO pin of the device. * The default value given is valid when SRCSWT pin is left unconnected or tied low. If SRCSWT is tied high, the default value is 15 (hex).	X0000101*
50	cnfg_activ_upper_threshold 0	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
51	cnfg_activ_lower_threshold 0	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
52	cnfg_bucket_size 0	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
53	cnfg_decay_rate 0	This 2 bit register controls the leak rate of the leaky bucket. The fill-rate of the bucket is +1 for every 128ms interval that has experienced some level of inactivity. The decay rate is programmable in ratios of the fill rate. The ratio can be set to 1:1, 2:1, 4:1, 8:1 by using values of 00, 01, 10, 11 respectively. However, these buckets are not 'true' leaky buckets in nature. The bucket stops 'leaking' when it is being filled. This means that the fill and decay rates can be the same (00 = 1:1) with the net effect that an active input can be recognised at the same rate as an inactive one.	XXXXXX01
54	cnfg_activ_upper_threshold 1	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
55	cnfg_activ_lower_threshold 1	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
56	cnfg_bucket_size 1	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
57	cnfg_decay_rate 1	As for register 53(hex) but for bucket 1.	XXXXXX01
58	cnfg_activ_upper_threshold 2	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
59	cnfg_activ_lower_threshold 2	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
5A	cnfg_bucket_size 2	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
5B	cnfg_decay_rate 2	As for register 53(hex) but for bucket 2.	XXXXXX01
5C	cnfg_activ_upper_threshold 3	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be raised.	00000110
5D	cnfg_activ_lower_threshold 3	This 8 bit register sets the value in the leaky bucket that causes the activity alarm to be cleared.	00000100
5E	cnfg_bucket_size 3	This 8 bit register sets the maximum value that the leaky bucket can reach given an inactive input.	00001000
5F	cnfg_decay_rate 3	As for register 53(hex) but for bucket 3.	XXXXXX01

Selection of Input Reference Clock Source

Under normal operation, the input reference sources are selected automatically by an order of priority, where SEC1 is the highest priority, SEC2 is the second highest priority and SEC3 is the lowest priority. The priorities can be re-assigned with external software. The SEC1 reference source has inputs via either a low speed TTL input port or a high speed PECL/ LVDS input port. Similarly, the SEC2 reference source has both a low speed TTL or a high speed PECL/LVDS input port. The SEC3 (standby) reference source only has provision via a low speed TTL input port. There is provision for one sync clock input via a TTL port. Whilst SEC1, SEC2 and SEC3 reference source inputs can all be active at the same time, only one of the TTL or PECL/LVDS input ports for the SEC1 and SEC2 reference sources may be used at any time, the inactive port is ignored, by setting the priority of that port to zero.

Restoration of repaired reference sources is handled carefully to avoid inadvertent disturbance of the output clock. The ACS8515 has two modes of operation; Revertive and non-Revertive. In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the reference source which is currently selected, a switch over will take place. Many applications prefer to minimise the clock switching events and choose Non-Revertive mode. In Non-Revertive mode , when a re-validated (or newly validated) source has a higher priority then the selected source will be maintained. The re-validation of the reference source will be flagged in the sts_sources_valid register and, if not masked, will generate an interrupt. Selection of the re-validated source can only take place under software control - the software should briefly enable Revertive mode to affect a switch-over to the higher priority source. If the selected source fails under these conditions the device will still not select the higher priority source until instructed to do so by the software, by briefly setting the Revertive mode bit. When there is a reference available with higher priority than the selected reference, there will be NO change of reference source as long as the Non-Revertive mode remains on. This is the case even of there are lower priority references available or the currently selected reference fails. When the ONLY valid reference sources that are available have a lower priority than the selected reference, a failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Automatic Control Selection

When automatic selection is required, the 'cnfg_ref_selection' registers must be set to all-zero. The configuration registers, 'cnfg_ref_selection_priority', held in the µP port are organised as 5, 4-bit registers with each representing an input reference port. Unused ports should be given the value, '0000' in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the whole of the configuration file will be defaulted to the values defined by Table 1. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each reference source should be given a unique number, the valid values are 1 to 15(dec). A value of 0 disables the reference source. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the

channel numbers.

Activity Monitoring

The ACS8515 has a combined inactivity and irregularity monitor. The ACS8515 uses a "leaky bucket" accumulator, which is a digital circuit which mimics the operation of an analog integrator, in which input pulses increase the output amplitude but die away over time. Such integrators are used when alarms have to be triggered either by fairly regular defect events, which occur sufficiently close together, or by defect events which occur in bursts. Events which are sufficiently spread out should not trigger the alarm. By controlling the alarm-setting threshold, the point at which the alarm is triggered can be controlled. The point at which the alarm is cleared depends upon the decay rate and the alarm-clearing threshold. On the alarm-setting side, if several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur a little more spread out, but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. On the alarm-clearing side, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm-clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set).

The "leaky bucket" accumulators are programmable for size, alarm set & reset thresholds and decay rate. Each source is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the accumulator is incremented. The accumulator will continue to increment up to the point that it reaches the programmed bucket size. The "fill rate" of the leaky bucket is, therefore, 8 units/second. The "leak rate"

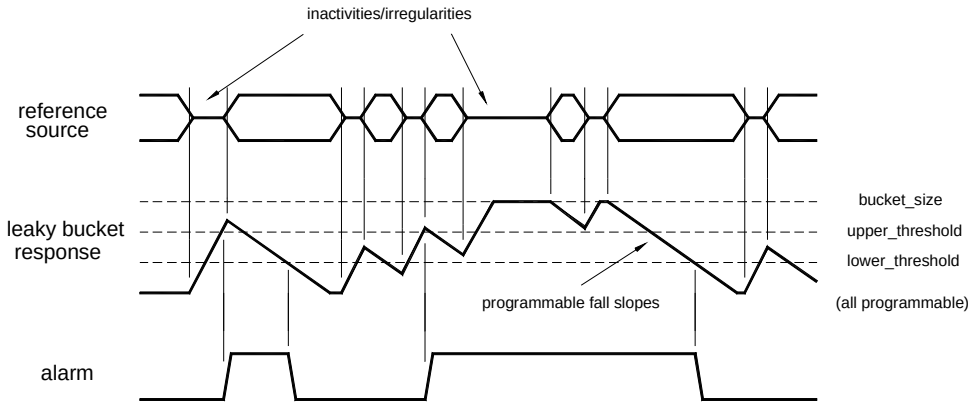


Figure 7: Inactivity and irregularity monitoring

of the leaky bucket is programmable to be in multiples of the fill rate (x1, x0.5, x0.25 and x0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to 'leak' at the same time as a 'fill' is avoided by preventing a 'leak' when a 'fill' event occurs.

Disqualification of a non-selected reference source is based on inactivity, or on an out of band result from the frequency monitors. The currently selected reference source can be disqualified for phase, frequency, inactivity or if the source is outside the DPLL lock range. If the currently selected reference source is disqualified, the next highest priority, active reference source is selected.

Restoration of repaired reference sources is handled carefully to aviod inadvertant disruption of the output clock. The ACS8515 operates in a Non-revertive mode by default. In this mode, if the restored reference source has a higher priority than the reference source which is currently selected, a switch-over to the restored source will not tale place automatically. A restored reference source will assume its correct place in the priority table but a switch-over will only take place automatically upon failure of the currently selected source. It is possible to invoke a switch-over by external control or by enabling revertive mode.

Ultra Fast Switching

A reference source is normally disqualified after the leaky bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if register 48H, bit 5 (Ultra Fast Switching), is set then a loss of activity of just a few reference clock cycles will set the 'no activity alarm' and cause a reference switch. This can be chosen to cause an interrupt to occur instead of or as well as causing the reference switch.

Leaky bucket timing

The time taken to raise an inactivity alarm on a reference source that has previously been fully active (leaky bucket empty) will be:

$$\frac{(\text{cnfg\_activ\_upper\_threshold N})}{8} \quad \text{secs}$$

where N is the number of the relevent leaky bucket configuration. If an input is intermittently inactive then this time can be longer. The default setting of cnfg_activ_upper_threshold is 6, therefore the default time is 0.75 s.

The time taken to cancel the activity alarm on a previously completely inactive reference source is calculated as:

$$\frac{2^{(\text{cnfg\_decay\_rate N})} \times ((\text{cnfg\_bucket\_size N}) - (\text{cnfg\_activ\_lower\_thrshold N}))}{8} \quad \text{secs}$$

where N is the number of the relevent leaky bucket configuration in each case. The default setting are shown in the following:

$$\frac{2^{1} \times (8\text{-}4)}{8} = 1.0 \text{ s}$$

External Protection Switching

Fast external switching between inputs SEC1 and SEC2 can also be triggered directly from a dedicated pin (SRCSW). This mode can be activated either by holding this pin high during reset, or by writing to bit 4 of register address 48Hex.

Once external protection switching is enabled, then the value of this pin directly selects either SEC1 (SRCSW high) or SEC2 (SRCSW low). If this mode is activated at reset by pulling the SRCSW pin high, then it configures the default frequency tolerance of SEC1 and SEC2 to +/- 80 ppm (register address 41Hex and 42Hex). Any of these registers can be subsequently set by external s/w if required.

When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. The operating state (sts_operating_mode register) will always indicate 'locked' in the mode.

Modes of Operation

The ACS8515 has three primary modes of operation (Free-Run, Locked and Holdover) supported by three secondary, temporary modes (Pre-Locked, Lost_Phase and Pre-Locked2). These are shown in the State Transition Diagram, Figure 6.

The ACS8515 can operate in Forced or Automatic control. On reset, the ACS8515 reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-Run mode

The Free-Run mode is typically used following a power-on-reset or a device reset before network synchronisation has been achieved. In the Free-Run mode, the timing and synchronisation signals generated from the ACS8515 are based on the Master clock frequency provided from the external oscillator and are not synchronised to an input reference source. The frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the Master clock.

The transition from Free-Run to Pre-locked(1) occurs when the ACS8515 selects a reference source.

Pre-Locked(1) mode

The ACS8515 will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE specification, if the selected reference source is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-Run mode and another reference source is selected.

Locked mode

The Locked mode is used when an input reference source has been selected and the PLL has had time to lock. When the Locked mode is achieved, the output signal is in phase and locked to the selected input reference source. The selected input reference source is determined by the priority table. When the ACS8515 is in Locked mode, the output frequency and phase follows that of the selected input reference source. Variations of the external crystal frequency have a minimal effect on the output frequency. Only the minimum to maximum frequency range is affected. Note that the term, 'in phase', is not applied in the conventional sense when the ACS8515 is used as a frequency translator (e.g., when the input frequency is 2.048 MHz and

the output frequency is 19.44 MHz) as the input and output cycles will be constantly moving past each other; however, this variation will itself be cyclical over time unless the input and output are not locked.

Lost_Phase mode

Lost_Phase mode is used whenever the selected reference source suffers most kinds of anomalous behaviour. Clock generation is performed in the same way as in the Holdover mode. If the leaky bucket accumulator calculates that the anomaly is serious, the device rejects the reference source and one of the following transitions takes place:

Go to Pre-Locked(2);

- If a known-good standby source is available.

Go to Holdover;

- If no standby sources are available.

Holdover mode

The Holdover mode is used when the circuit was in Locked mode but the selected reference source has become unavailable and a replacement has not yet been selected.

The Holdover performance is mainly limited by what is happening to the TCXO. The ACS8515 has 3 ways of determining Holdover, either;

1. By external frequency setting (cnfg_holdover_offset register)

2. By an internal frequency measuring and averaging system which averages the last 20 minutes

3. By just using the last frequency (as reported by the sts_curr_inc_offset register). This value can be read out of the device and used to build up a longer term average using an external averaging circuit. This value can then to readback into the device and used as the Holdover offset (via cnfg_holdover_offset register).

By default it uses the internal averager. This means that if the TCXO frequency is varying due to temperature fluctuations in the room, then the instantaneous value can be different from the average value, and then it may be possible to exceed the 0.05 ppm limit (depending on how extreme the temperature fluctuations are). It is advantageous to shield the TCXO to slow down frequency changes due to drift and external temperature fluctuations.

In Holdover mode, the ACS8515 provides the timing and synchronisation signals to maintain the Network Element (NE), but they are not phase locked to any input reference source. The timing is based on a stored value of the frequency ratio obtained during the last Locked mode period.

The frequency accuracy of Holdover mode has to meet the ITU-T, ETSI and Telcordia performance requirements. The performance of the external oscillator clock is critical in this mode, although only the frequency stability is important - the stability of the output clock in Holdover is directly related to the stability of the external oscillator.

Pre-Locked(2) mode

This state is very similar to the Pre-Locked(1) state. It is entered from the Holdover state when a reference source has been selected and applied to the phase locked loop. It is also entered if the device is operating in revertive mode and a higher-priority reference source is restored.

PORB

The Power On Reset (PORB) pin resets the device if forced Low for a power-on-reset to be initiated. The reset is asynchronous, the minimum Low pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Asserting Reset (POR) is required at power on, and may be re-asserted at any time to restore defaults. This is implemented

most simplistically by an external capacitor to GND along with the internal pull-up resistor. The ACS8510 is held in a reset state for 250 ms after the PORB pin has been pulled High. In normal operation PORB should be held High.

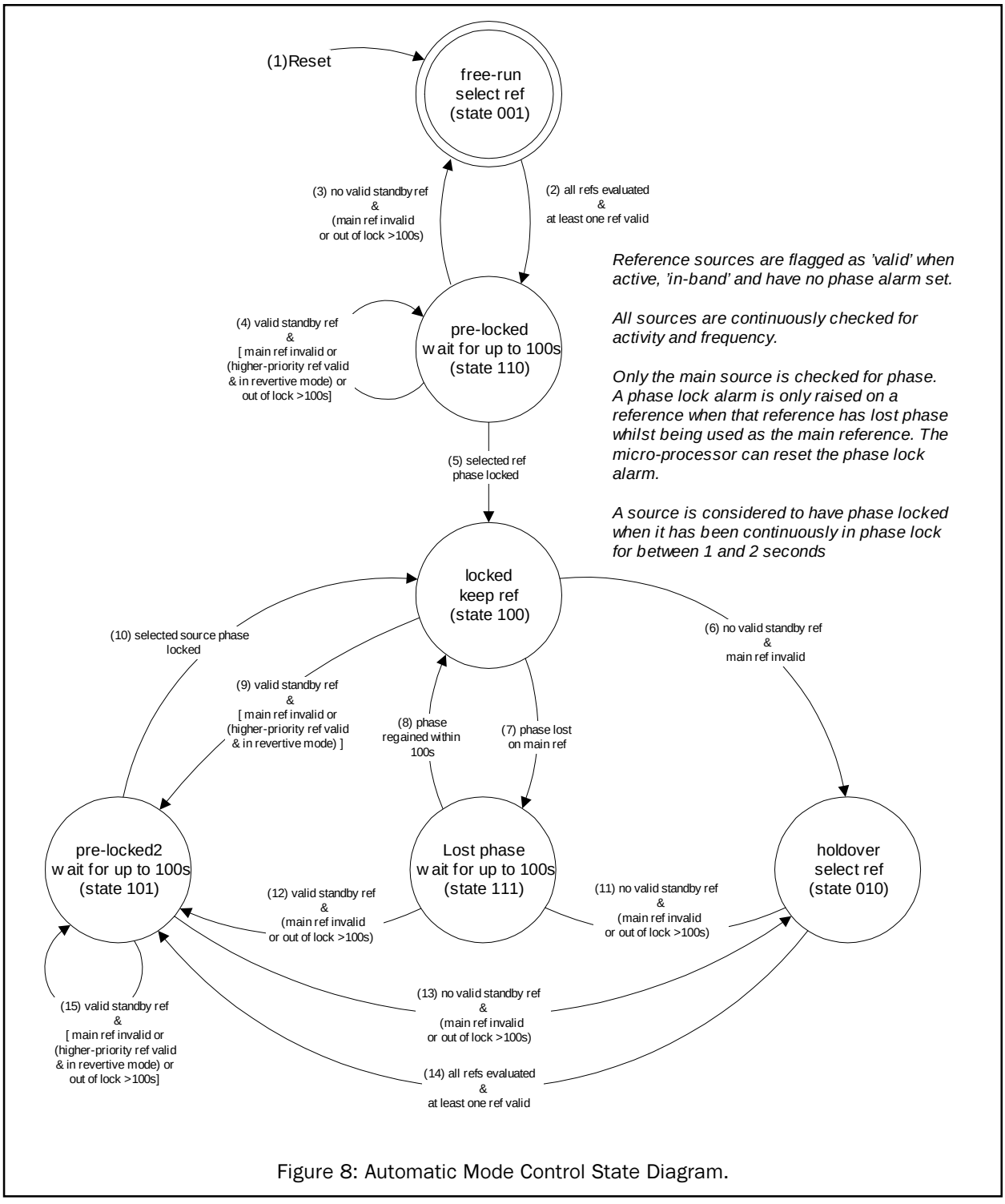


Figure 8: Automatic Mode Control State Diagram.

Electrical Specification

Important Note: The "Absolute Maximum Ratings" are stress ratings only, and functional operation of the device at conditions other than those indicated in the "Operating Conditions" sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage V_{DD}, V_D+, V_A1+,V_A2+	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	Vin	-	5.5	V
Output Voltage (non-supply pins)	Vout	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	85	°C
Storage Temperature	T_{stor}	-50	150	°C

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply (dc voltage) VDD, VD+,VA1+, VA2+, VDD_DIFF	VDD	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5	VDD5	3.0	3.3/5.0	5.5	V
Ambient temperature Range	T_A	-40	-	85	°C
Supply current Typical - one 19 MHz output Maximum - 190 mA before s/w initialisation, 150 mA after s/w intialisation	IDD	-	110	190/150	mA
Total power dissipation	P_{TOT}	-	360	685	mW

DC CHARACTERISTICS: TTL Input pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Input current	I_{in}	-	-	10	µA

DC CHARACTERISTICS: TTL Input pad with internal pull-up.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-up resistor	PU	30	-	80	kW
Input current	I_{in}	-	-	120	µA

DC CHARACTERISTICS: TTL Input pad with internal pull-down.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{in} High	V_{ih}	2.0	-	-	V
V_{in} Low	V_{il}	-	-	0.8	V
Pull-udown resistor	PD	30	-	80	kW
Input current	I_{in}	-	-	120	µA

DC CHARACTERISTICS: TTL Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Vout Low Iol = 4mA	Vol	0	-	0.4	V
Vout High Ioh = 4mA	Voh	2.4	-		V
Drive current	ID	-	-	4	mA

DC CHARACTERISTICS: PECL Input/Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
PECL Input Low voltage Differential inputs (Note 1)	V_{ILPECL}	VDD-2.5	-	VDD-0.5	V
PECL Input High voltage Differential inputs (Note 1)	V_{IHPECL}	VDD-2.4	-	VDD-0.4	V
Input Differential voltage	V_{IDPECL}	0.1	-	1.4	V
PECL Input Low voltage Single ended input (Note 2)	V_{ILPECL_S}	VDD-2.4	-	VDD-1.5	V
PECL Input High voltage Single ended input (Note 2)	V_{IHPECL_S}	VDD-1.3	-	VDD-0.5	V
Input High current Input differential voltage V_{ID} = 1.4v	I_{IHPECL}	-10	-	+10	µA
Input Low current Input differential voltage V_{ID} = 1.4v	I_{ILPECL}	-10	-	+10	µA
PECL Output Low voltage (Note 3)	V_{OLPECL}	VDD-2.10	-	VDD-1.62	V
PECL Output High voltage (Note 3)	V_{OHPECL}	VDD-1.25	-	VDD-0.88	V
PECL Output Differential voltage (Note 1)	V_{ODPECL}	580	-	900	mV

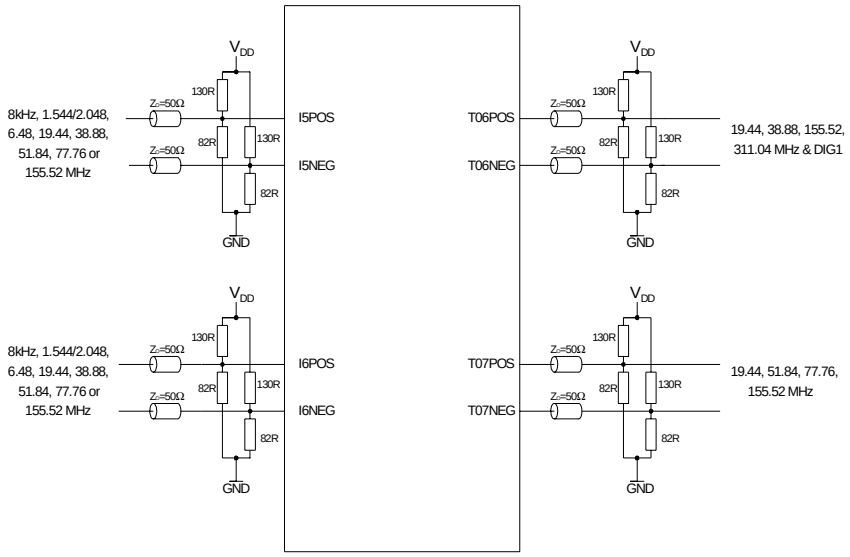
Notes:

Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to VDD and GND respectively.

Note 1. Assuming a differential input voltage of at least 100 mV.

Note 2. Unused differential input terminated to VDD-1.4v.

Note 3. With 50Ω load on each pin to VDD-2v. i.e. 82Ω to GND and 130Ω to VDD.



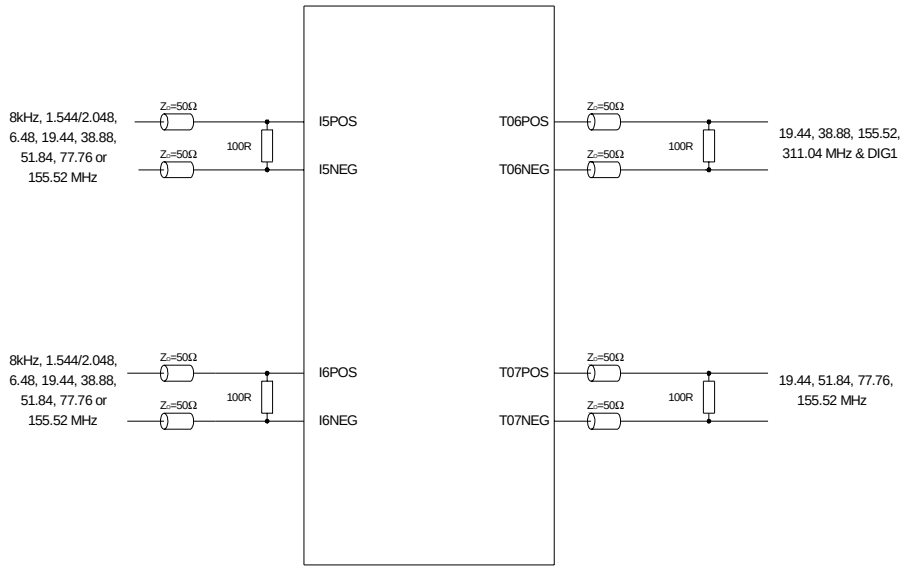
Recommended line termination for PECL Input/Output ports for VDD = 3.3V

DC CHARACTERISTICS: LVDS Input/Output pad.

Across operating conditions, unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
LVDS Input voltage range Differential input voltage = 100 mV	V_{VRLVDS}	0	-	2.40	V
LVDS Differential input threshold	V_{DITH}	-100	-	+100	mV
LVDS Input Differential voltage	V_{IDLVDS}	0.1	-	1.4	V
LVDS Input termination resistance Must be placed externally across the LVDS+/- input pins of ACS8510. Resistor should be 100W with 5% tolerance	R_{TERM}	95	100	105	W
LVDS Output high voltage (Note 1)	V_{OHLVDS}	-	-	1.585	V
LVDS Output low voltage (Note 1)	V_{OLLVDS}	0.885	-	-	V
LVDS Differential output voltage (Note 1)	V_{ODLVDS}	250	-	450	mV
LVDS Charge in magnitude of differential output voltage for complimentary states (Note 1)	$V_{DOSLVDS}$	-	-	25	mV
LVDS output offset voltage Temperature = 25°C (Note 1)	V_{OSLVDS}	1.125	-	1.275	V

Note 1. With 100Ω load between the differential outputs.



Recommended line termination for LVDS Input/Output ports

DC CHARACTERISTICS: Output Jitter Generation

Across operating conditions, unless otherwise stated

Output jitter generation measured over 60 seconds interval, UI pp max measured using Vectron 6664 12.8MHz TCXO on ICT Flexacom + 10MHz reference from Wavetek 905.

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
G813 for 155.52 MHz option 1	500 Hz to 1.3 MHz	UI_{pp} = 0.5	0.058 (Note 2)
G813 for 155.52 MHz option 1	65 kHz to 1.3 MHz	UI_{pp} = 0.1	0.048 (Note 3) 0.048 (Note 2)
G813 for 155.52 MHz option 2	12 kHz to 1.3 MHz	UI_{pp} = 0.1	0.053 (Note 4) 0.053 (Note 5)
			0.058 (Note 6) 0.053 (Note 7)
			0.053 (Note 2) 0.058 (Note 3)
			0.057 (Note 8) 0.055 (Note 9)
			0.057 (Note 10) 0.057 (Note 11)
			0.057 (Note 12) 0.053 (Note 13)
G813 & G812 for 2.048 MHz option 1	20 Hz to 100 kHz	UI_{pp} = 0.05	0.046 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
G812 for 1.544 MHz	10 Hz to 40 kHz	UI_{pp} = 0.05	0.036 (Note 14)
G812 for 155.52 MHz electrical	500 Hz to 1.3 MHz	UI_{pp} = 0.5	0.058 (Note 3)
G812 for 2.048 MHz electrical	65 kHz to 1.3 MHz	UI_{pp} = 0.075	0.048 (Note 3)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
ETS-300-462-3 for 2.048 MHz SEC	20 Hz to 100 kHz	UI_{pp} = 0.5	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SEC (Filter spec 49 Hz to 100 kHz)	20 Hz to 100 kHz	UI_{pp} = 0.2	0.046 (Note 14)
ETS-300-462-3 for 2.048 MHz SSU	20 Hz to 100 kHz	UI_{pp} = 0.05	0.046 (Note 14)
ETS-300-462-3 for 155.52 MHz	500 Hz to 1.3 MHz	UI_{pp} = 0.5	0.058 (Note 3)
ETS-300-462-3 for 155.52 MHz	65 kHz to 1.3 MHz	UI_{pp} = 0.1	0.048 (Note 3)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
GR-253-CORE net i/f, 51.84 MHz	100 Hz to 400 kHz	UI_{pp} = 1.5	0.022 (Note 3)
GR-253-CORE net i/f, 51.84 MHz (Filter spec 20 kHz to 400 kHz)	18 kHz to 400 kHz	UI_{pp} = 0.15	0.019 (Note 3)
GR-253-CORE net i/f, 155.52 MHz	500 Hz to 1.3 MHz	UI_{pp} = 1.5	0.058 (Note 3)
GR-253-CORE net i/f, 155.52 MHz	65 kHz to 1.3 MHz	UI_{pp} = 0.15	0.048 (Note 3)
GR-253-CORE cat II elect i/f, 155.52 MHz	12 kHz to 1.3 MHz	UI_{pp} = 0.1	0.058 (Note 3)
		UI_{rms} = 0.01	0.006 (Note 3)
GR-253-CORE cat II elect i/f, 51.84 MHz	12 kHz to 400 kHz	UI_{pp} = 0.1	0.017 (Note 3)
		UI_{rms} = 0.01	0.003 (Note 3)
GR-253-CORE DS1 i/f, 1.544 MHz	10 Hz to 40 kHz	UI_{pp} = 0.1	0.036 (Note 14)
		UI_{rms} = 0.01	0.0055 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
AT&T 62411 for 1.544 MHz (Filter spec 10 Hz to 8 kHz)	10 Hz to 40 kHz	UI_{rms} = 0.02	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	UI_{rms} = 0.025	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	10 Hz to 40 kHz	UI_{rms} = 0.025	0.0055 (Note 14)
AT&T 62411 for 1.544 MHz	Broadband	UI_{rms} = 0.05	0.0055 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
G-742 for 2.048 MHz	DC to 100 kHz	UI_{pp} = 0.25	0.047 (Note 14)
G-742 for 2.048 MHz (Filter spec 18 kHz to 100 kHz)	20 Hz to 100 kHz	UI_{pp} = 0.05	0.046 (Note 14)
G-742 for 2.048 MHz	20 Hz to 100 kHz	UI_{pp} = 0.05	0.046 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
TR-NWT-000499 & G824 for 1.544 MHz	10 Hz to 40 kHz	UI_{pp} = 5.0	0.036 (Note 14)
TR-NWT-000499 & G824 for 1.544 MHz (Filter spec 8 kHz to 40 kHz)	10 Hz to 40 kHz	UI_{pp} = 0.1	0.036 (Note 14)

Test definition	Filter used	UI spec	UI measurement on ACS8515 Rev 2
GR-1244-CORE for 1.544 MHz	>10 Hz	UI_{pp} = 0.05	0.036 (Note 14)

Notes for the output jitter generation tables

Note 1. Filter used is that defined by test definition unless otherwise stated

Note 2. 5 Hz bandwidth, 19.44 MHz input, direct lock

Note 3. 5 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 4. 20 Hz bandwidth, 19.44 MHz input, direct lock

Note 5. 20 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 6. 10 Hz bandwidth, 19.44 MHz input, direct lock

Note 7. 10 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 8. 2.5 Hz bandwidth, 19.44 MHz input, direct lock

Note 9. 2.5 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 10. 1.2 Hz bandwidth, 19.44 MHz input, direct lock

Note 11. 1.2 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 12. 0.6 Hz bandwidth, 19.44 MHz input, direct lock

Note 13. 0.6 Hz bandwidth, 19.44 MHz input, 8 kHz lock

Note 14. 5 Hz bandwidth, 2.048 MHz input, 8 kHz lock

Microprocessor interface timing

SERIAL MODE

In SERIAL mode, the device is configured to interface with a serial microprocessor bus. The following figures show the timing diagrams of write and read accesses for this mode.

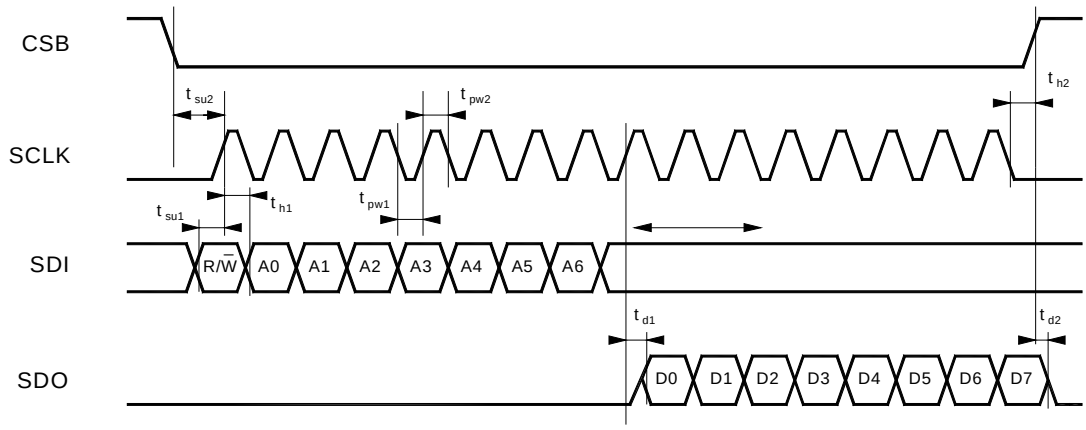
During read access the output data SDO is clocked out on the rising edge of SCLK when the active edge selection control bit CLKE is 0 and on the falling edge when CLKE = 1.

Address, read/write control bit and write data are always clocked into the interface on the rising edge of SCLK.

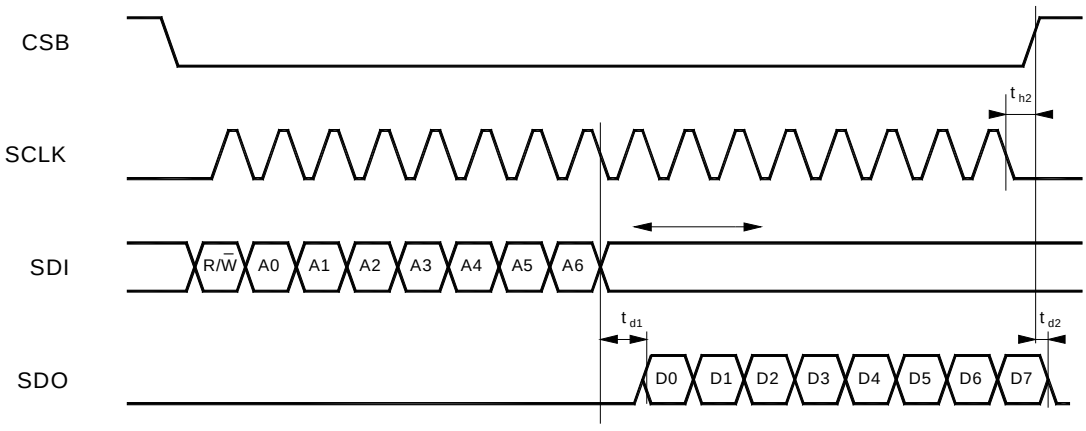
Both input data SDI and clock SCLK are oversampled, filtered and synchronized to the 6MHz internal clock.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).

CLKE = 0; SDO data is clocked out on the rising edge of SCLK



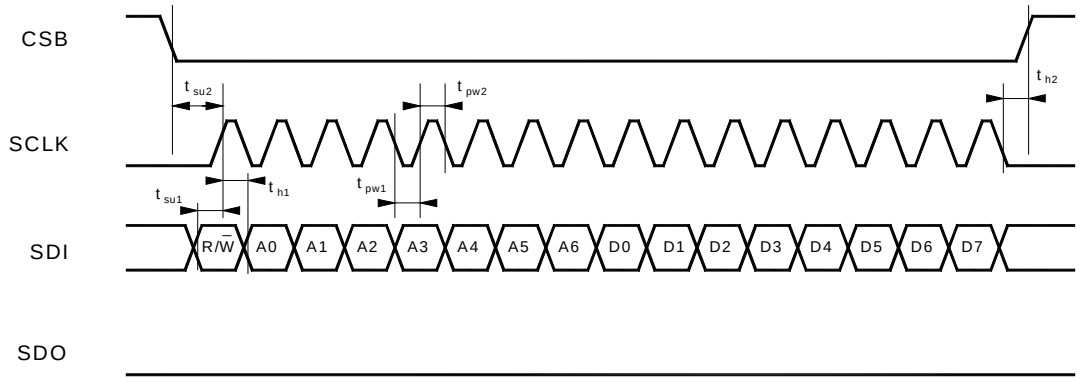
CLKE = 1; SDO data is clocked out on the falling edge of SCLK



Read access timing in SERIAL Mode.

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	160 ns	-	-
t_{d1}	Delay $SCLK_{rising\ edge}$ ($SCLK_{falling\ edge}$ for CLKE = 1)to SDO valid	-	-	17 ns
t_{d2}	Delay $CSB_{rising\ edge}$ to SDO high-Z	-	-	10 ns
t_{pw1}	SCLK low time	180 ns	-	-
t_{pw2}	SCLK high time	180 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB low after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB low after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

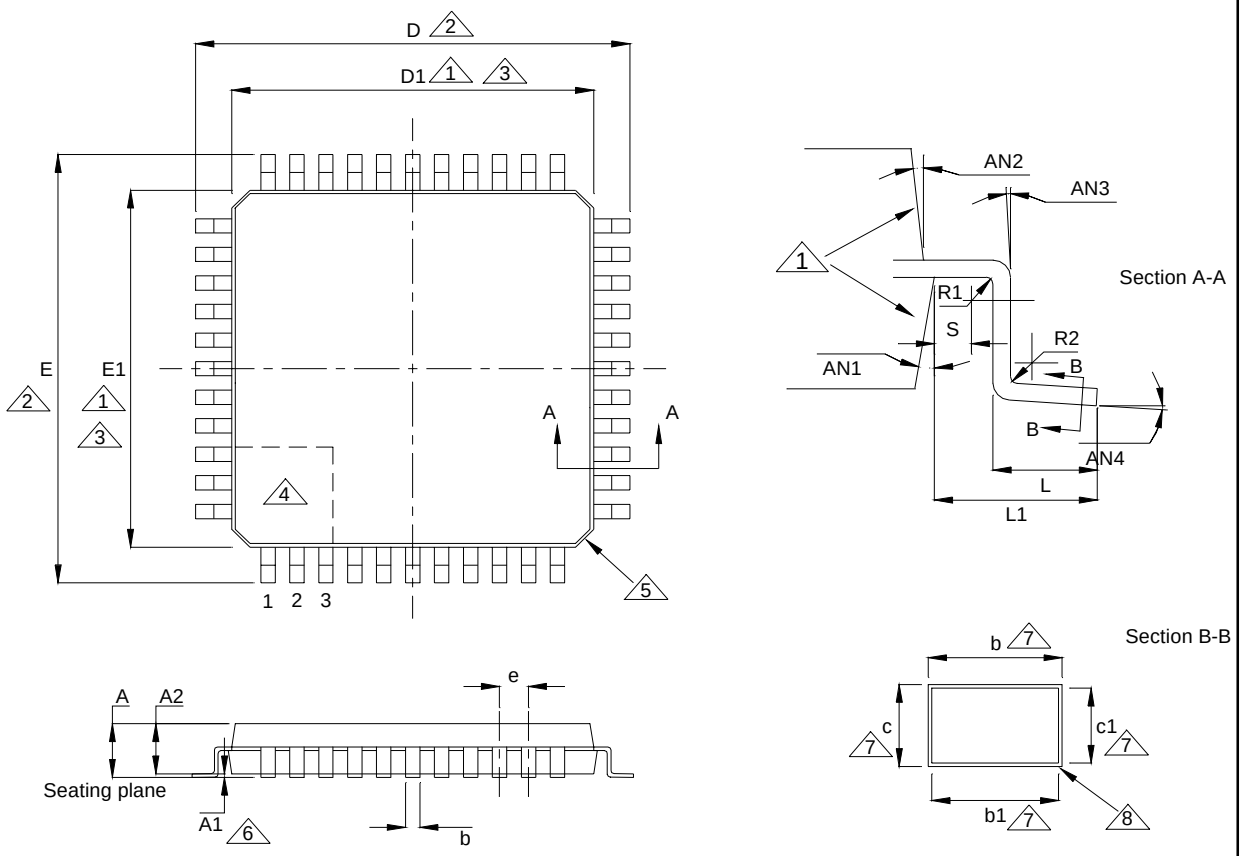
Read access timing in SERIAL Mode.



Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	0 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	160 ns	-	-
t_{pw1}	SCLK low time	180 ns	-	-
t_{pw2}	SCLK high time	180 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	170 ns	-	-
t_{h2}	Hold CSB low after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	160 ns	-	-

Write access timing in SERIAL Mode.

Package information



Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.
2. To be determined at seating plane.
3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Details of pin 1 identifier are optional but will be located within the zone indicated.
5. Exact shape of corners can vary.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. Shows plating.

64 LQFP Package Dimensions in mm	D/E	D1/E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min			1.40	0.05	1.35		11°	11°	0°	0°	0.08	0.08	0.45		0.20	0.17	0.17	0.09	0.09
Nom	12.00	10.00	1.50	0.10	1.40	0.50	12°	12°	-	3.5°	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max			1.60	0.15	1.45		13°	13°	-	7°	-	0.20	0.75		-	0.27	0.23	0.20	0.16

Thermal conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

NOTES

Application information

A simplified Application Schematic for the ACS8515 is illustrated in Figure 9.

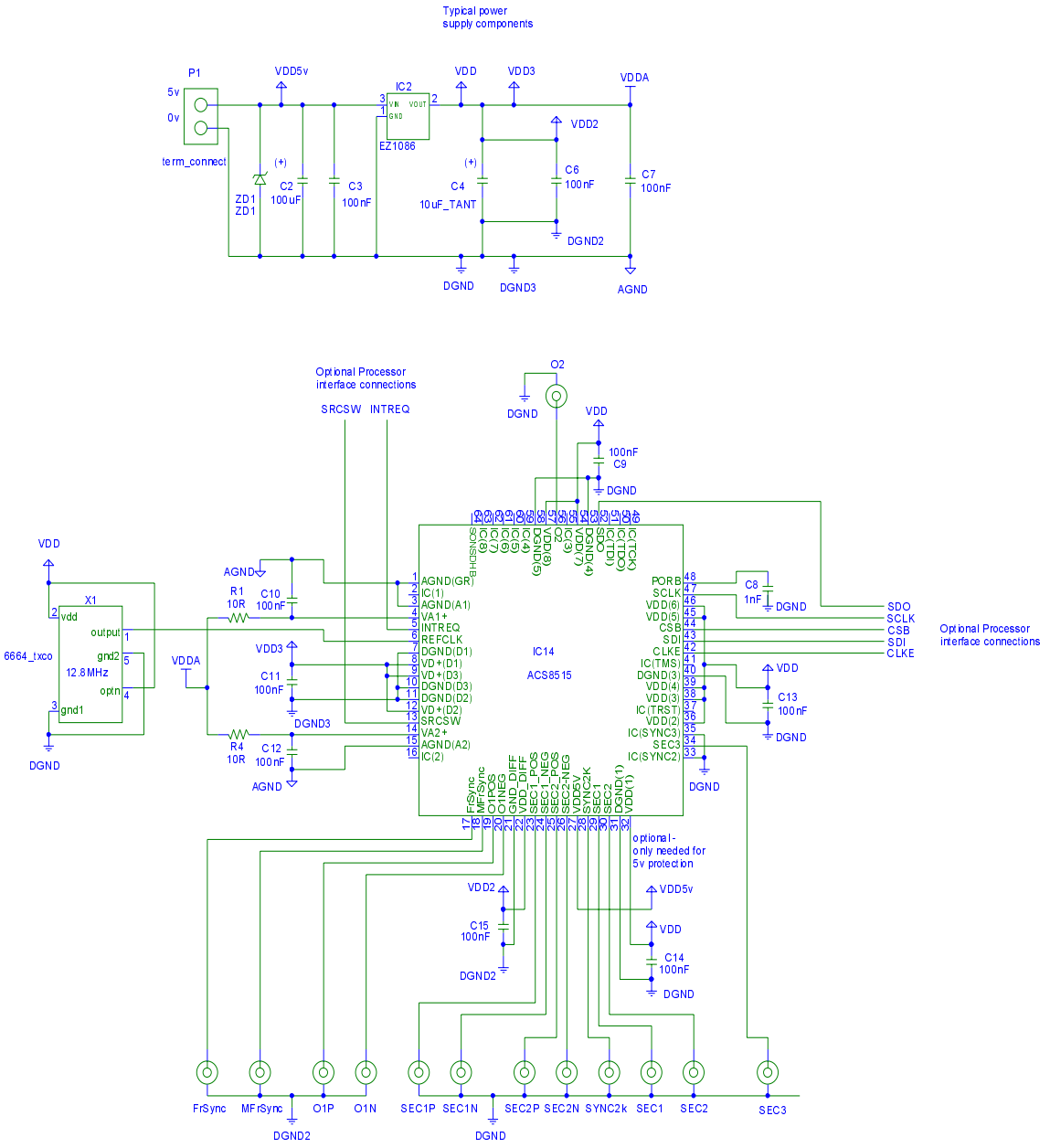


Figure 9: A simplified Application Schematic.

Revision History

Changes from revision 2.04 to 2.05, January 2001.

Item	Section	Page	Description
1	Table of contents	2	Inclusion of Revision History
2	Register description	20	sts_interrupts register re-formatted
3	Register description	22	cnfg_operating_mode register error corrected
4	Register description	24	cnfg_differential_outputs error corrected
5	Register description	25	cnfg_freq_limit register re-formatted and re-written
6	Holdover mode	31	Spelling error corrected
7	Revision History	46	Section added

Ordering information

PART NUMBER	DESCRIPTION
ACS8515	SONET/SDH Line Card Protection, 64 pin LQFP

Disclaimers

Life support - This product is not designed or intended for use in life suport equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech Corporation for such use.

Right to change - Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

For additional information, contact the following:

Semtech Corporation Advanced Communications Products

E-Mail: AdvCom@semtech.com

Internet: http://www.semtech.com

USA: 652 Mitchell Road, Newbury Park, CA 91320-2289

Tel: +1 805 498 2111, Fax: +1 805 498 3804

FAR EAST: 11F, No. 46, Lane 11, Kuang Fu North Road, Taipei, Taiwan, R.O.C.

Tel: +886 2 2748 3380, Fax: +886 2 2748 3390

EUROPE: Delta House, Chilworth Science Park, Southampton, Hants, SO16 7NS, UK

Tel: +44 23 80 769008, Fax: +44 23 80 768612

SEMTECH
Today's Results...Tomorrow's Vision

ISO9001
CERTIFIED