Y/C/Jungle IC for PAL/NTSC

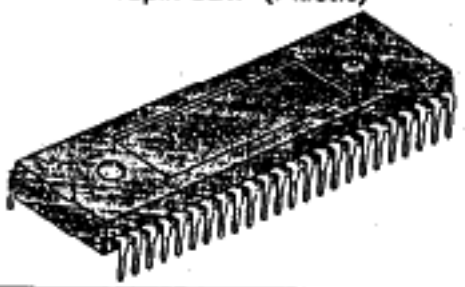
Description

The CXA1213AS is a Y/chroma/jungle signal processing IC of PAL, NTSC (4.43MHz, 3.58MHz) systems color TVs.

Features

- TV system is compatible with PAL,SECAM, and NTSC(4.43MHz,3.58MHz)through combination with the CXA1214P.
- No adjustment of H,V oscillation frequency by count down system.
- Built-in 50/60Hz automatic discrimination circuit and compulsory mode applicable.
- Built-in 3.58/4.43MHz color sub carrier oscillation frequency automatic discrimination circuit and compulsory mode applicable.
- Input prohibition gate function according to frequency of input vertical synchronization. (Noise elimination ability)
- Black expansion function. (New dynamic picture)
- High speed blanking function which blanks interval of characters.

48pin SDIP (Plastic)



- Built-in SHP circuit and OFF applicable.
- Auto white balance IC CXA1024S compatible.

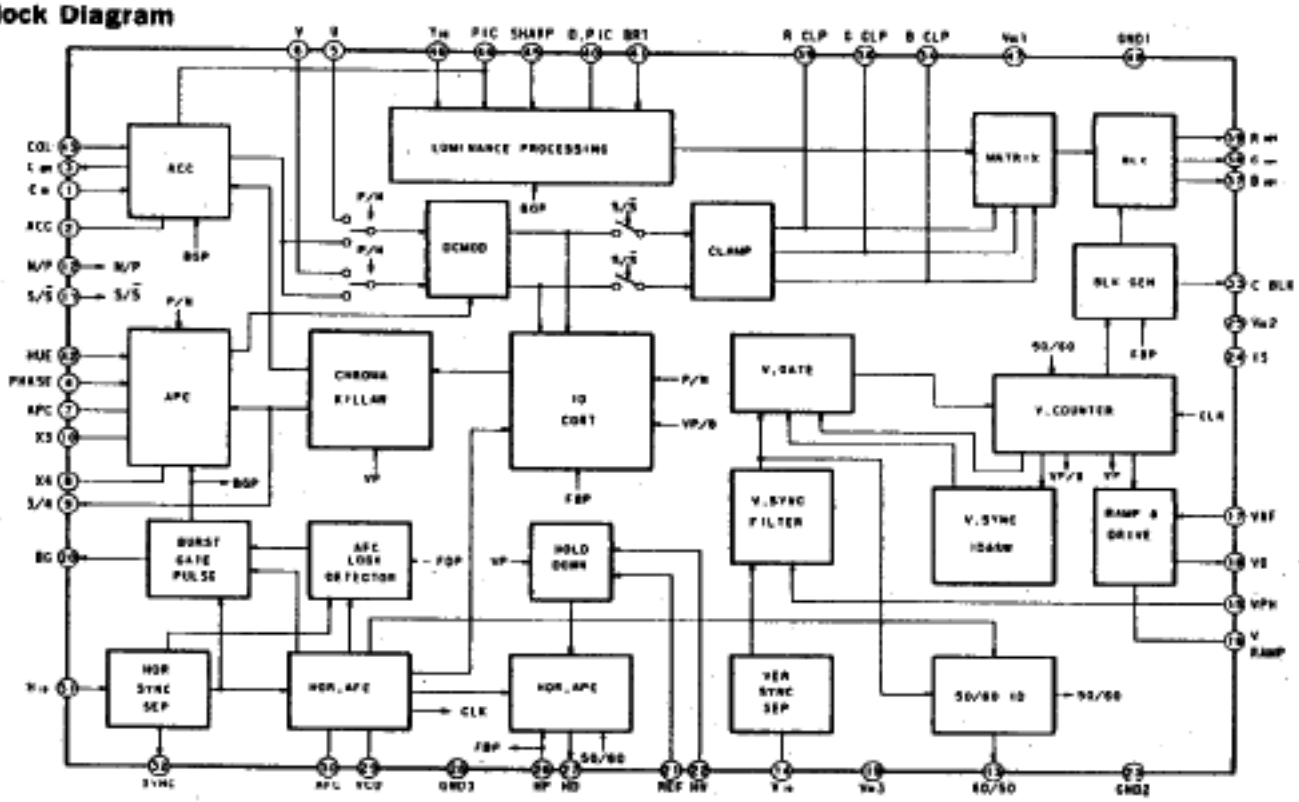
Applications

Color decoder for PAL/NTSC system

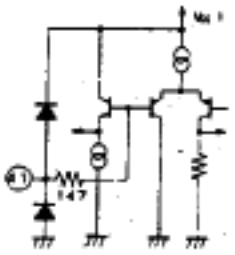
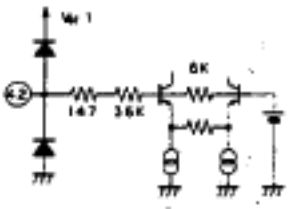
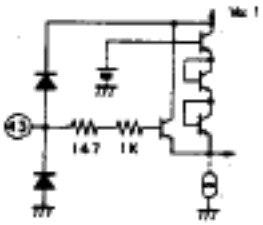
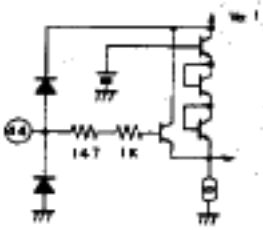
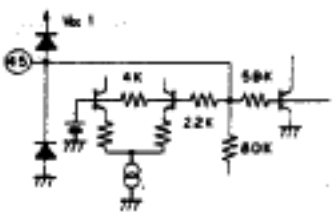
Structure

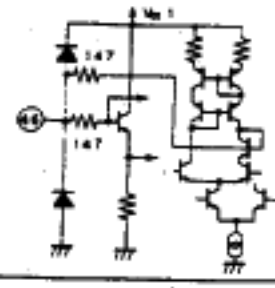
Bipolar silicon monolithic IC

Block Diagram



E90931-HP

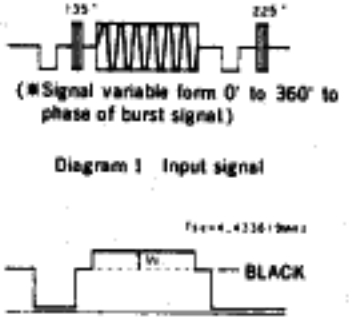
No.	Symbol	Voltage	Equivalent circuit	Description
41	BRT	—		Bright control voltage input pin. It is applicable for interface to auto white balance IC when BRT pin is to be V_{CC}.
42	HUE	4.5V		HUE control voltage input pin for NTSC.
43	COL	—		Color control voltage input pin.
44	PIC	—		Picture control voltage input pin.
45	SHARP	3.2V		Sharpness control voltage input pin. The sharpness circuit in IC dose not go through when this pin is connected to V_{CC}.

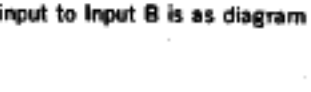
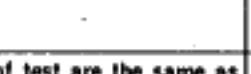
No.	Symbol	Voltage	Equivalent circuit	Description
46	V_{IN}	6.4V		Y signal input pin. 1Vp-p input.(Typ.)
47	V_{CC1}			V_{CC} pin (Y/C system)
48	GND1	0V		GND pin (Y/C system)

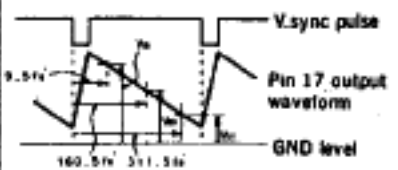
Electrical Characteristics

(Ta=25°C V_{CC}=9V See Electrical Characteristics Test Circuit)

No	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
1	Current consumption	IV_{CC1}	a	a	a	a	a	a	a			20	9	5	3	0	SIG1	A1	Test current consumption at A1	24	39	57	mA
2	BRT Center black level DC (B)	V_{BBC}								ON								Pin 37	Input SIG2 to Input A. Test DC at Pin 37	1.6	1.8	2.0	V
3	BRT MAX black level DC (B)	V_{BBMAX}		b															Pin 37 waveform	3.4	3.6	3.8	
4	BRT MIN black level DC (B)	V_{BBMIN}		c																0	0.45	0.75	
5	PIC Center (B)	V_{BPC}		a														Pin 37	Input SIG3 to Input A. Test DC value at Pin 37 on 3 SW conditions. The formula V_X-V_{BBC} is applied for the Specifications V_{BPC}, V_{BPMAX}, and V_{BPMIN}. Pin 37 waveform	1.8	2.1	2.3	V
6	PIC MAX (B)	V_{BPMAX}					b													2.55	2.85	3.1	
7	PIC MIN (B)	V_{BPMIN}					c													0.25	0.5	0.75	
8	COLOR CONTROL Center	V_{CCBO}					a				ON							Pin 37	Input SIG4 to Input B. Test DC value at Pin 37 on 3SW conditions. The formula V_X-V_{BBC} is applied for the specifications V_{CCBO}, V_{CXBO}, and V_{CNBO}.	0.6	0.9	1.2	V
9	MAX	V_{CXBO}				b	d													1.4	2.0	2.6	
10	MIN	V_{CNBO}				c	d													0	20	100	mV

No	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
11	Detection axis at PAL (B axis)	ϕ_{BP}				a	a											Pin 37 Pin 38 Pin 39	Input the signal as shown in Diagram 1 to Input B. R,G,and B outputs V_X are taken as V_R,V_G,and V_B respectively. At this time vary input signal from 0° to 360° and test maximum value V_{RMAX}, V_{GMAX},and V_{BMAX} of V_R,V_G,and V_B. Phase angles of each output at maximum value are taken as ϕ_{BP}',ϕ_{RP}',and ϕ_{GP}' respectively.(Get maximum value at each output.) At this time the following formulas are applied. $\Phi_{BP}=\phi_{BP}'$, $\Phi_{RP}=\phi_{RP}'-\phi_{BP}'$, $\Phi_{GP}=\phi_{GP}'-\phi_{BP}'$ And also, $(R/B)P=V_{RMAX}/V_{BMAX}$, $(G/B)P=V_{GMAX}/V_{BMAX}$.  (*Signal variable form 0° to 360° to phase of burst signal) Diagram 1 Input signal Diagram 2 RGB each output signal	−10	4	17	deg
12	Detection axis at PAL (R axis)	ϕ_{RP}																		82	90	98	
13	Detection axis at PAL (G axis)	ϕ_{GP}																		228	235	242	
14	Gain ratio (R/B)	(R/B)P																		0.43	0.5	0.57	
15	Gain ratio (G/B)	(G/B)P																		0.24	0.28	0.33	
16	KILLER POINT	D_{KILL}	e															Pin 37	Attennate SIG4 less then 300mVp-p and test amplitude of SIG4 when color killer operates. the following formula is applied for D_{KILL} when the value the is taken as V_X. $20 \log \frac{V_X}{300}$			−28	dB

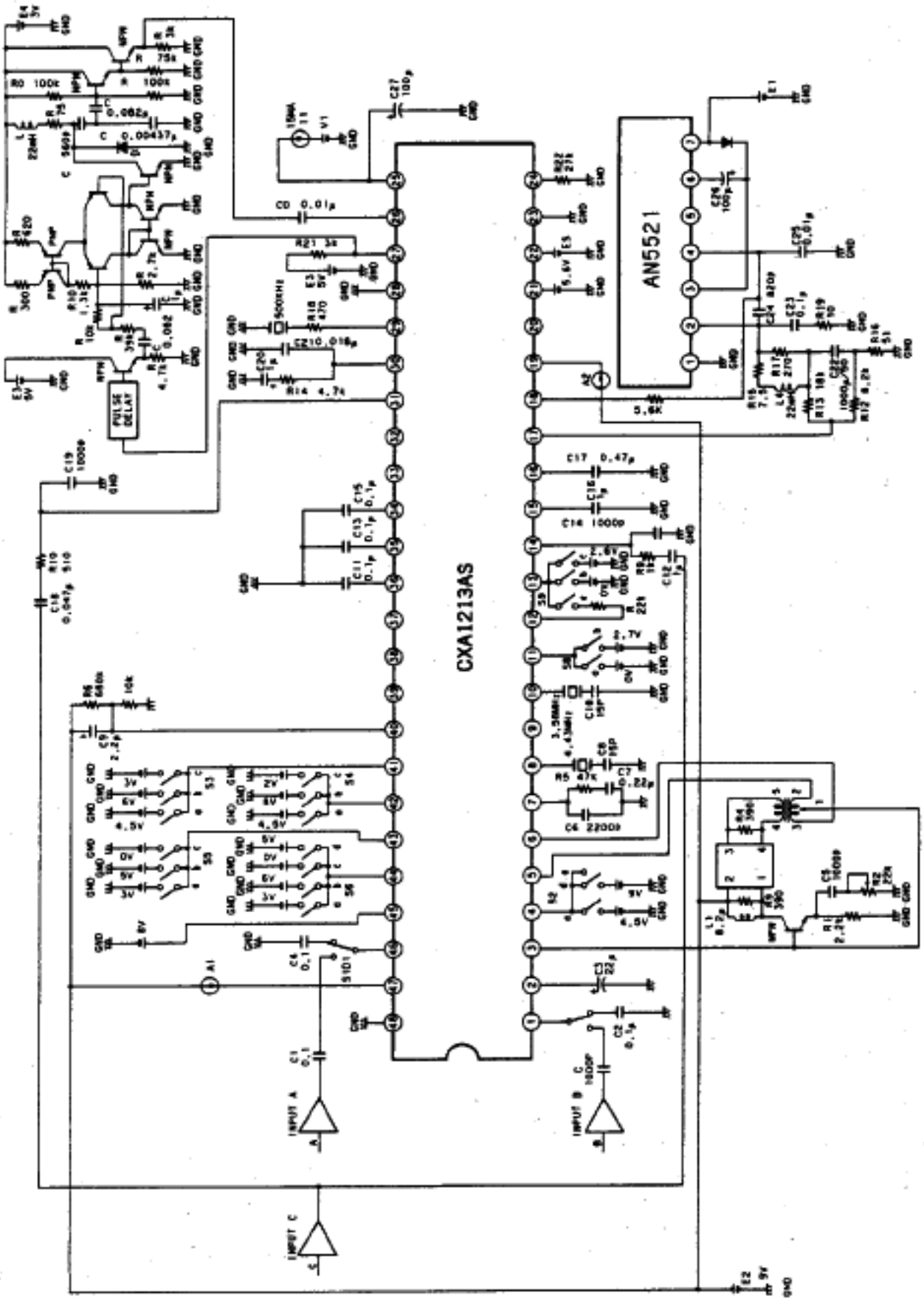
No	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
17	4.43 f_O	ΔF_P	d																Since APC circuit does not operate when Pin 4 is connected to 9V, the carrier frequency of SIG4 is varied and the frequency FP when the demodulation waveform occurs at Pin 37 is to be free run frequency. Then formula $\Delta F_P = F_P - 4433619$Hz applies.	−220	0	210	
18	APC pull-in (+)	ΔF_{CPU}	e								ON							Pin 37	The APC circuit operates when Pin 4 is opened and vary the subcarrier frequency as the killer circuit is operating.	240	420		Hz
19	APC pull-in (−)	ΔF_{CDO}	e																The frequency when demodulation waveform occurs at Pin37 is to be pull-in range frequency. Then the following formulas are applied. $\Delta F_{CUP} = (f_X - F_P)$ (when f_X is $f_X > F_P$) $\Delta F_{CDO} = (f_X - F_P)$ (when f_X is $f_X < F_P$)		−870	−550	
20	Detection axis at NTSC (B axis)	Φ_{BN}	a														SIG5	Pin 37 Pin 38 Pin 39	The contents of test are the same as the Items 10 to 15, however, the signal input to Input B is as diagram below.  (* Signal variable from 0° to 360° to phase of burst signal.)	0	11	20	deg
21	Detection axis at NTSC (R axis)	Φ_{RN}																		93	99	105	
22	Detection axis at NTSC (G axis)	Φ_{GN}																		234	240	246	
23	Gain ratio (G/B)	(R/B) N																		0.72	0.77	0.84	
24	Gain ratio (G/B)	(G/B) N																		0.26	0.3	0.34	
25	HUE characteristics 1	Φ_{BNMAX}	a	a	b	a	a	a	a		ON	20	9.0	5.0	3.0	0		Pin 37 Pin 38 Pin 39	The contents of test are the same as the Items 10 to 15. Input signal is shown in the right diagram.  (Sub carrier frequency is to be free run frequency F_N.)		−18.5	−8	deg
26	HUE characteristics 2	Φ_{BNMIN}			c															18	30		

No.	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
27	3.58 f_0	ΔF_N	d		a														The contents of test are the same as the same as Items 17 to 19. $\Delta F_N = F_N - 3579545HZ$ F_N: Free run frequency $\Delta F_{CUP1} = f_x - F_N$ Hz (When fx is $fx > F_N$) $\Delta F_{DO1} = f_x - F_N$ Hz (when fx is $fx < F_N$)	−180	30	230	Hz
28	APC pull-in (+)	ΔF_{CPUI}	e								ON									210	410		
29	APC pull-in (−)	ΔF_{DOI}	e																		−1000	−600	
30	Horizontal power supply voltage	V_{CH}	a														SIG1	Pin 25	Test voltage at Pin 25 when current 15mA is flowed into Pin 25.	8.6	9.0	9.4	V
31	Vertical power supply inflow current	I_{CV}																A_2	Test the current flows into Pin 19	9.5	13.7	18	mA
32	Vertical triangle level (H) 1	V_{H1}																Pin 17	Test the voltages V_{H1}, V_{M1}, and V_{L1} at Pin 17 after 9.5fH', 160.5fH', and 311.5fH' from V_{SYNC} pulse rising. 	3.75	4.00	4.25	V
33	Level (M) 1	V_{M1}																		2.55	2.90	3.20	
34	Level (L) 1	V_{L1}																		1.35	1.80	2.40	
35	S/S output level (H)	$V_{S/SH}$																Pin 32	Test each level, $V_{S/SH}$ and $V_{S/SL}$, and pulse width $t_{S/S}$ from GND of Pin 32 output. 	7.5	7.85	8.2	V
36	S/S output level (L)	$V_{S/SL}$																		0	0.02	0.1	
37	S/S output pulse width	$t_{S/S}$																		4.4	4.8	5.2	μs

No.	Item	Symbol	SW conditions 2	3	4	5	6	7	8	101	102	Bias conditions (V) E1	E2	E3	E4	E5	Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
38	BG OUT level (H)	V_{BGH}																Pin 20	Test each level, V_{BGL}, V_{BGH}, and pulse width t_{BGI} from GND of Pin 20 output.	2.7	3.3	4.1	V
39	BG OUT level (L)	V_{BGL}																		0	0.01	0.1	V
40	BG OUT pulse width	t_{BGI}																	Pin 20 output waveform	2.9	3.4	3.9	µs
41	HBLK level (H)	V_{HBLH}																	V pulse, H pulse, GND, 3.5V, Pin 33 Output waveform	1.8	2.2	2.6	V
42	HBLK level (L)	V_{HBLL}																		0	0.05	0.1	V
43	H_{BLK} pulse width	t_{HBLK}																		10.8	11.7	12.5	µs
44	V_{BLK} level (H)	V_{VBLH}																	Test each level from GND of Pin33 output waveform and pulse width. Input SIG1 or SIG5 to Input C when t_{BLK1} and t_{BLK2} are tested.	4.2	4.8	5.4	V
45	V_{BLK} pulse width 1	t_{VBLK1}																		1.70	1.76	1.80	ms
46	V_{BLK} pulse width 2	t_{VBLK2}															SIG5			1.40	1.44	1.50	ms
47	BG OUT phase	t_{BGD}															SIG1		Pin 20 output waveform that tests the time difference t_{BGD} at this point. Test the time difference t_{BGD} at this point, Input C waveform, Pin 20 output waveform	0.4	0.7	1.1	µs
48	HOLD DOWN operating voltage	V_{HOLDI}														※			※ Raise the voltage of E5 from 5.6V subsequently and test offset voltage from 5.6V of E5 when HD pulse of Pin 27 stops.	0	45	60	mV

No	Item	Symbol	SW conditions									Bias conditions (V)					Input C conditions	Test point	Details of measurement	Min.	Typ.	Max.	Unit
			2	3	4	5	6	7	8	101	102	E1	E2	E3	E4	E5							
49	Horizontal pull-in range 1	F_{H1}	a	a	a	a	a	a	a			20	9.0	5	3	0	SIG8	Pin 37 Input C	Confirm the output waveform Pin 37 agrees with f_H=16.075kHz and f_H=15.175kHz of SIG8 and SIG9 which are input to Input C. This range is to be pull-in range.			16.075	kHz
50	Horizontal pull-in range 2	F_{H2}															SIG9			15.175			
51	Vertical pull-in range 1	F_{V1}						b									SIG1	Pin 37 Input C	Pull-in frequency range which varies V frequency and synchronizes from asynchronism. * However, let f_H=15.625kHz. (Compulsion 50Hz mode)	42.1	50	72.6	Hz
52	Vertical pull-in range 2	F_{V2}						c											Pull-in frequency range which varies V frequency and synchronizes from asynchronism. * However, let f_H=15.625kHz (Compulsion 60Hz mode)	48.6	60	72.6	

Electrical Characteristics Test Circuit



Input Signal

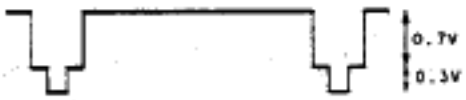
SIG1

PAL V_{SYNC} available
f_H=15.625kHz

SIG2

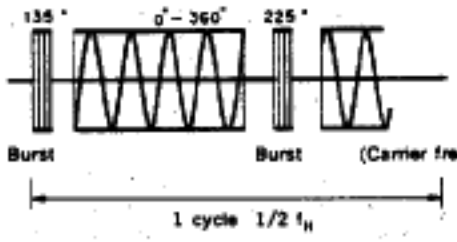
PAL V_{SYNC} available
f_H=15.625kHz

SIG3



PAL V_{SYNC} available
f_H=15.625kHz

SIG4



PAL V_{SYNC} available
f_H=15.625kHz
(Carrier frequency f=4.433619MHz,phase variation applicable)

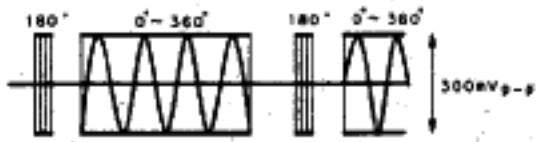
SIG5

NTSC V_{sync} available
f_H=15.734kHz

SIG6

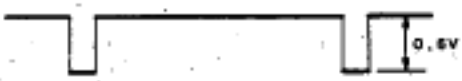
NTSC V_{sync} available
f_H=15.734kHz

SIG7



NTSC V_{sync} available
f_H=15.734kHz
(Carrier frequency f=3.579545MHz, phase variation applicable)

SIG8



f_H'=(15.625+0.45) kHz
(V_{sync} available)

f_H'=(15.625−0.45) kHz
(V_{sync} available)

SIG9

T-77-07-09

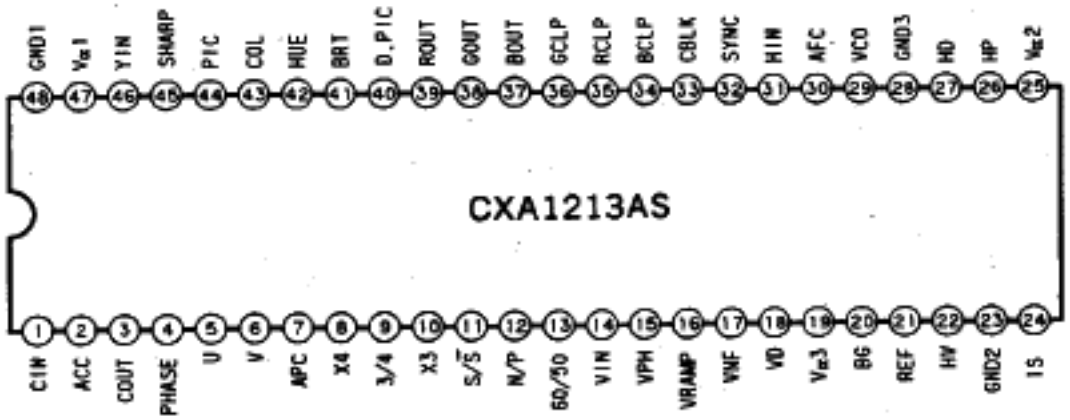
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	12	V
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	2.2	W

Recommended Operating Conditions

• Supply voltage	V_{CC}	9 ±1	V
• Operating temperature	T_{opr}	−20 to +75	°C

Pin Configuration



Operation Description

(1) Luminance signal system

(i) SHP circuit

The luminance signal that is input from Pin 46 is emphasized around 3.0 MHz of luminance signal by SHP circuit. Connect Pin 45 to V_{CC} so that SHP circuit gets OFF when it is not necessary.

(ii) BLK MUTE circuit

Connecting Pin 41 to V_{CC} replaces BLK section to black level and connection with auto white balance IC (CXA1024S) applicable.

(iii) Fast BLK circuit

Inputting the character signal etc. to CBLK pin makes the function that attenuates the character signal part of video signals available.

(iv) New Dynamic Picture circuit

The function to expand black operates in the signals under 50IRE of input signal. Connecting Pin 40 at around 10kΩ resistance makes the function cancelled.

(2) Chroma system

(i) ACC circuit

Detects the burst signal (that is demodulated by average level detection) by ACC DET and applies return to ACC amplifier according to the detection output to keep the demodulated burst level always stable.

(ii) APC circuit

The input chroma component from Pin 1 composes B-Y signal and R-Y signal by detecting to the external crystal at Pin 8 (3.58MHz) or Pin 10 (4.43MHz), which are output of VCO by APC circuit, after it is amplified via ACC and color amplifiers.

(iii) Matrix

Composes G-Y signal by mixing B-Y and R-Y signals. Then,outputs at R,G,and B orignal signal by these signals and the luminance signal Y.

(iv) ID correction

PAL system is sent after R-Y (V) component of the sygnal gets inverted every 1H. Due to this reason, the demodulation axis also needs to be inverted every 1H. The R-Y axis is inverted every 1H synchronizing with HP in this IC, however, the flip-flop corrects it if it is wrong according to R-Y burst detection output.

(v) SECAM system applicable (Combined with the CXA1214P)

The combination with the CXA1214P enables the SECAM signal demodulated. (See Application Circuit 2) Inputting the direct voltage of H level (over 2.5V) and R-Y and B-Y signals, which SECAM signal is demodulated to R CLP (Pin 35) and B CLP (Pin 34) via direct capacitor make the original signals R,G, and B output.

(3) Jungle system

The count down system is adopted by the $32f_H$ ceramic oscillator.

Due to these reason, no adjustment of H and V free run frequency is realized and the number of pins and external parts get lesser.

The horizontal synchronization cicuit adopts double loops. The input, VCO frequency and phase are combined and the HD pulse is generated in the first loop and the phase with FBP of deflection is combined in the second loop.

The burst gate pulse is generated synchronizing with the input horizontal sync, however this generates a artifical pulse at no signal with a artifical horizontal sync from the horizontal count down circuit.

The vertical synchronization circuit varies the width of input prohibition gate according to input frequency and shortens the section that vertical sync passes throngh to improve the elimination capacity of the noises going into vertical sync. (See Diagram of (i) Vertical Synchronization Prohibition Gate)

At the same time, the elminated capacity of the noises are furthermore improved since the peak hold circuit is adopted at vertical sync separation circuit.

The auto discrimination circuit is built in when Switching 50 or 60Hz.

(i) Vertical synchronization prohibition gate

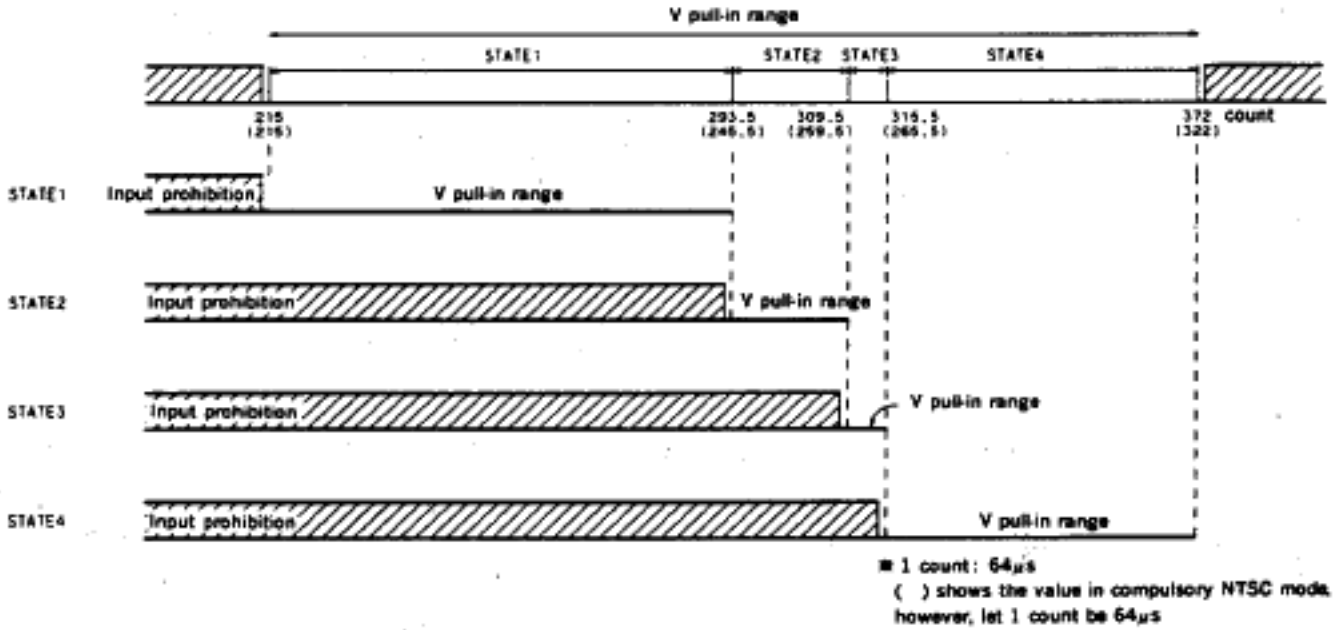
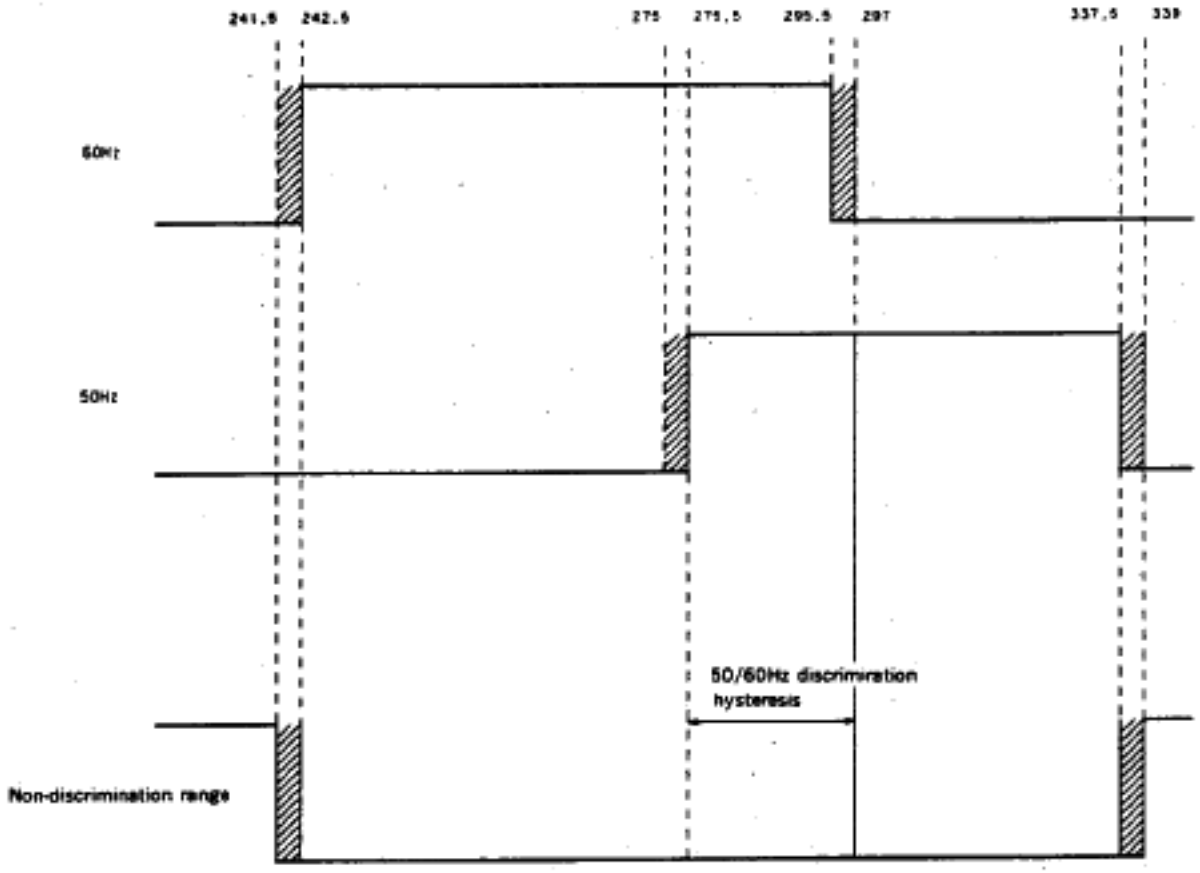


Diagram 1. Vertical pull-in range

This is synchronized in state 1 to 4 by vertical sync wavelength. The vertical pull-in range is composed as Diagram 1. Throngh this,the noise is eliminated as providing the input prohibition gate severely not to discriminate the non-continuous noise pulse besides vertical sync. (ex. VHS noise).

(ii) 50/60Hz Discrimination Operation



The count number is 64μs by a count ($=1/f_H$)

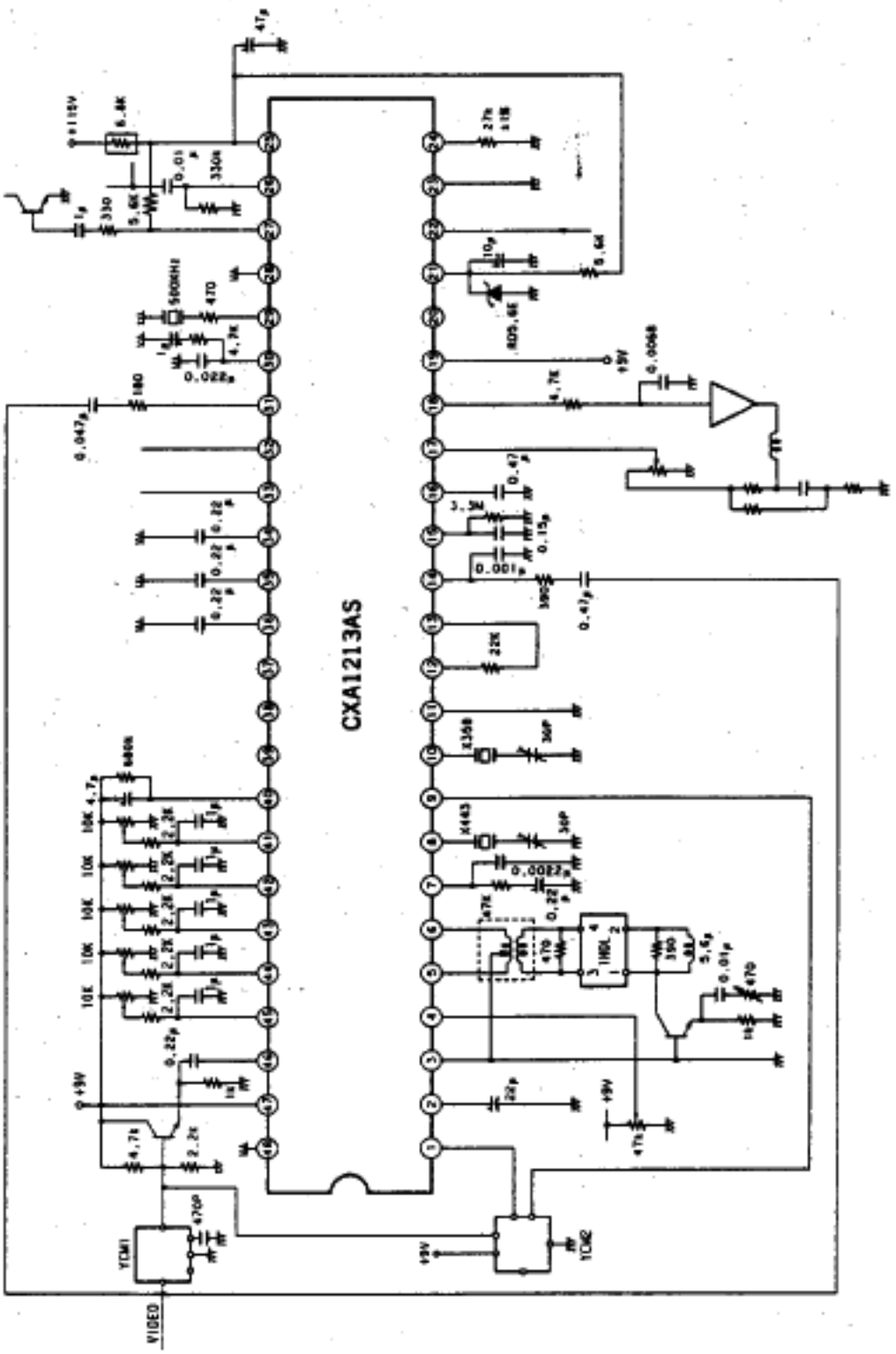
Diagram 2. 50/60Hz Discrimination Range

This IC automatically discriminates the discrimination of 50Hz and 60Hz from the input vertical sync. The 50Hz has priority when the power supply is on and discriminates as in Diagram 2 by vertical sync wavelength. The discrimination output pin is Pin 13 ,and outputs as 60Hz mode H and 50Hz mode L.

For example, this discriminates as 60Hz mode when the input signal is from 242.5 to 295.5 counts and 50Hz mode when the input signal is from 275.5 to 337.5 counts. And the hysteresis is provided between the count from 275.5 to 295.5. No discrimination occurs besides those so that the discrimination output of former state is held.

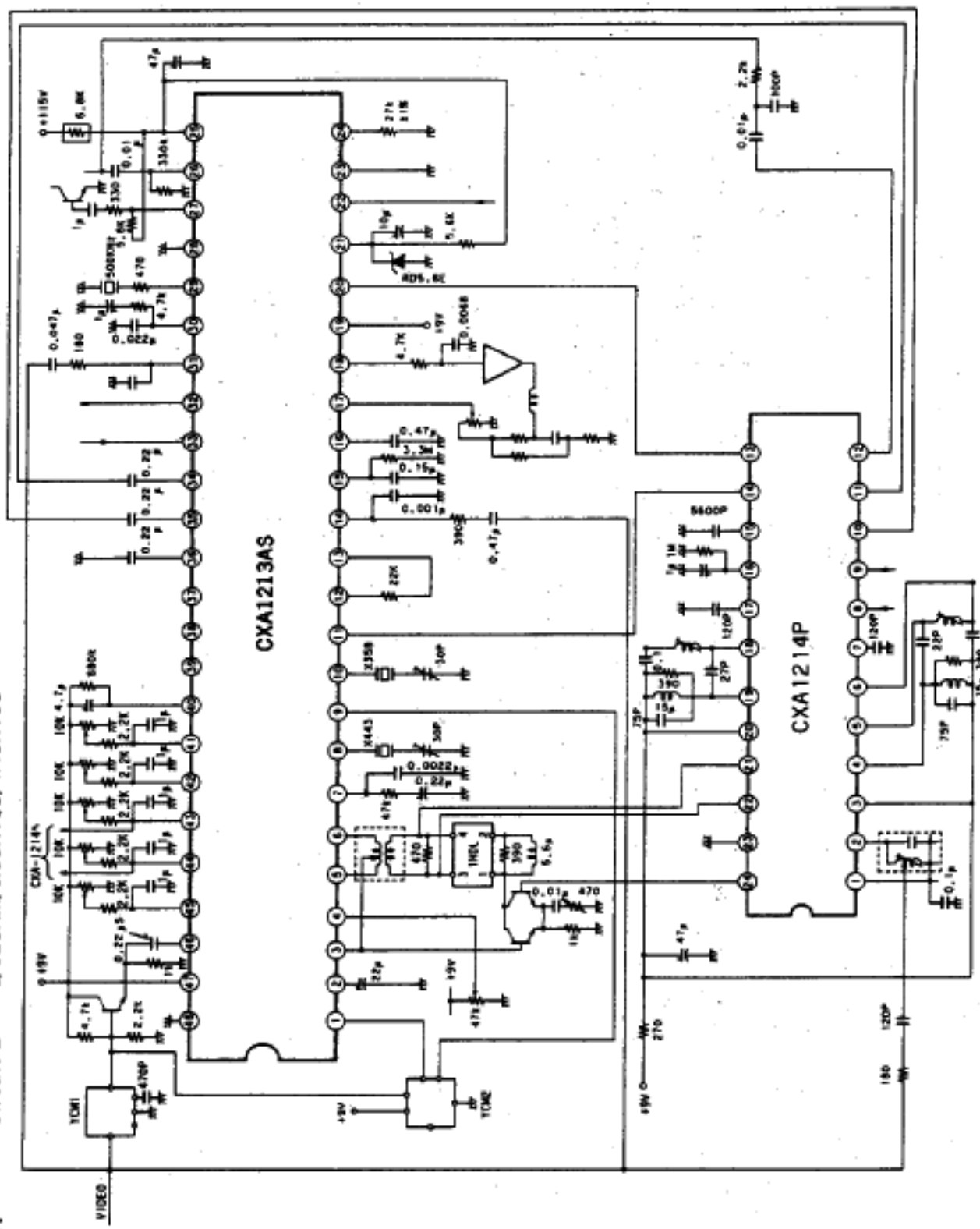
The mark ▨, which is a discrimination error occurs due to like an error of vertical sync separation circuit in this IC, is a state that discriminates as either 50Hz or 60Hz.

Application Circuit 1 PAL/3.58NTSC/4.43NTSC System



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 PAL/SECAM/3.58NTSC/4.43NTSC



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Bright Control Characteristics

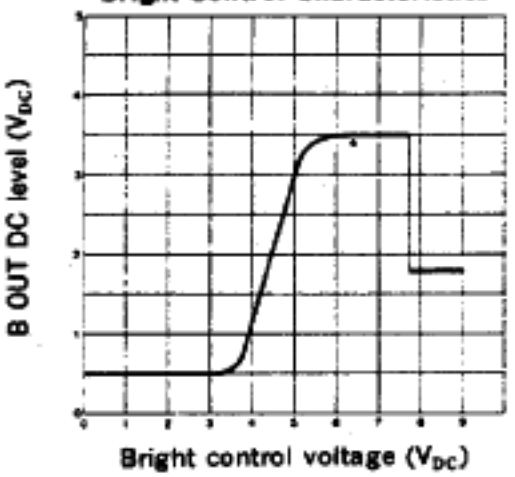


Fig. 1

Picture Control Characteristics

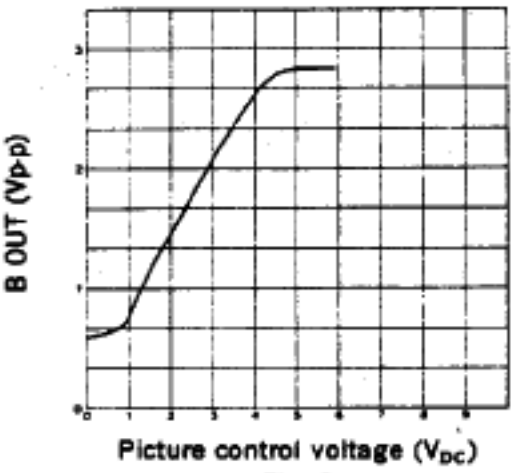


Fig. 2

New Dynamic Picture I/O Characteristics

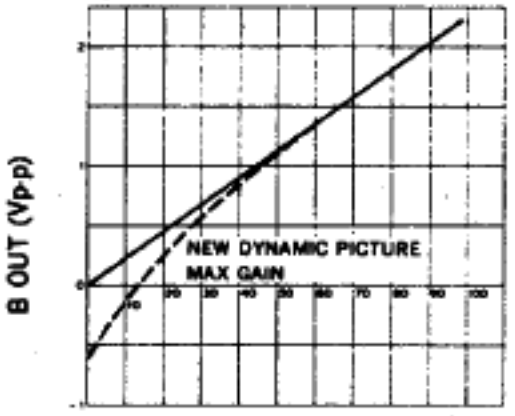


Fig. 3

Color Control Characteristics

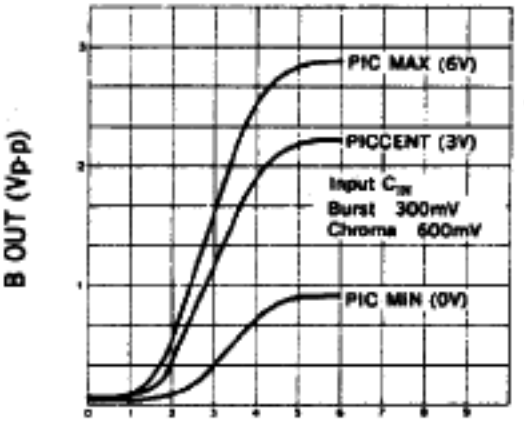


Fig. 4

ACC Characteristics

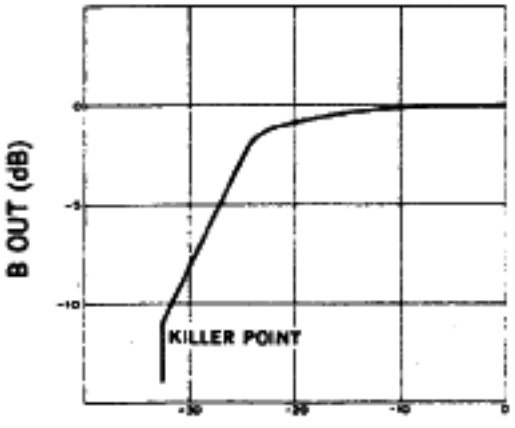


Fig. 5

Y. Signal Frequency Characteristics

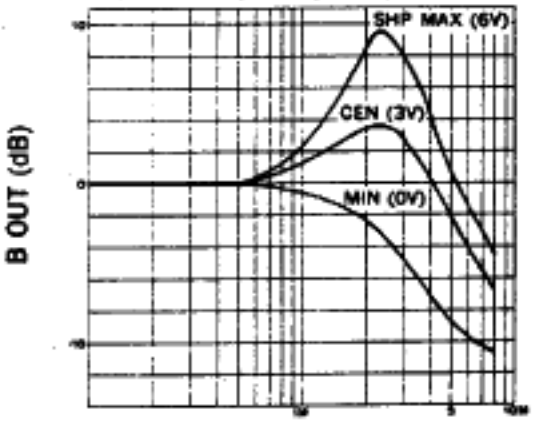
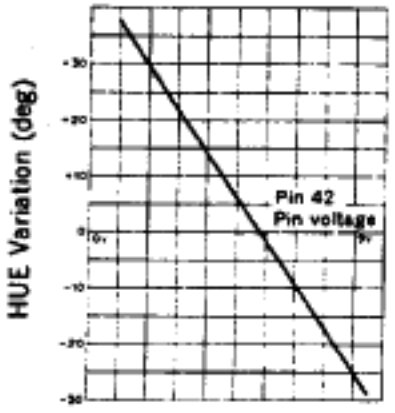


Fig. 6

HUE Control Characteristics



Pin voltage at pin 42

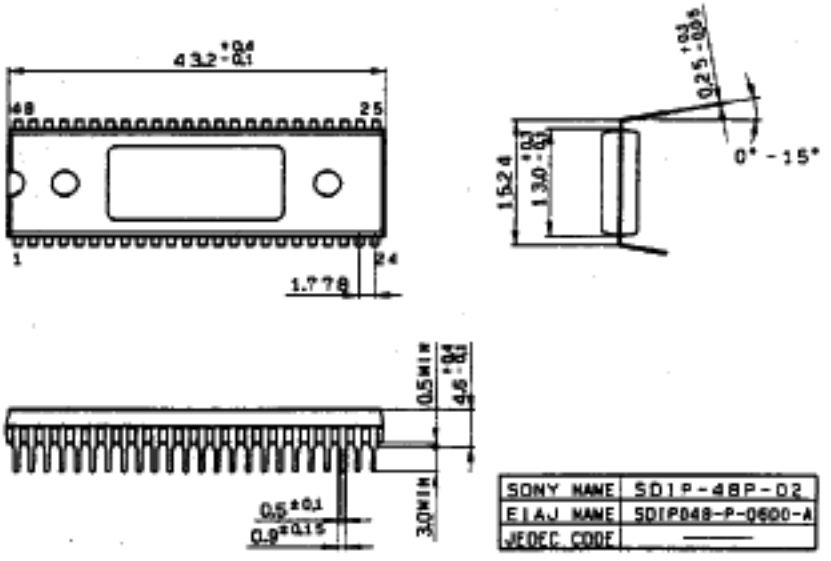
Fig. 7

Notes or Operation

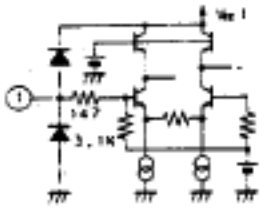
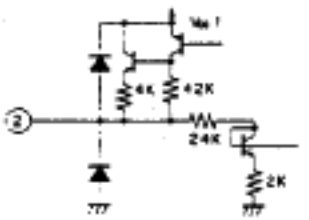
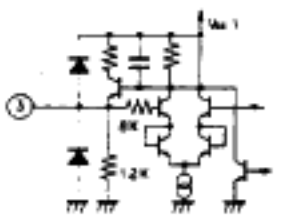
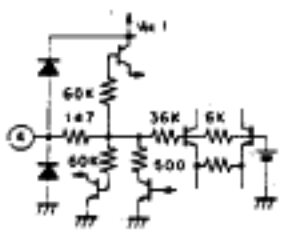
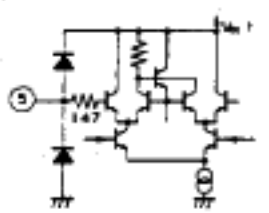
(1) Recommend adjusting the free run frequency to 4.433619MHz and 3.579545MHz by using the trimmer capacitor.
(2) The HUE characteristics 1 and 2 are tested at HUE pin voltage 8V and 2V. The HUE center is about 6.0V.
(3) Adjust the detection axis of PAL mode B output to 0deg by contorolling Pin 4 (PHASE).
(4) Input the signal to Pin 33 in the emitter follower type when the high speed blanking function used.

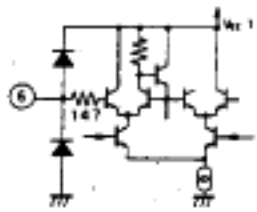
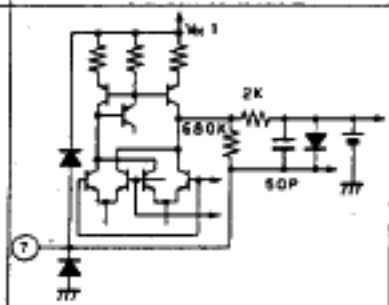
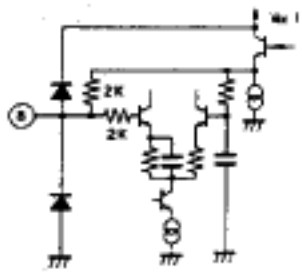
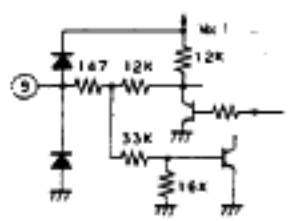
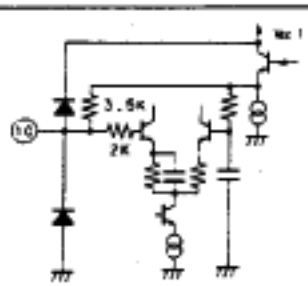
Package Outline **Unit : mm**

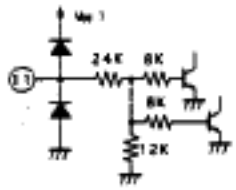
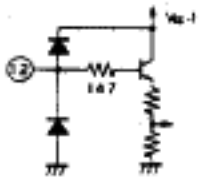
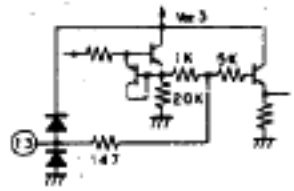
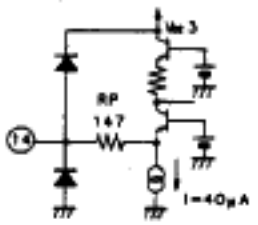
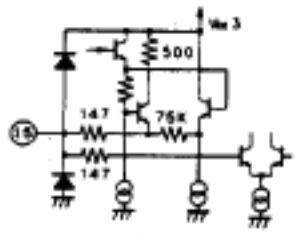
48pin SDIP (Plastic) 600mil 5.1g

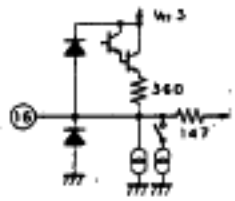
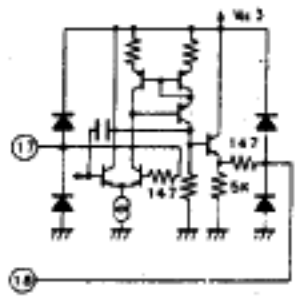
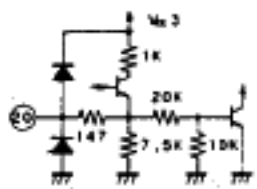
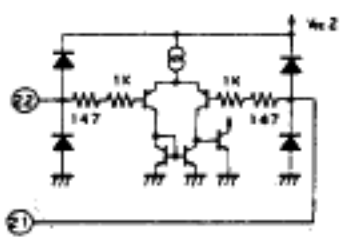
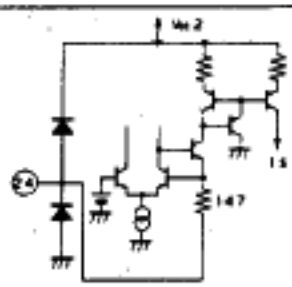


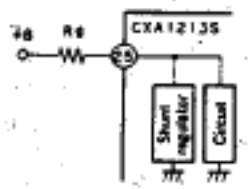
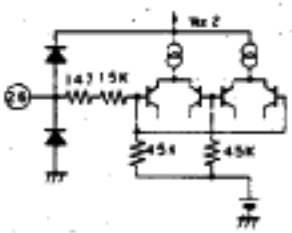
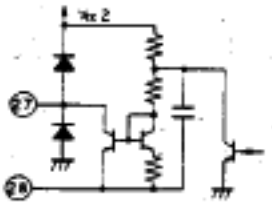
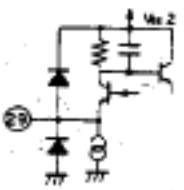
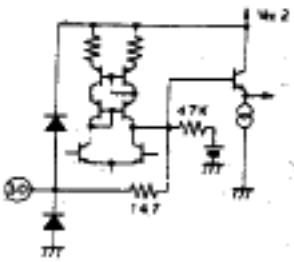
Pin Description

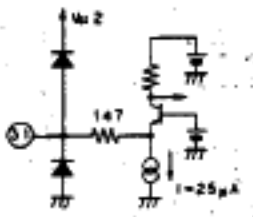
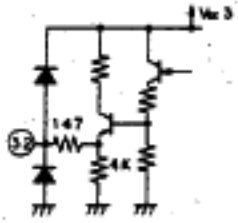
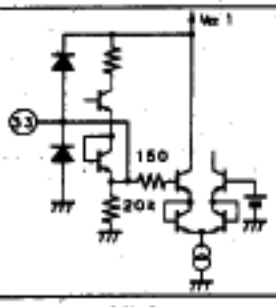
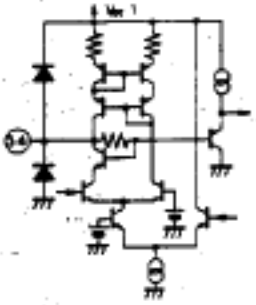
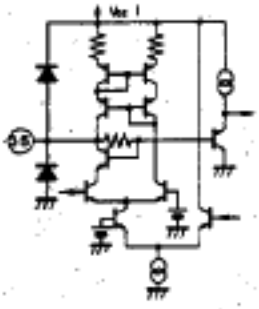
No.	Symbol	Voltage	Equivalent circuit	Description
1	C_{IN}	2.5V		Chroma input pin. Input signal after passing chroma B.P.F via capacitor.
2	ACC	Approx. 5.5V (At Typ. input)		External capacitance pin for ACC control. This pin voltage is to be ACC voltage.
3	C_{OUT}	$\overline{\text{SECAM}}$: 5.85V SECAM : 0V		ACC and chroma output pin after passing color control circuit. Pin voltage varies by SECAM/$\overline{\text{SECAM}}$. At $\overline{\text{SECAM}}$: $5.85V_{DC}$ At SECAM: $0V_{DC}$
4	PHASE	4.5V		Phase control voltage input pin for PAL this pin is also applicable to forced killer input. killer output and f_{SC} free run adjustment mode. V_{DD} : Forced fsc free run adjustment 2 to 8V: Phase control GND : Forced killer input or killer output
5	U	—		U signal input pin after separating C_{OUT} signal at Pin 3 to U and V by using 1H Delay Line.

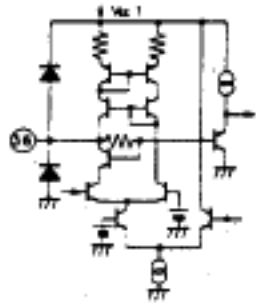
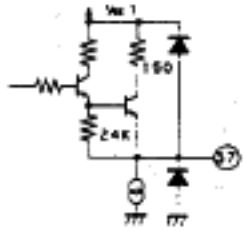
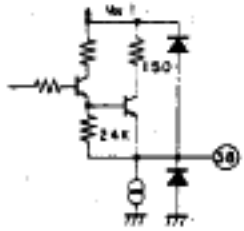
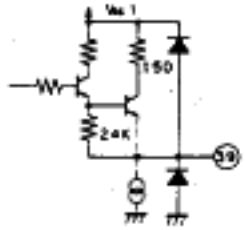
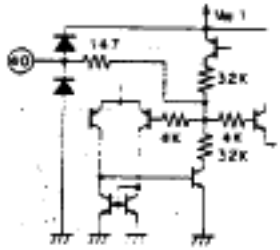
No.	Symbol	Voltage	Equivalent circuit	Description
6	V	—		V signal input pin after separating C_{OUT} signal at Pin 3 to U and V by using 1H Delay Line.
7	APC	6.7V		Lag lead filter pin for APC
8	X4			4.43MHz crystal pin for chroma VCO
9	3/4	At 3.58MHz output: 5.5V AT 4.43MHz output: GND		Discrimination output pin of VCO oscillation frequency. High level(5.5V) at oscillation frequency 3.58MHz, Low level at oscillation frequency 4.43MHz. Also input pin applicable: Forced 3.58MHz at mode H and 4.43MHz at mode L. Repeats H and L every 5 Vertical section at killer mode.
10	×3			3.58MHz crystal pin for chroma VCO.

No.	Symbol	Voltage	Equivalent circuit	Description
11	S/$\overline{S}$	—		SECAM/$\overline{SECAM}$ input pin. Input high voltage over 2.7V at SECAM and low voltage under 0.3V at $\overline{SECAM}$.
12	N/P	—		NTSC/PAL input pin. Input low voltage under 0.3V at PAL and high voltage over 3.0V at NTSC.
13	60/50	At 50Hz: 0V At 60Hz: 4V		Discrimination output pin of vertical frequencies 50Hz and 60Hz. Also input pin applicable: Forced 60Hz mode at V_{CC}, Forced 50Hz mode at GND.
14	V_{IN}			Input pin for vertical sync separation. Slice level is decided by internal constant current of 40μA and protection resistance R_P and external resistance. Video signal is input at 2Vp-p.
15	VPH	3.35V		Pin to detect slice level to take out V.sync peak of sync separation output is detected at this pin. Connect Capacitor or Capacitor and Resistance between GNDs for external fixing.

No.	Symbol	Voltage	Equivalent circuit	Description
16	VRAMP			Generates saw tooth wave for vertical deflection. Use the external capacitance which holds a stable temperature characteristics.
17	VNF	—		Feedback pin for vertical deflection. This is compared to saw tooth wave generated at Pin 16 with comparator and obtains almost the same waveform as internal saw tooth wave.
18	VD			Pin which outputs the difference of comparison between feedback waveform at Pin 17 and internal saw tooth wave.
19	V_{CC3}	9V		Power supply pin for vertical drive circuit. This supplies a stable 9V voltage.
20	BG			Burst gate pulse is output. Artificial H.sync is supplied instead of H.sync when AFC is not locked like at no signal. and it outputs approx. 4μs width pulse.
21	REF	—		Pins 21 and 22 are the pins to detect over voltage and to make it hold down. This supplies reference voltage to Pin 21 and high voltage detection output to Pin 22.
22	HV	—		
23	GND2	0V		GND pin for Jungle.
24	IS	2.1V		Pin to generate the reference current to be used at internal IC. Use the external resistance at 27kΩ which holds a stable temperature characteristics since the reference current is 80μA.

No.	Symbol	Voltage	Equivalent circuit	Description
25	V_{CC2}	9V		Power supply pin for horizontal drive circuit. Shunt regulator provided inside and it regulates to 9V. Since the current flowed into is approx. 15mA.the Rg value is obtained by the following formula when +B is +115V. $Rg=\frac{(115-9)V}{15mA}=7.07\rightarrow 6.8k\Omega$
26	HP	4.3V		FBP input pin and inputs it via capacitor.
27	HD			Horizontal drive output pin and open collector output. Drive pulse width is 24μs constant.
28	GND3	0V		Horizontal drive GND pin.
29	VCO			Connect ceramic oscillator for $32f_H$ VCO and dumping resistance. CSB500F2 for ceramic oscillator and 470Ω for dumping resistance are recommended.
30	AFC	5.2V		Pin that connects AFC loop filter.

No.	Symbol	Voltage	Equivalent circuit	Description
31	H_{IN}	2.3V		Input pin for H.sync separator. The form of circuit is the same as V.sync separator,however,set the slice level lower and time constant shorter than V.sync Separator when H. sync separator.
32	S_{sync}			Outputs sync pulled out in H.sync Separator circuit.
33	C BLK			C BLK output pin and BLK signal input pin. BLK input is ON: over 2.5V at H. OFF: under 0.3V at L. Input in emitter follower circuit at input pin.
34	B CLP	6.2V		External Capacitor pin for B-Y signal color clamp. Also B-Y signal input pin of SECAM.
35	R CLP	6.2V		External Capacitor pin for R-Y signal color clamp. Also R-Y signal input pin of SECAM.

No.	Symbol	Voltage	Equivalent circuit	Description
36	G CLP	6.2V		External Capacitor pin for G-Y signal color clamp.
37	B_{OUT}			B signal output pin.
38	G_{OUT}			G signal output pin.
39	R_{OUT}			R signal output pin.
40	D. PIC	4V		External Resistance and Capacitor pin for black peak hold of New Dynamic Picture. Connect this pin to GND at 10kΩ when you want New Dynamic Picture OFF.