



8 OUTPUT CLOCK GENERATOR

IDT5V928

FEATURES:

- 3V to 3.6V operating voltage
- 50MHz to 160MHz output frequency range
- Input from fundamental crystal oscillator or external source
- Internal PLL feedback (loading feedback output relative to other outputs, adjusts propagation delay between REF inputs and outputs)
- Select inputs (S[1:0]) for FB divide selection (multiply ratio of 2, 3, 4, 4.25, 5, 6, 6.25, and 8)
- Low jitter
- PLL bypass for testing and power-down control (S1 = H, S0 = H, powers part down <math><500\mu A</math>)
- Available in TSSOP package

APPLICATIONS:

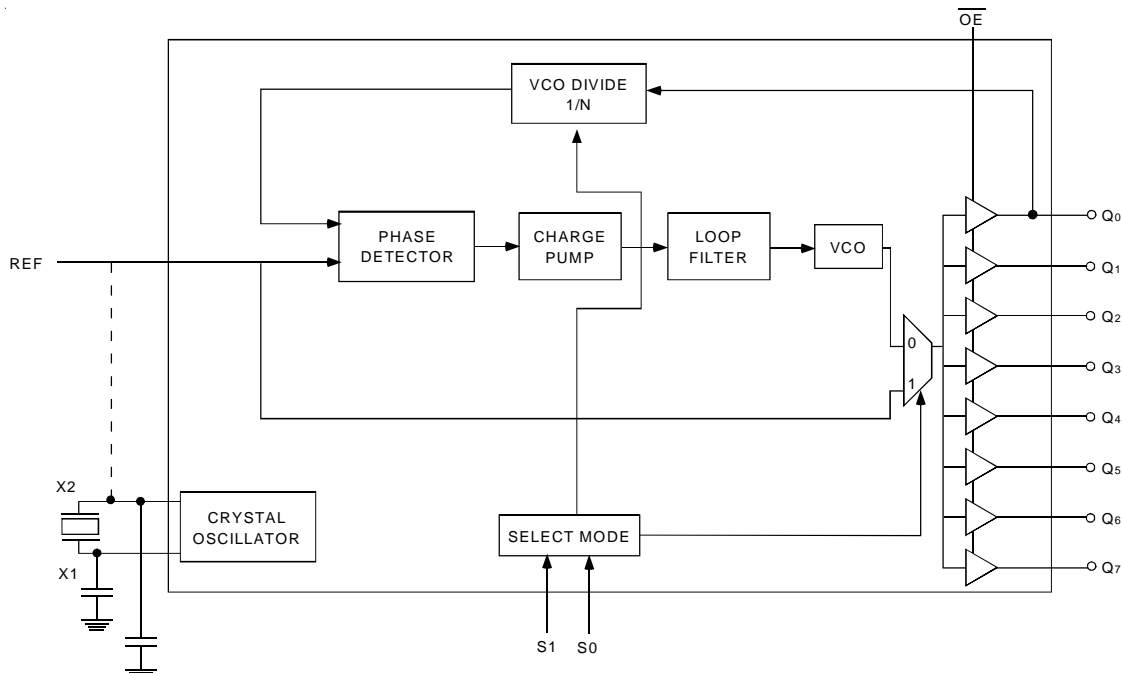
- Gigabit ethernet
- Router
- Network switches
- SAN
- Instrumentation
- Fibre channel

DESCRIPTION:

The IDT5V928 is a low-cost, low skew, low jitter, and high-performance clock synthesizer. It has been specially designed to interface with Gigabit Ethernet (125MHz), Fibre Channel (106.25MHz), and OC-3 (155.52MHz) applications. It can be programmed to provide output frequencies ranging from 50MHz to 160MHz, with input frequencies ranging from 6.25MHz to 80MHz.

The IDT5V928 includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the chip accepts a 10 - 40MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω.

FUNCTIONAL BLOCK DIAGRAM

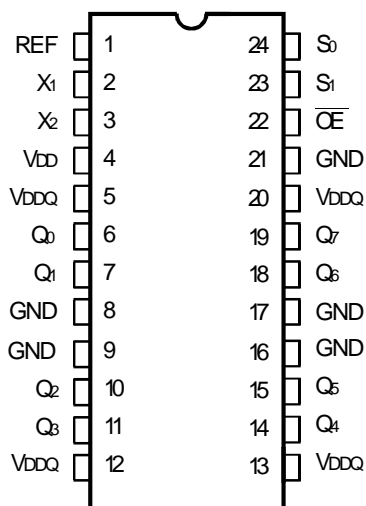


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

FEBRUARY 2003

PIN CONFIGURATION



TSSOP
TOP VIEW

CRYSTAL SPECIFICATION

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. Crystal tuning capacitors should be connected from X₂/REF to GND and from X₁ to GND.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{DD} /V _{DDQ}	Supply Voltage to Ground	-0.5 to +4.6	V
V _I	Input Voltage	-0.5 to +4.6	V
I _O	Output Current	±50	mA
T _{STG}	Storage Temperature	-65 to +150	°C
T _J	Junction Temperature	150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Name	Type	Description
S[1:0]	I	Three level divider/mode select pins. Float to MID.
\overline{OE}	I	Output enable bar. \overline{OE} has a pull-down. Output Q[1:7] tristated when HIGH. Output Q ₀ remains running when in PLL mode and tri-states when in TEST mode.
X ₁	I	Crystal oscillator input. Connect to GND if oscillator not required.
X ₂	I	Crystal oscillator output. Leave unconnected for clock input.
REF	I	Input clock. Connect to X ₂ if crystal oscillator is used.
Q[1:7]	O	Output at N*REF frequency
Q ₀	O	Output at N*REF internally connected for PLL feedback
V _{DDQ}	PWR	Power supply for the device outputs. Connect to V _{DD} on PCB.
V _{DD}	PWR	Power supply for the device core and inputs. Connect to V _{DD} on PCB.
GND	PWR	Ground supply

DIVIDE SELECTION TABLE⁽¹⁾

S ₁	S ₀	Divide-by-N Value	Mode
L	L	2	PLL
L	M	3	PLL
L	H	4	PLL
M	L	4.25	PLL
M	M	5	PLL
M	H	6	PLL
H	L	6.25	PLL
H	M	8	PLL
H	H	TEST	TEST ⁽²⁾

NOTES:

- H = HIGH
M = MEDIUM
L = LOW
- Test mode for low frequency testing. In this mode, REF clock bypasses the VCO (VCO powered down) and the crystal oscillator is powered down.

COMMON OUTPUT FREQUENCY EXAMPLES (MHz)

Output	50	60	64	72	75	80	90	100
Input	25	10	16	12	25	10	15	20
FB Divide Selection S[1:0]	LL	MH	LH	MH	LM	HM	MH	MM

Output	106.25	106.25	120	125	125	125	150	155.52
Input	17	25	15	20	25	62.5	25	19.44
FB Divide Selection S[1:0]	HL	ML	HM	HL	MM	LL	MH	HM

OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD} /V _{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T _A	Operating Temperature	-40	25	+85	°C
C _L	Output Load Capacitance	—	—	15	pF
C _{IN}	Input Capacitance, OE, F = 1MHz, V _{IN} = 0V, T _A = 25°C	—	5	7	pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: T_A = -40°C to +85°C, V_{DD}/V_{DDQ} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V _{IL}	Input LOW Voltage		—	—	0.8	V
V _{IH}	Input HIGH Voltage		2	—	—	V
V _{IHH}	Input HIGH Voltage	3-level input only	V _{DD} - 0.6	—	—	V
V _{IMM}	Input MID Voltage	3-level input only	V _{DD} /2 - 0.3	—	V _{DD} /2 + 0.3	V
V _{ILL}	Input LOW Voltage	3-level input only	—	—	0.6	V
I _{IN}	Input Leakage Current (REF input only)	V _{IN} = V _{DD} or GND, V _{DD} = Max.	-5	—	+5	μA
I ₃	3-Level Input DC Current, S[1:0]	V _{IN} = V _{DD} HIGH Level	—	—	+200	μA
		V _{IN} = V _{DD} /2 MID Level	-50	—	+50	
		V _{IN} = GND LOW Level	-200	—	—	
I _{IH}	Input HIGH Current	V _{IN} = V _{DD}	—	—	100	μA
V _{OL}	Output LOW Voltage	I _{OL} = 12mA	—	—	0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = -12mA	2.4	—	—	V

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max	Unit
I _{DD_PD}	Power Down Current	V _{DD} = Max. S _[1:0] = HH \overline{OE} = L; REF = L; X1 = L All outputs unloaded	—	—	500	μA
ΔI _{DD}	Supply Current per Input	V _{DD} = Max., V _{IN} = 3V	—	—	30	μA
I _{DD}	Dynamic Supply Current	V _{DD} = 3.6V S _[1:0] = LL \overline{OE} = L F _{OUT} = 150MHz All outputs unloaded	—	—	130	mA

NOTE:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
t _R , t _F	Rise Time, Fall Time	0.8V to 2V	—	0.7	1.5	ns	
d _T	Output/Duty Cycle	V _T = V _{DDQ} /2	45	50	55	%	
t _{PD}	REF to Q ₀ ⁽¹⁾	V _T = V _{DDQ} /2	f _{OUT} ≥ 100MHz, all N	-200	—	200	ps
			50 < f _{OUT} < 160MHz, N ≤ 4	-200	—	200	
			50 < f _{OUT} < 160MHz, N ≥ 4.25	-350	—	350	
t _{sk}	Output to Output Skew (Q ₀ to Q _{1:7})	Equal loads	—	—	200	ps	
t _j	Cycle - Cycle Jitter	f _{OUT} ≥ 100MHz	-100	—	100	ps	
f _{OUT}	Output Frequency		50	—	160	MHz	

NOTE:

- When using a clock input.

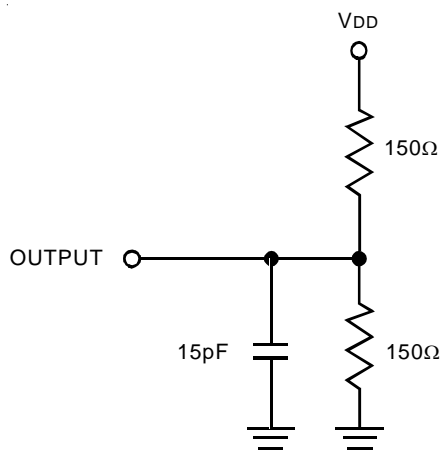
INPUT TIMING REQUIREMENTS

Symbol	Description ⁽¹⁾	Min.	Max.	Unit
t _R , t _F	Maximum input rise and fall time, 0.8V to 2V ⁽²⁾	—	10	ns/V
t _{PWC}	Input clock pulse, HIGH or LOW ⁽²⁾	2	—	ns
D _H	Input duty cycle ⁽²⁾	10	90	%
f _{OSC}	XTAL oscillator frequency	—	40	MHz
f _{IN}	Input frequency ⁽²⁾	50/N	160/N	MHz

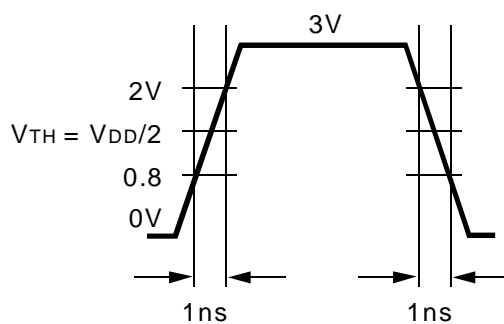
NOTES:

- Where pulse width implied by D_H is less than the t_{PWC} limit, t_{PWC} limit applies.
- When using a clock input.

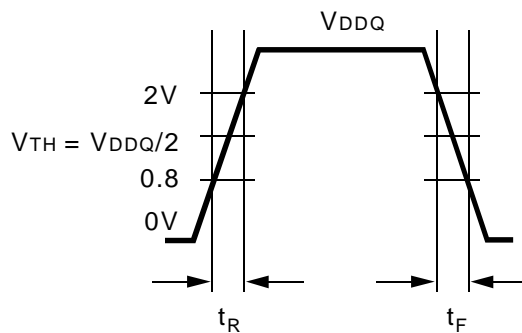
AC TEST LOADS AND WAVEFORMS



AC Test Load

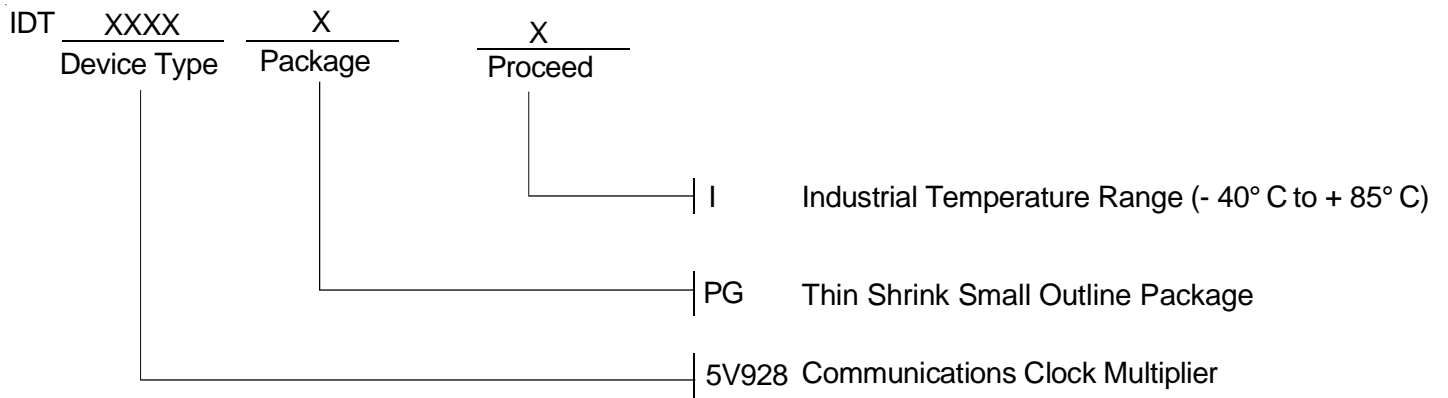


Input Test Waveform



Output Waveform

ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
logichelp@idt.com
(408) 654-6459