

# Timer

# NE/SA/SE555/SE555C

## DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

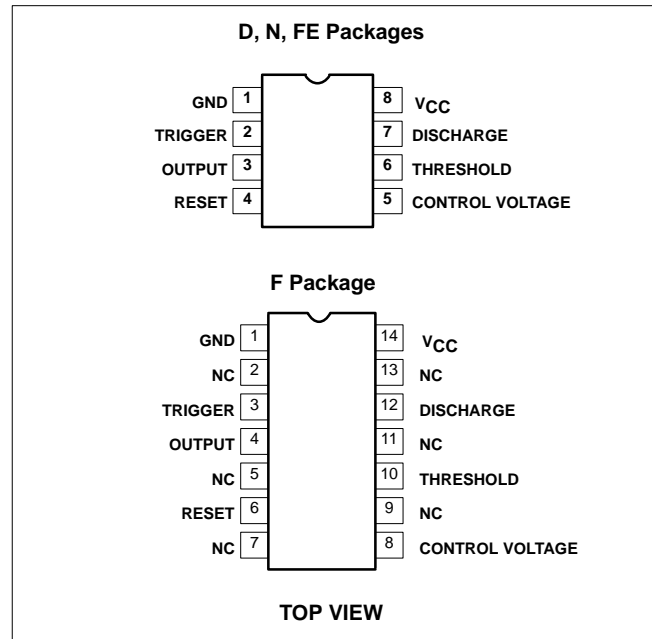
## FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

## APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

## PIN CONFIGURATIONS



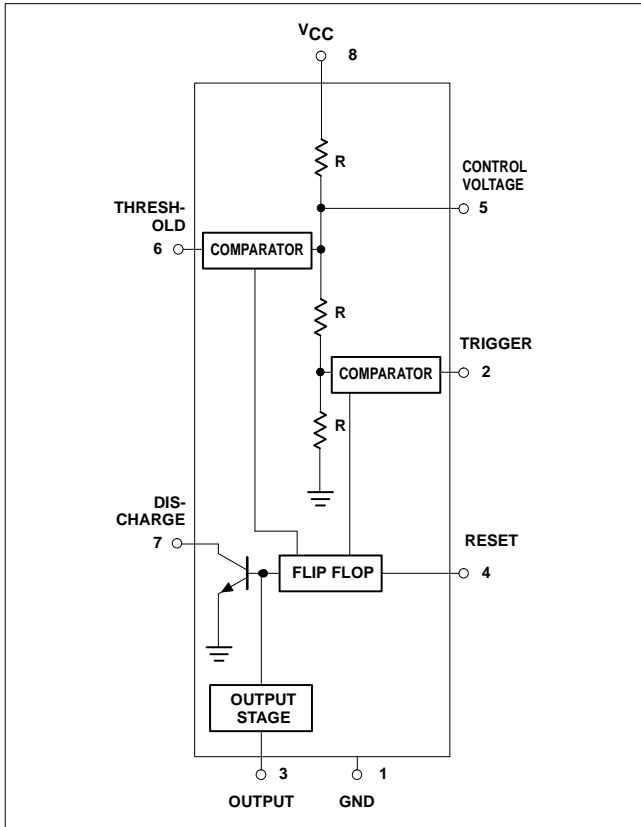
## ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

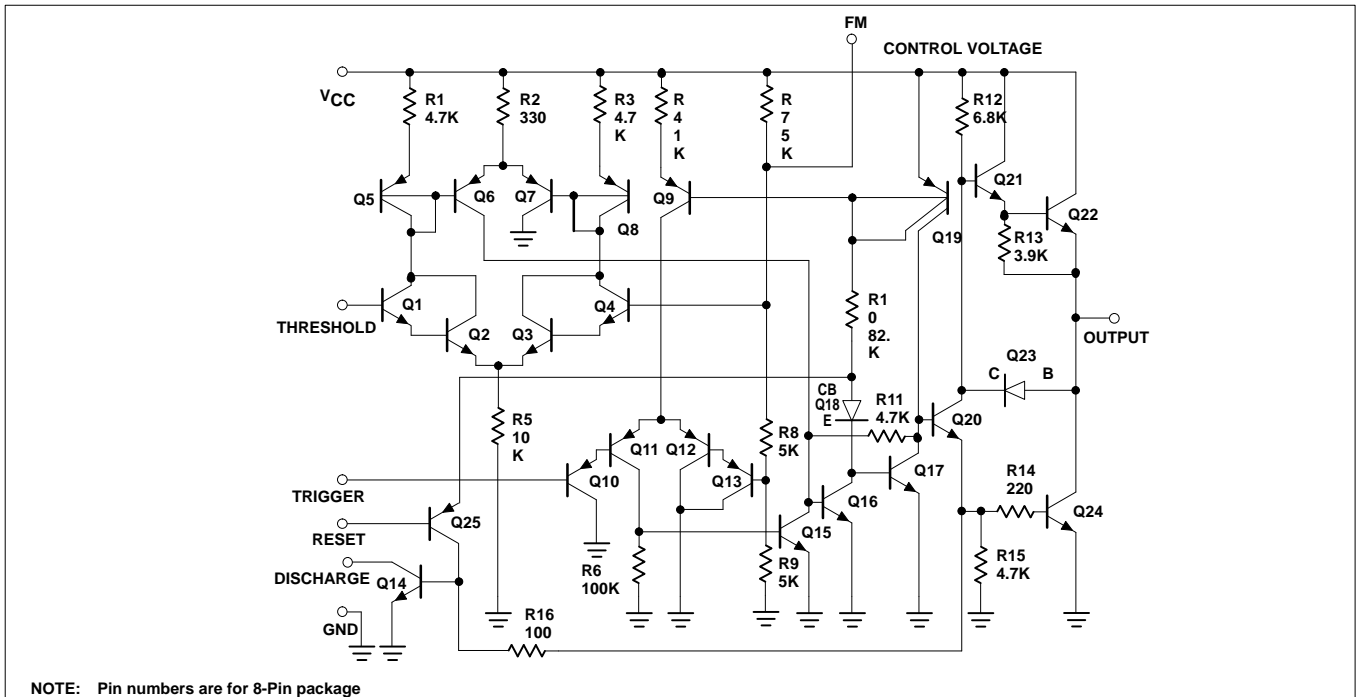
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BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



## Timer

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**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P <sub>D</sub>	Maximum allowable power dissipation <sup>1</sup>	600	mW
T <sub>A</sub>	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C
T <sub>SOLD</sub>	Lead soldering temperature (10sec max)	+300	°C

**NOTES:**

- The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:

D package 160°C/W  
 FE package 150°C/W  
 N package 100°C/W  
 F package 105°C/W

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**DC AND AC ELECTRICAL CHARACTERISTICS**

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15$  unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	Supply voltage		4.5		18	4.5		16	V
$I_{CC}$	Supply current (low state) <sup>1</sup>	$V_{CC}=5\text{V}$ , $R_L=\infty$ $V_{CC}=15\text{V}$ , $R_L=\infty$		3 10	5 12		3 10	6 15	mA mA
$t_M$ $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy <sup>2</sup> Drift with temperature Drift with supply voltage	$R_A=2\text{k}\Omega$ to $100\text{k}\Omega$ $C=0.1\mu\text{F}$		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 150 0.5	% ppm/ $^\circ\text{C}$ %/V
$t_A$ $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy <sup>2</sup> Drift with temperature Drift with supply voltage	$R_A, R_B=1\text{k}\Omega$ to $100\text{k}\Omega$ $C=0.1\mu\text{F}$ $V_{CC}=15\text{V}$		4 0.15	6 500 0.6		5 0.3	13 500 1	% ppm/ $^\circ\text{C}$ %/V
$V_C$	Control voltage level	$V_{CC}=15\text{V}$ $V_{CC}=5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
$V_{TH}$	Threshold voltage	$V_{CC}=15\text{V}$ $V_{CC}=5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
$I_{TH}$	Threshold current <sup>3</sup>			0.1	0.25		0.1	0.25	$\mu\text{A}$
$V_{TRIG}$	Trigger voltage	$V_{CC}=15\text{V}$ $V_{CC}=5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
$I_{TRIG}$	Trigger current	$V_{TRIG}=0\text{V}$		0.5	0.9		0.5	2.0	$\mu\text{A}$
$V_{RESET}$	Reset voltage <sup>4</sup>	$V_{CC}=15\text{V}$ , $V_{TH}=10.5\text{V}$	0.3		1.0	0.3		1.0	V
$I_{RESET}$	Reset current Reset current	$V_{RESET}=0.4\text{V}$ $V_{RESET}=0\text{V}$		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
$V_{OL}$	Output voltage (low)	$V_{CC}=15\text{V}$ $I_{SINK}=10\text{mA}$ $I_{SINK}=50\text{mA}$ $I_{SINK}=100\text{mA}$ $I_{SINK}=200\text{mA}$ $V_{CC}=5\text{V}$ $I_{SINK}=8\text{mA}$ $I_{SINK}=5\text{mA}$		0.1 0.4 2.0 2.5 0.1 0.05	0.15 0.5 2.2 2.5 0.25 0.2		0.1 0.4 2.0 2.5 0.3 0.25	0.25 0.75 2.5 V 0.4 0.35	V V V V V V
$V_{OH}$	Output voltage (high)	$V_{CC}=15\text{V}$ $I_{SOURCE}=200\text{mA}$ $I_{SOURCE}=100\text{mA}$ $V_{CC}=5\text{V}$ $I_{SOURCE}=100\text{mA}$	13.0 3.0	13.3 3.3		12.75 2.75	13.3 3.3		V V V
$t_{OFF}$	Turn-off time <sup>5</sup>	$V_{RESET}=V_{CC}$		0.5	2.0		0.5	2.0	$\mu\text{s}$
$t_R$	Rise time of output			100	200		100	300	ns
$t_F$	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

**NOTES:**

1. Supply current when output high typically 1mA less.

2. Tested at  $V_{CC}=5\text{V}$  and  $V_{CC}=15\text{V}$ .

3. This will determine the max value of  $R_A+R_B$ , for 15V operation, the max total  $R=10\text{M}\Omega$ , and for 5V operation, the max. total  $R=3.4\text{M}\Omega$ .

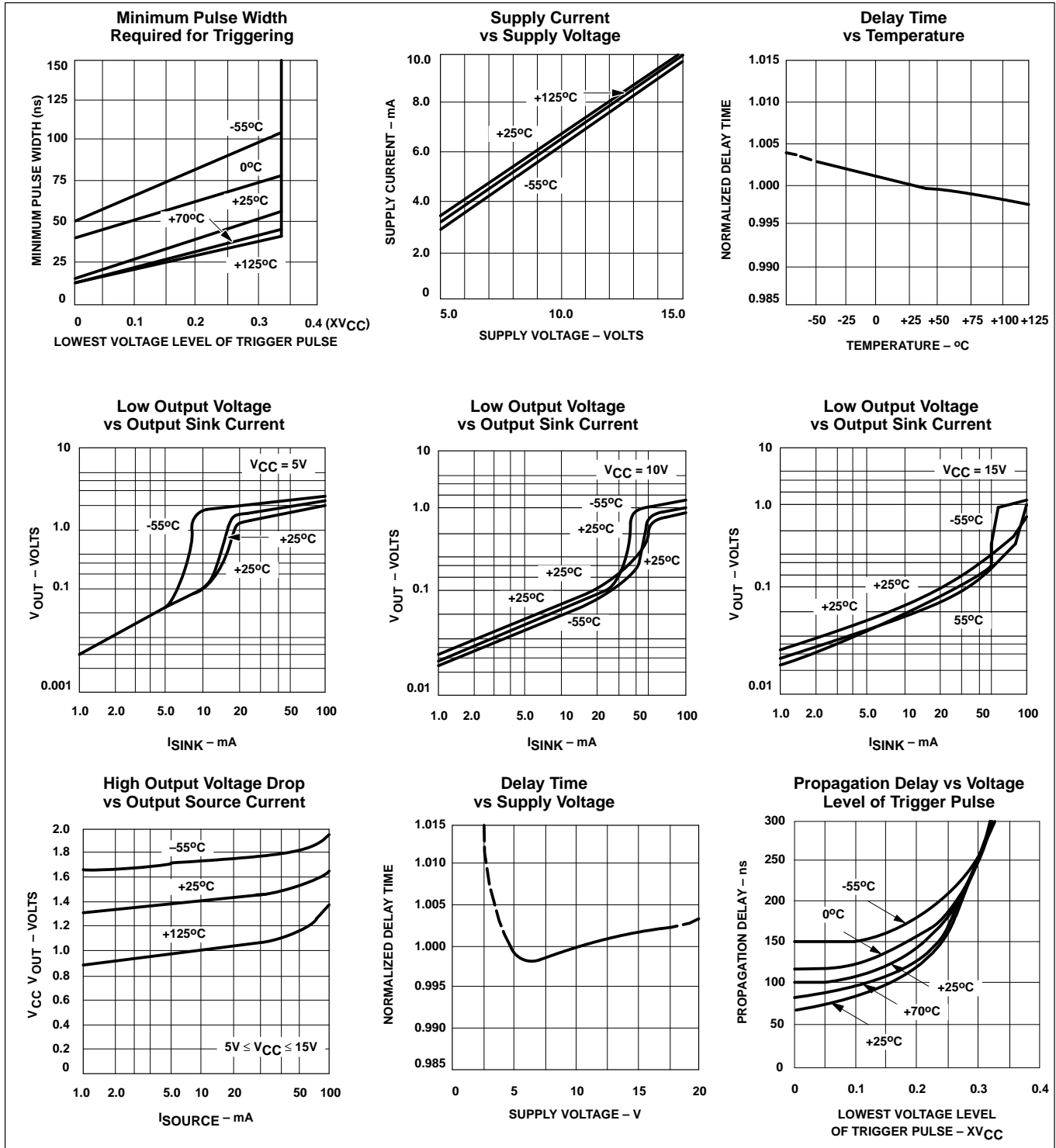
4. Specified with trigger input high.

5. Time measured from a positive going input pulse from 0 to  $0.8 \times V_{CC}$  into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

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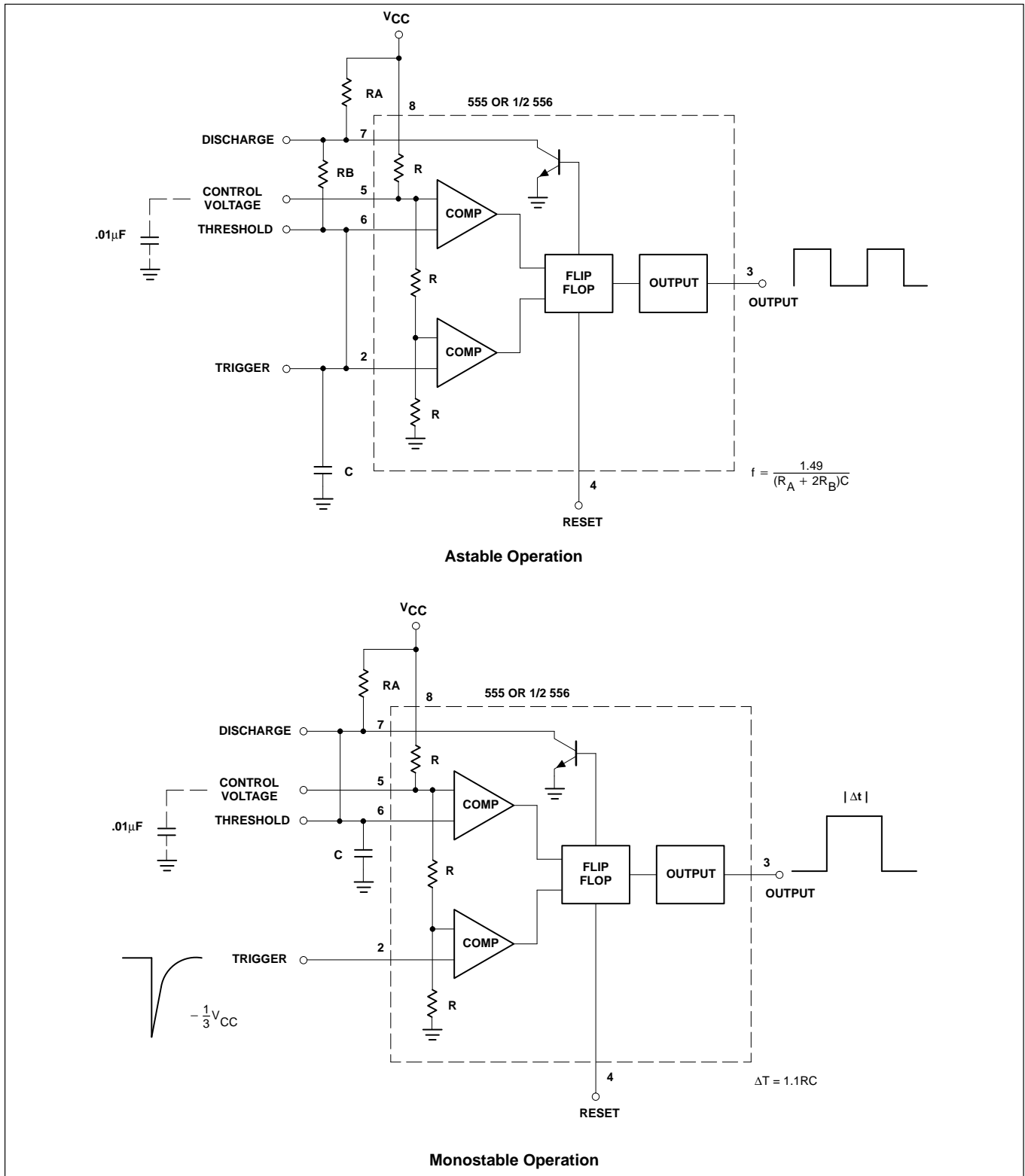
TYPICAL PERFORMANCE CHARACTERISTICS



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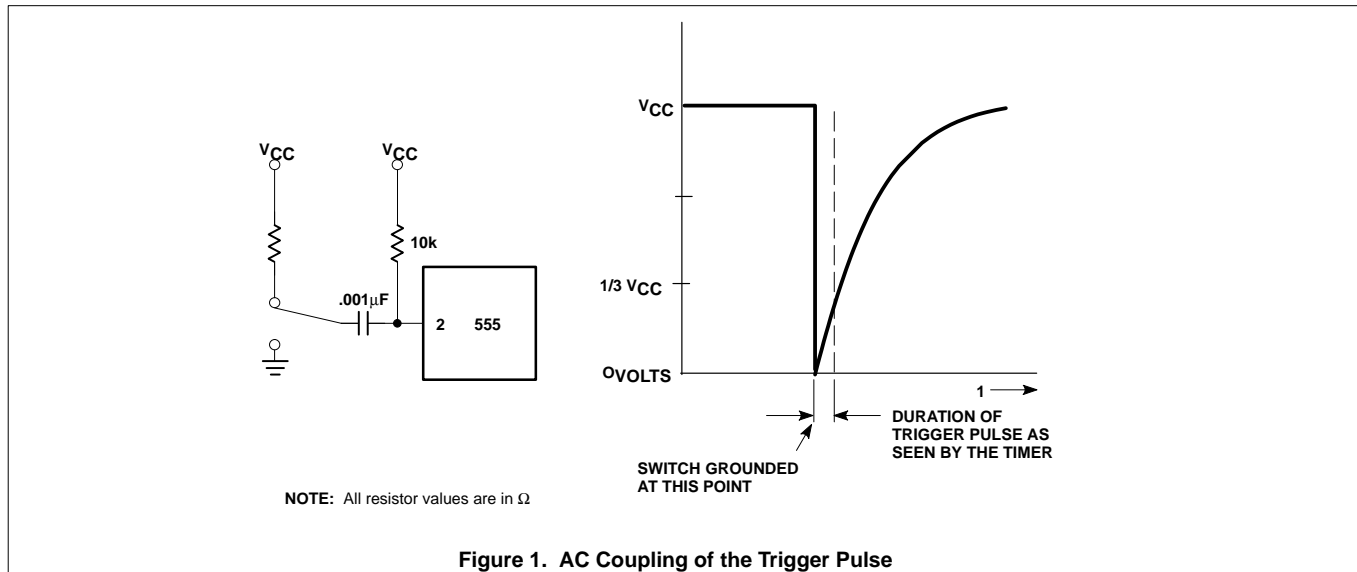
TYPICAL APPLICATIONS



## Timer

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## TYPICAL APPLICATIONS



### Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of  $Q_{15}$  on the base of  $Q_{16}$ , controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches  $2/3 V_{CC}$  to turn the output low. To explain further,  $Q_1$  at the threshold input turns on after reaching  $2/3 V_{CC}$ , which then turns on  $Q_5$ , which turns on  $Q_6$ . Current from  $Q_6$  turns on  $Q_{16}$  which turns  $Q_{17}$  off. This allows current from  $Q_{19}$  to turn on  $Q_{20}$  and  $Q_{24}$  to give an output low. These steps cause the  $2\mu s$  max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low,  $Q_{10}$  is on and turns on  $Q_{11}$  which turns on  $Q_{15}$ .  $Q_{15}$  turns off  $Q_{16}$  and allows  $Q_{17}$  to turn on. This turns off current to  $Q_{20}$  and  $Q_{24}$ , which results in output high. When the trigger is released,  $Q_{10}$  and  $Q_{11}$  shut off,  $Q_{15}$  turns off,  $Q_{16}$  turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.