



N-Channel 80-V (D-S) MOSFET

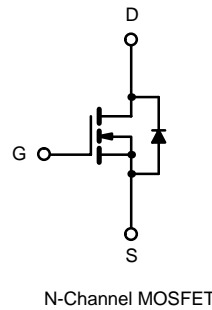
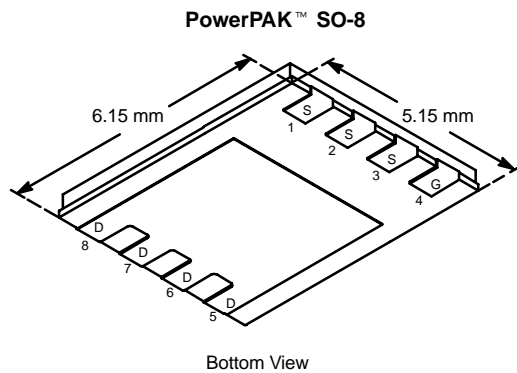
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.0165 @ $V_{GS} = 10$ V	12.5
	0.022 @ $V_{GS} = 6$ V	10.9

FEATURES

- TrenchFET® Power MOSFETS
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

APPLICATIONS

- Primary Side Switch for DC/DC Applications



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	80		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	12.5	7.6	A
		$T_A = 70^\circ\text{C}$	10.0	6.1	
Pulsed Drain Current	I_{DM}	50			
Avalanch Current	I_{AS}	40			
Continuous Source Current (Diode Conduction) ^a	I_S	4.7	1.7		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.2	1.9	W
		$T_A = 70^\circ\text{C}$	3.3	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	19	24	$^\circ\text{C/W}$
		Steady State	52	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.5	1.8		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

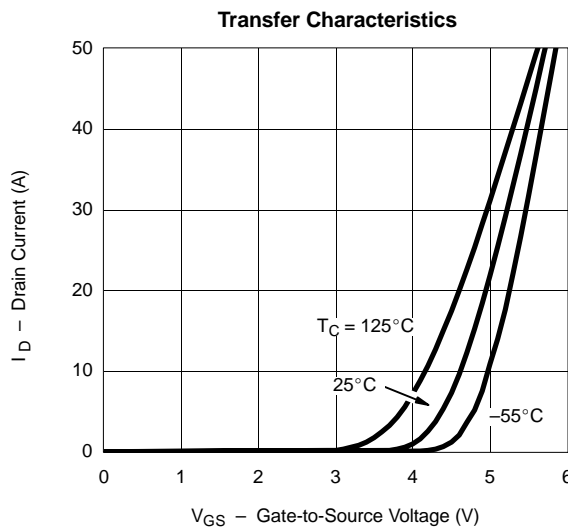
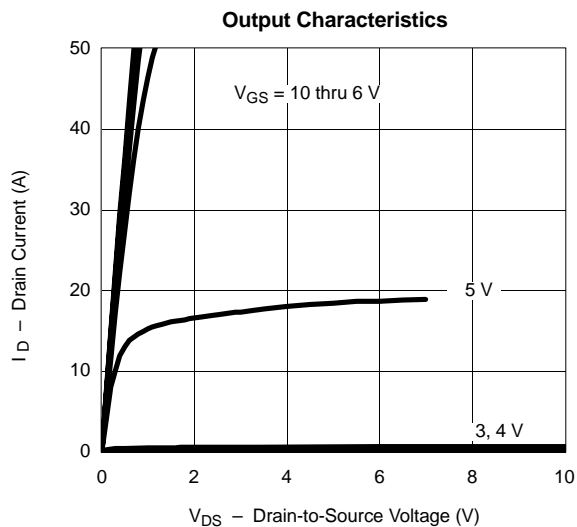
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 64 V, V _{GS} = 0 V			1	μA
		V _{DS} = 64 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 10 A		0.0135	0.0165	Ω
		V _{GS} = 6.0 V, I _D = 8.0 A		0.0175	0.022	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 10 A		25		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.8 A, V _{GS} = 0 V		0.75	1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A		34	41	nC
Gate-Source Charge	Q _{gs}			7.5		
Gate-Drain Charge	Q _{gd}			11.0		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 40 Ω I _D = 1.0 A, V _{GEN} = 10 V, R _G = 6 Ω		17	25	ns
Rise Time	t _r			11	17	
Turn-Off Delay Time	t _{d(off)}			40	60	
Fall Time	t _f			31	45	
Gate Resistance	R _g				0.85	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.8 A, di/dt = 100 A/μs		45	75	ns

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

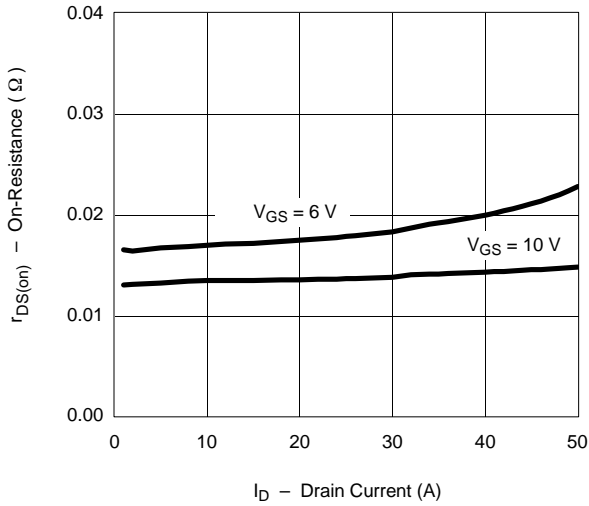
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



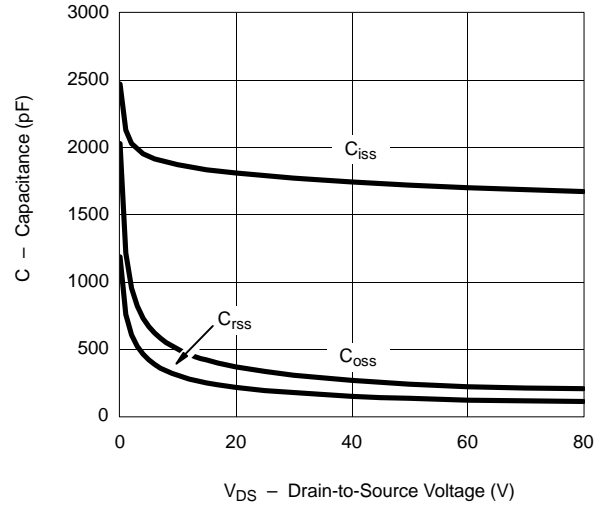


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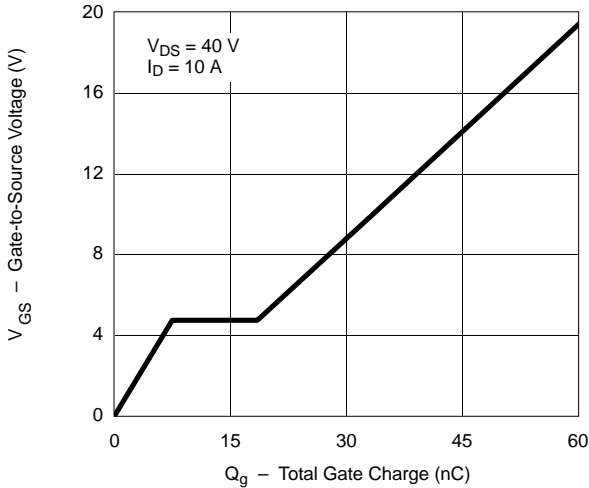
On-Resistance vs. Drain Current



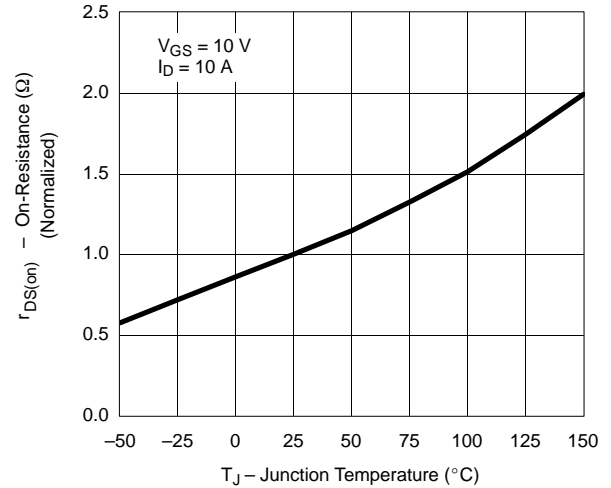
Capacitance



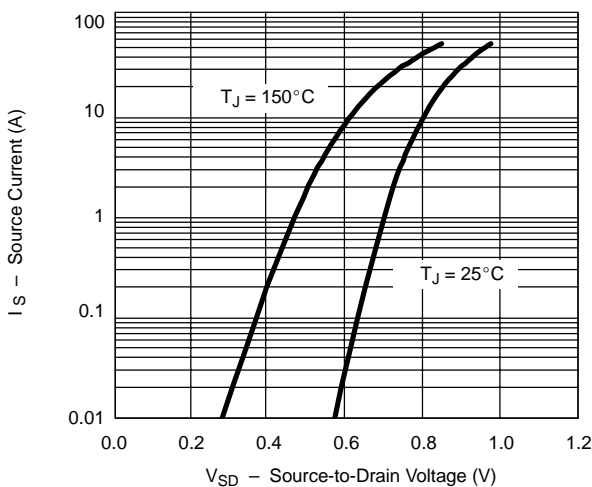
Gate Charge



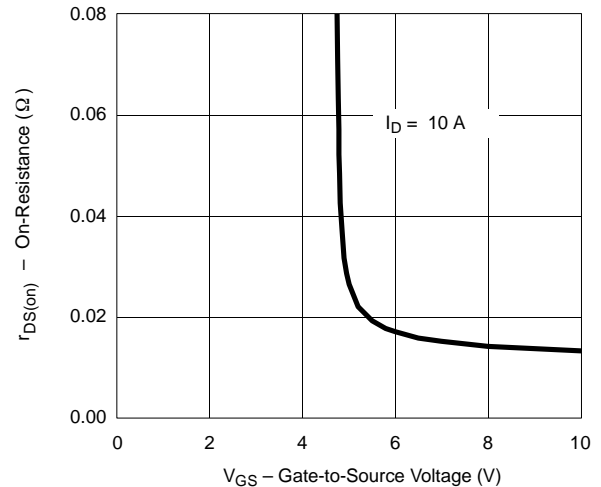
On-Resistance vs. Junction Temperature



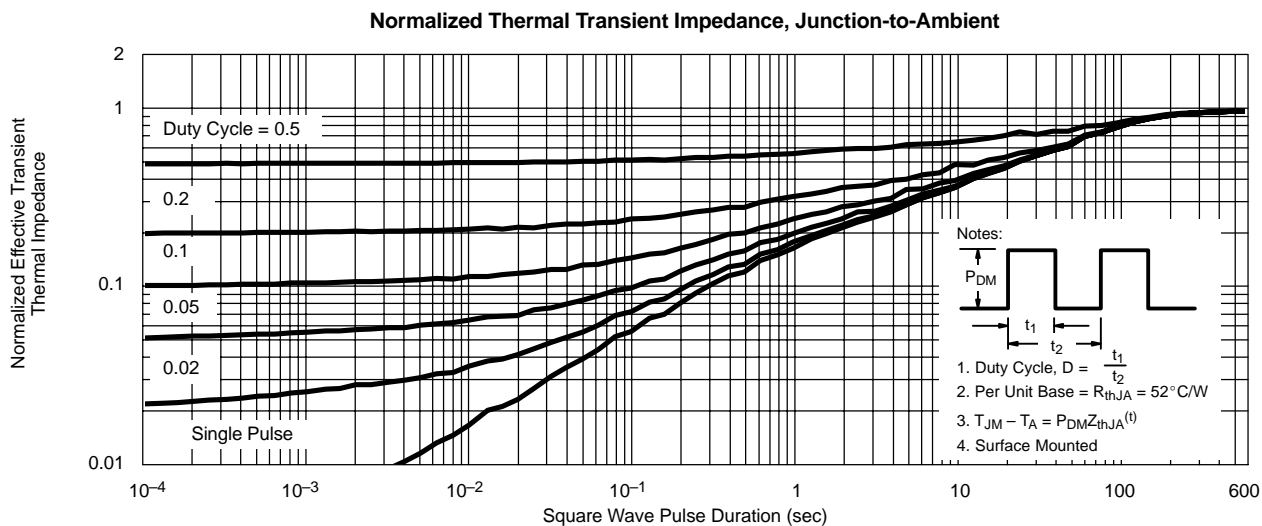
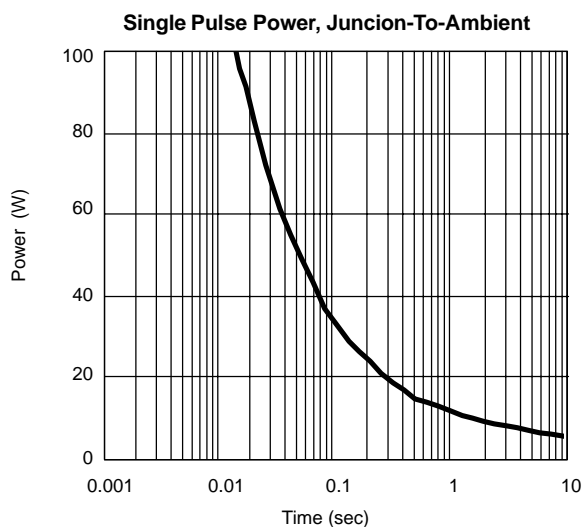
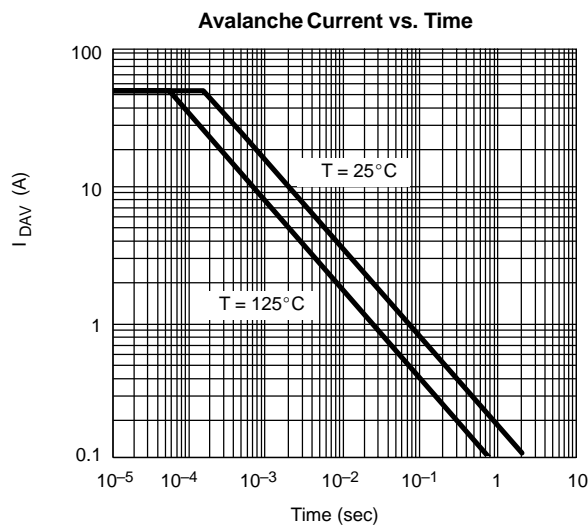
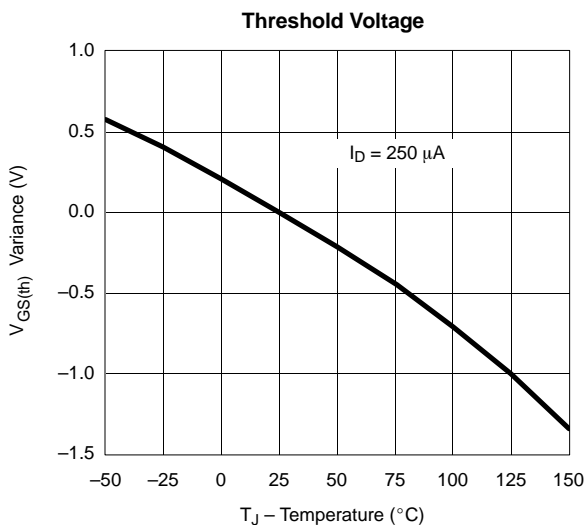
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

