The RF Line

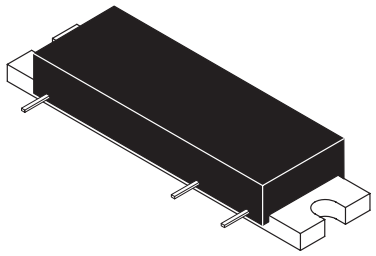
Cellular Band RF Linear LDMOS Amplifier

MHL9318

Designed for ultra–linear amplifier applications in 50 ohm systems operating in the cellular frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for the most demanding analog or digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49 dBm Typ
- Power Gain: 17.5 dB Typ (@ f = 880 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- For Use in TDMA and CDMA Multi–Carrier Applications

3.0 W, 17.5 dB
860–900 MHz
RF LINEAR LDMOS AMPLIFIER



CASE 301AS–01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	–40 to +100	°C
Operating Case Temperature Range	T_C	–20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	560	mA
Power Gain	(f = 880 MHz)	G_p	17	17.5	18.5	dB
Gain Flatness	(f = 860–900 MHz)	G_F	—	0.1	0.2	dB
Power Output @ 1 dB Comp.	(f = 880 MHz)	P_{out} 1 dB	—	35.5	—	dBm
Input VSWR	(f = 860–900 MHz)	$VSWR_{in}$	—	1.2:1	1.5:1	
Output VSWR	(f = 860–900 MHz)	$VSWR_{out}$	—	1.2:1	1.5:1	
Third Order Intercept (f1 = 879 MHz, f2 = 884 MHz)		ITO	47	49	—	dBm
Noise Figure	(f = 960 MHz)	NF	—	3	4.5	dB

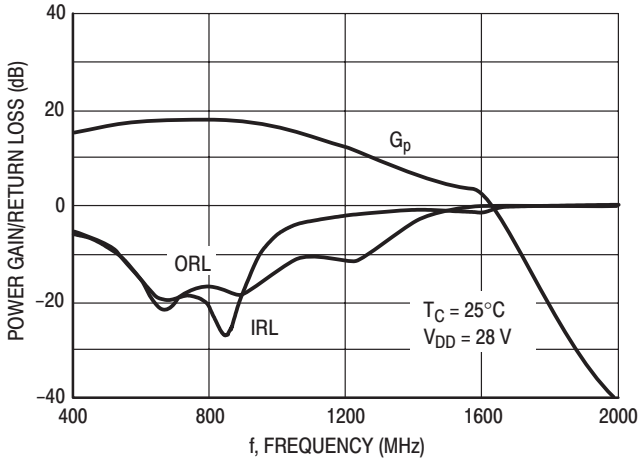


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

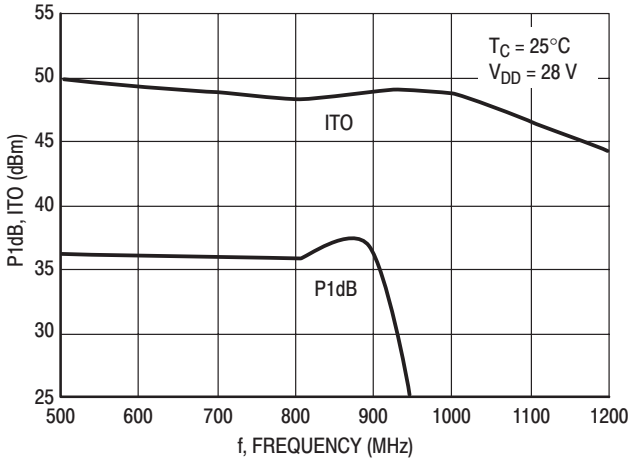


Figure 2. P1dB, ITO versus Frequency

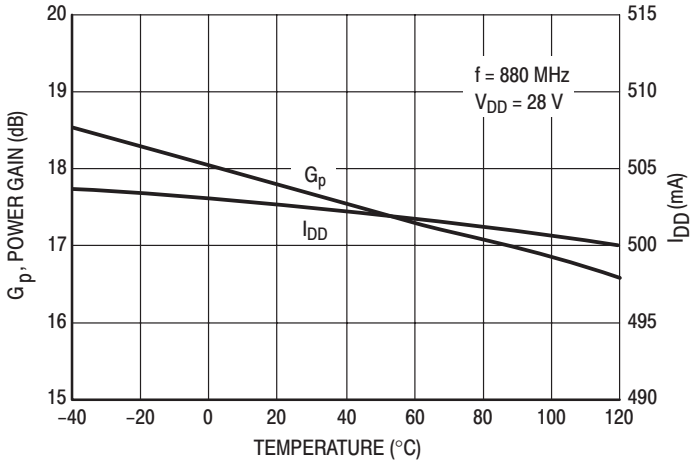


Figure 3. Power Gain, I_{DD} versus Temperature

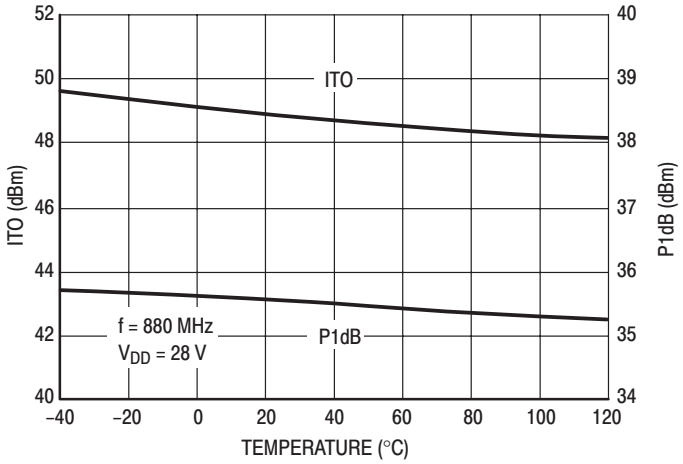


Figure 4. ITO, P1dB versus Temperature

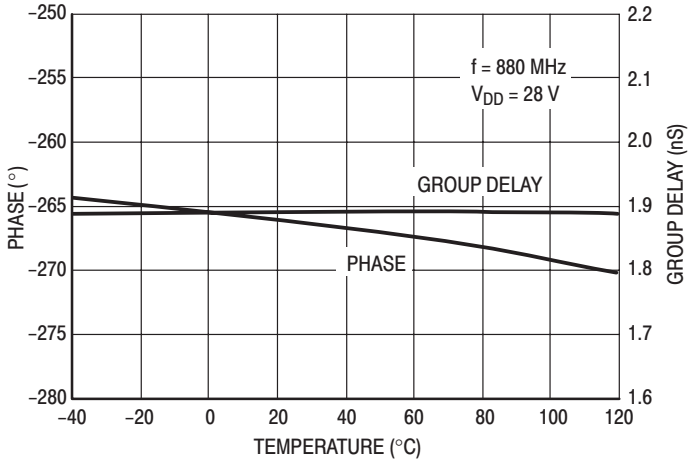


Figure 5. Phase(1), Group Delay(1) versus Temperature

(1)In Production Test Fixture

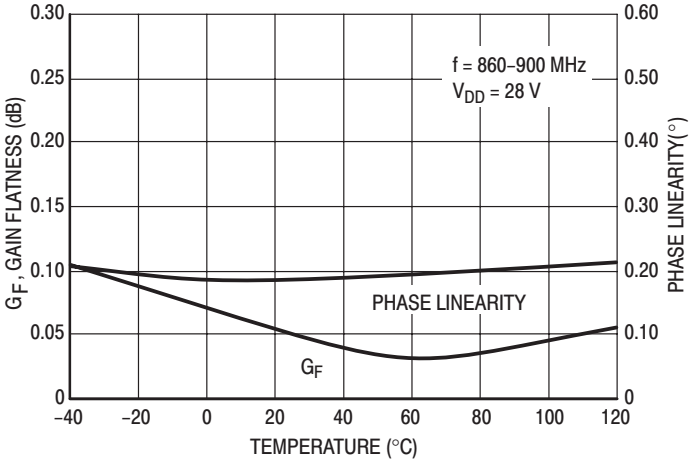


Figure 6. Gain Flatness, Phase Linearity versus Temperature

TYPICAL CHARACTERISTICS

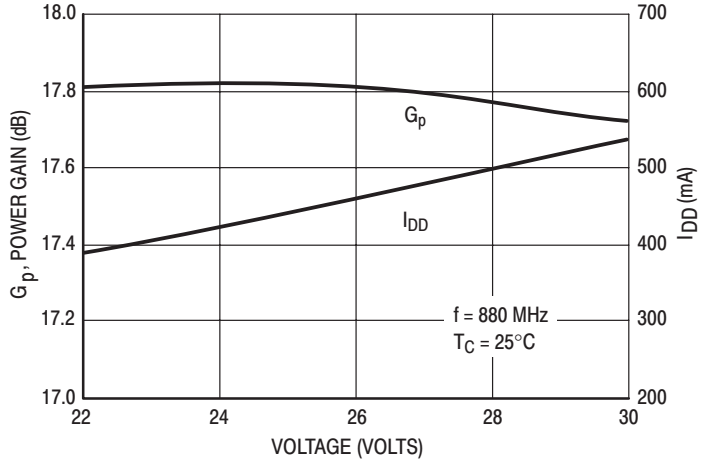


Figure 7. Power Gain, I_{DD} versus Voltage

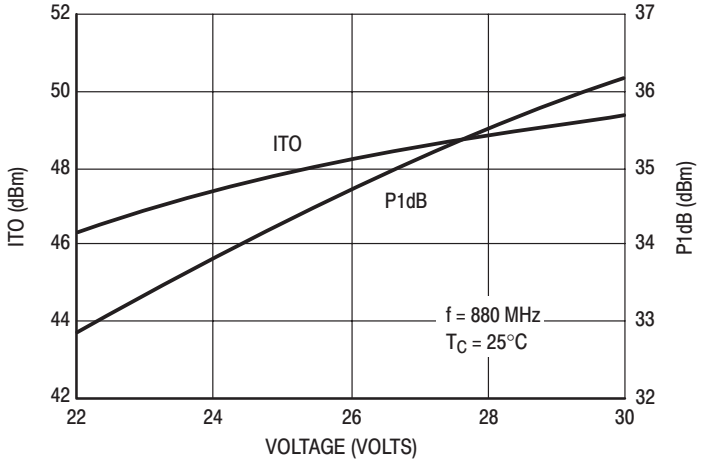


Figure 8. ITO, P1dB versus Voltage

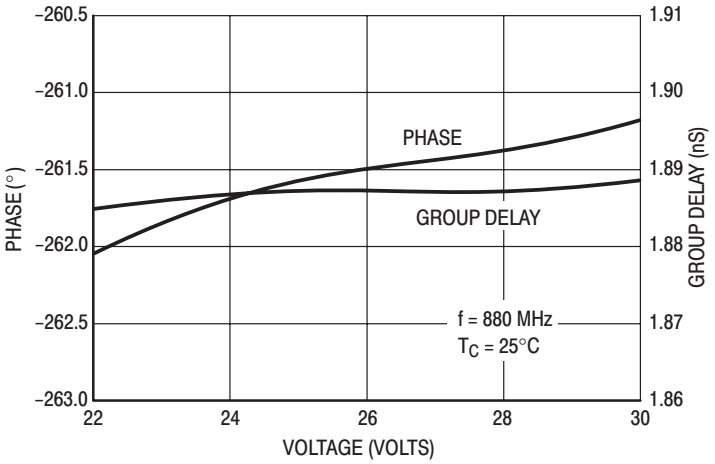


Figure 9. Phase(1), Group Delay(1) versus Voltage

(1)In Production Test Fixture

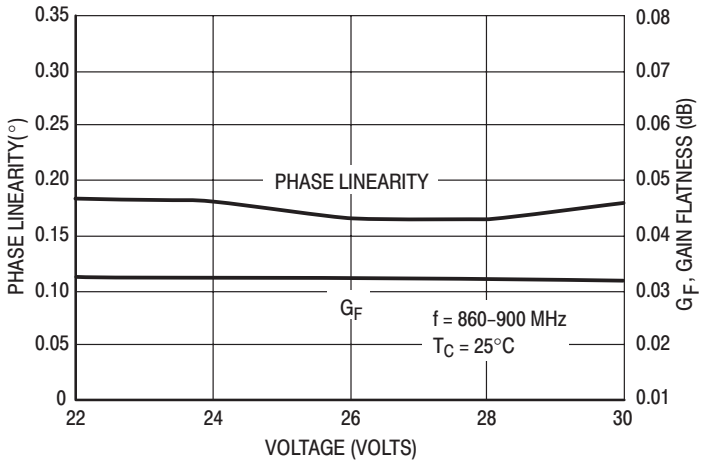
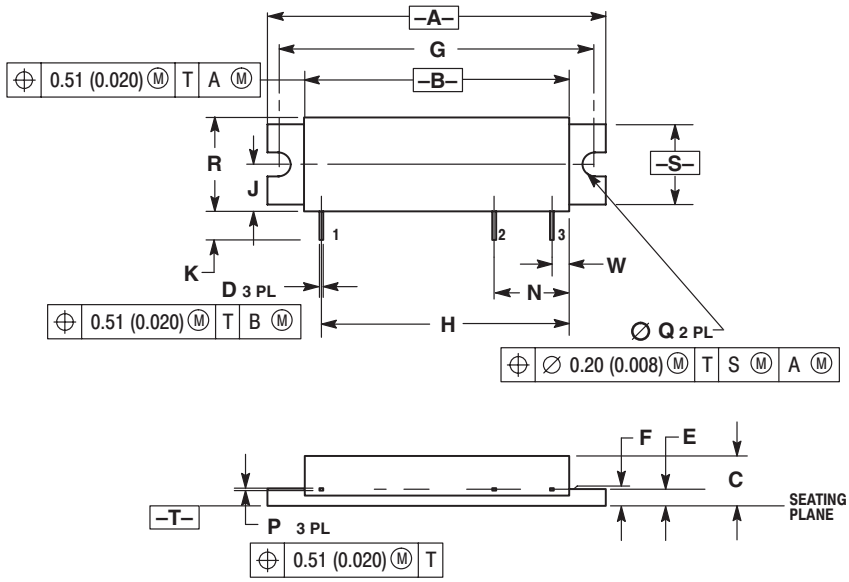


Figure 10. Phase Linearity, Gain Flatness versus Voltage

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD
3. RF OUTPUT
CASE: GROUND

CASE 301AS–01
ISSUE A

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

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