

3875081 G E SOLID STATE  
Triacs

01E 17747 D F-25-17

**2N5441-2N5446, T6420 Series**

File Number **593**

**40-A Silicon Triacs**

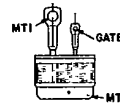
**Features:**

- *di/dt* capability = 100 A/ $\mu$ s
- Low switching losses
- Low on-state voltage at high current levels
- Low thermal resistance

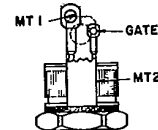
Package \ Voltage	200 V Types	400 V Types	600 V Types
Press-Fit	2N5441	2N5442	2N5443
Stud	2N5444	2N5445	2N5446
Isolated-Stud	T6420B	T6420D	T6420M

RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate-triggering voltages.

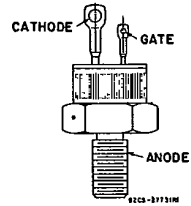
**TERMINAL DESIGNATIONS**



2N5441-43



T6420 Series



2N5444-46

**MAXIMUM RATINGS, Absolute-Maximum Values:**

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with resistive or Inductive Load

	2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	
* REPETITIVE PEAK OFF-STATE VOLTAGE $\Delta$ , $V_{DORM}$ Gate Open, $T_J = -65$ to $100^\circ\text{C}$ .....	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = $360^\circ\text{C}$ ), $I_{T(RMS)}$ Case temperature .....				
$T_C = 70^\circ\text{C}$ (Press-fit types) .....		40		A
$T_C = 65^\circ\text{C}$ (Stud types) .....		40		A
$T_C = 60^\circ\text{C}$ (Isolated-stud types) .....		40		A
For other conditions .....		See Fig. 3		
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT, $I_{TSM}$ For one cycle of applied principal voltage .....				
60 Hz (sinusoidal) .....		300		A
50 Hz (sinusoidal) .....		265		A
For more than one cycle of applied principal voltage .....		See Fig. 4		
RATE OF CHANGE OF ON-STATE CURRENT, $di/dt$ $V_{DM} = V_{DORM}$ , $I_{GT} = 200$ mA, $t_r = 0.1$ $\mu$ s (See Fig. 12) .....		100		A/ $\mu$ s
FUSING CURRENT (for Triac Protection), $I^2t$ $T_J = -65$ to $110^\circ\text{C}$ , $t = 1.25$ to $10$ ms .....		450		A <sup>2</sup> s
* PEAK GATE-TRIGGER CURRENT $\blacksquare$ , $I_{GTM}$ For 1 $\mu$ s max. ....		12		A
* GATE POWER DISSIPATION Peak (For 10 $\mu$ s max., $I_{GTM} \leq 4$ A, $P_{GM}$ .....		40		W
Average, $P_{G(AV)}$ .....		0.75		W
* TEMPERATURE RANGE $\Delta$ Storage, $T_{stg}$ .....		-65 to 150		$^\circ\text{C}$
Operating (Case), $T_C$ .....		-65 to 110		$^\circ\text{C}$
* TERMINAL TEMPERATURE (During Soldering), $T_T$ For 10 s max. (terminals and case) .....		225		$^\circ\text{C}$
STUD TORQUE, $\tau_s$ Recommended .....		35		in-lb
Maximum (DO NOT EXCEED) .....		50		in-lb

\* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.

■ For either polarity of main terminal 2 voltage ( $V_{MT2}$ ) with reference to main terminal 1.

■ For either polarity of gate voltage ( $V_G$ ) with reference to main terminal 1.

$\Delta$  For temperature measurement reference point, see Dimensional Outline

2N5441-2N5446, T6420 Series

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T<sub>C</sub>)

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			
		MIN.	TYP.	MAX.	
Peak Off-State Current: <sup>♠</sup> Gate open, T <sub>J</sub> = 110°C, V <sub>DROM</sub> = Max. rated value . . . . .	I <sub>DROM</sub>	—	0.2	4*	mA
Maximum On-State Voltage: <sup>♠</sup> For I <sub>T</sub> = 100 A (peak), T <sub>C</sub> = 25°C . . . . . For I <sub>T</sub> = 56 A (peak), T <sub>C</sub> = 25°C . . . . .	V <sub>TM</sub>	—	1.7 1.5	2 1.85*	V
DC Holding Current: <sup>♠</sup> Gate open, Initial principal current = 500 mA (dc), v <sub>D</sub> = 12V: T <sub>C</sub> = 25°C . . . . . T <sub>C</sub> = -65°C . . . . . For other case temperatures . . . . .	I <sub>HO</sub>	—	26 —	60 100*	mA
Critical Rate of Rise of Commutation Voltage: <sup>♠</sup> For v <sub>D</sub> = V <sub>DROM</sub> , I <sub>T</sub> (RMS) = 40 A, commutating di/dt = 22 A/ms, gate unenergized, (See Fig. 13): T <sub>C</sub> = 70°C (Press-fit types) . . . . . = 65°C (Stud types) . . . . . = 60°C (Isolated-stud types) . . . . .	dv/dt	5*	30 30 5	— — —	V/μs
Critical Rate of Rise of Off-State Voltage: <sup>♠</sup> For v <sub>D</sub> = V <sub>DROM</sub> , exponential voltage rise, gate open, T <sub>C</sub> = 110°C: 2N5441, 2N5444, T6420B. . . . . 2N5442, 2N5445, T6420D. . . . . 2N5443, 2N5446, T6420M . . . . .	dv/dt	50* 30* 20*	200 150 100	— — —	V/μs
DC Gate-Trigger Current: <sup>♠♠</sup> Mode V <sub>MT2</sub> V <sub>G</sub> For v <sub>D</sub> = 12 V (dc) I <sup>+</sup> positive positive R <sub>L</sub> = 30 Ω III <sup>-</sup> negative negative T <sub>C</sub> = 25°C I <sup>-</sup> positive negative III <sup>+</sup> negative positive	I <sub>GT</sub>	—	15 20 30 40	50 50 80 80	mA
For v <sub>D</sub> = 12 V (dc) Mode V <sub>MT2</sub> V <sub>G</sub> R <sub>L</sub> = 30 Ω I <sup>+</sup> positive positive T <sub>C</sub> = -65°C III <sup>-</sup> negative negative I <sup>-</sup> positive negative III <sup>+</sup> negative positive For other case temperatures . . . . .		—	— — — —	125* 125* 240* 240*	
DC Gate-Trigger Voltage: <sup>♠♠</sup> For v <sub>D</sub> = 12 V (dc), R <sub>L</sub> = 30 Ω, T <sub>C</sub> = 25°C . . . . . = -65°C . . . . . For other case temperatures . . . . . For v <sub>D</sub> = V <sub>DROM</sub> , R <sub>L</sub> = 125 Ω, T <sub>C</sub> = 110°C . . . . .	V <sub>GT</sub>	— — 0.2	1.35 1.8 —	2.5 3.4* —	V
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v <sub>D</sub> = V <sub>DROM</sub> , I <sub>GT</sub> = 200 mA, t <sub>r</sub> = 0.1 μs, I <sub>T</sub> = 60 A (peak), T <sub>C</sub> = 25°C (See Figs. 10 & 14) . . . . .	t <sub>gt</sub>	—	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types . . . . . Stud types . . . . . Isolated-stud types . . . . . Transient (Press-fit & stud types) . . . . .	R <sub>θJC</sub>	— — — —	— — — —	0.8* 0.9* 1	°C/W

\* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.  
♠ For either polarity of main terminal 2 voltage (V<sub>MT2</sub>) with reference to main terminal 1.  
♠♠ For either polarity of gate voltage (V<sub>G</sub>) with reference to main terminal 1.

2N5441-2N5446, T6420 Series

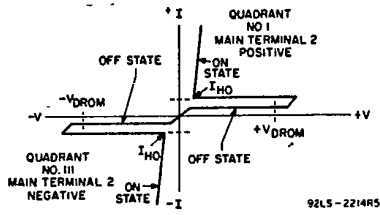


Fig. 1 - Principal voltage-current characteristic.

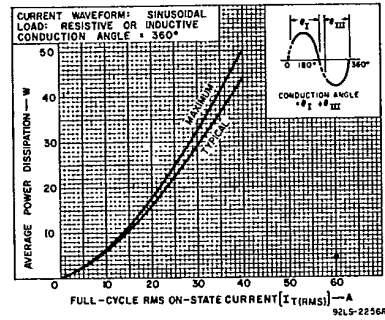


Fig. 2 - Power dissipation vs. on-state current.

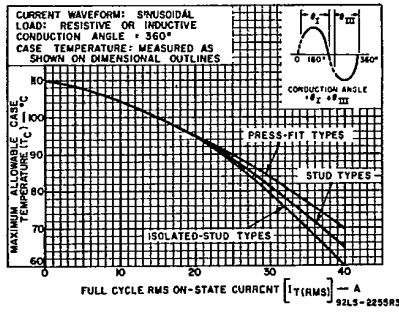


Fig. 3 - Maximum allowable case temperature vs. on-state current.

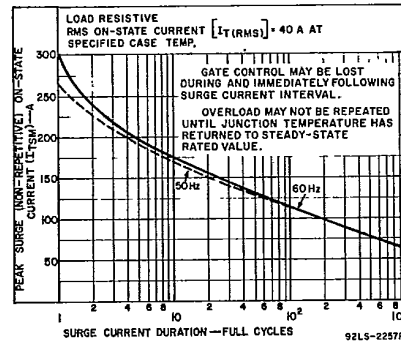


Fig. 4 - Peak surge on-state current vs. surge current duration.

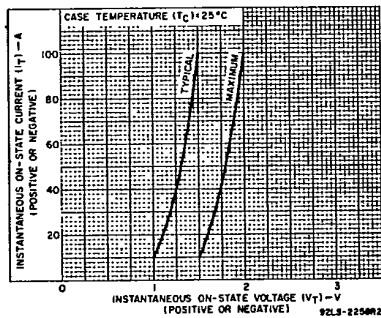


Fig. 5 - On-state current vs. on-stage voltage.

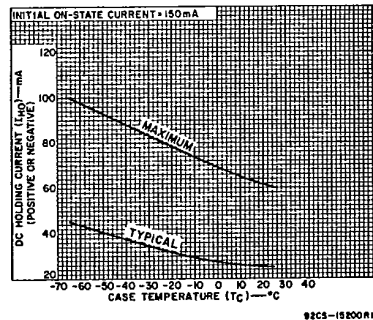


Fig. 6 - DC holding current vs. case temperature.

2N5441-2N5446, T6420 Series

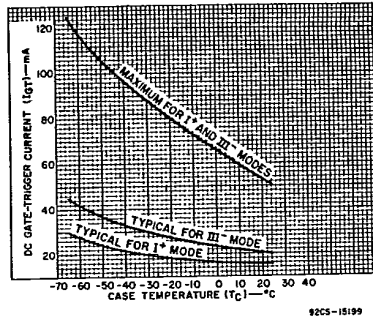


Fig. 7 - DC gate-trigger current vs. case temperature (I<sup>+</sup> & III<sup>-</sup> modes).

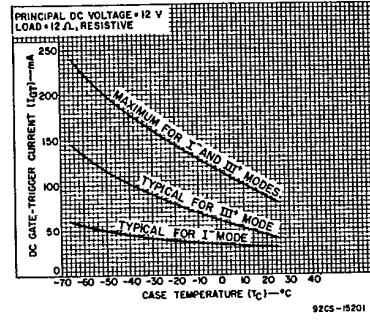


Fig. 8 - DC gate-trigger current vs. case temperature (I<sup>-</sup> & III<sup>+</sup> modes).

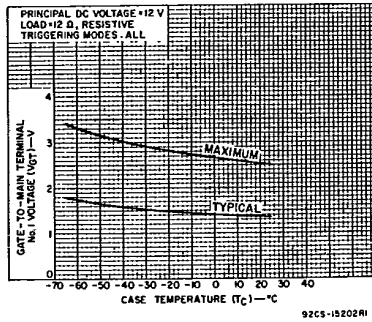


Fig. 9 - DC gate trigger voltage vs. case temperature.

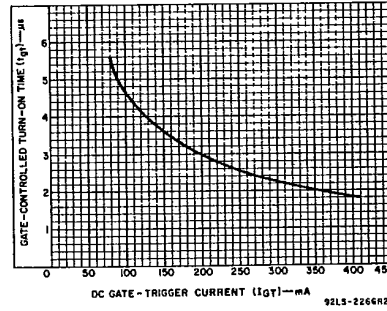


Fig. 10 - Turn-on time vs. gate-trigger current.

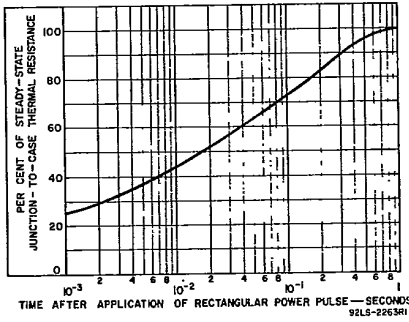


Fig. 11 - Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

Tracs

2N5441-2N5446, T6420 Series

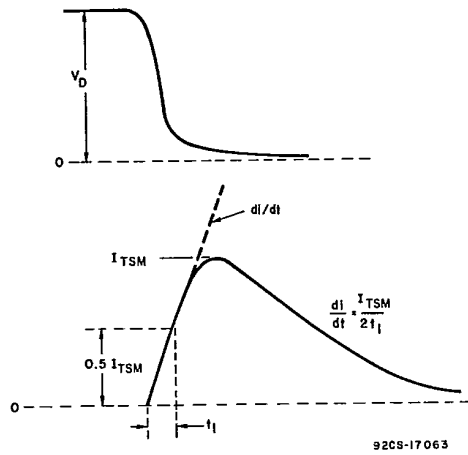


Fig. 12 - Rate of change of on-state current with time (defining di/dt).

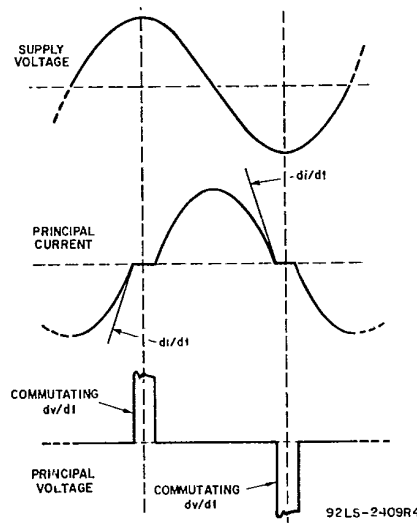


Fig. 13 - Relationship between supply voltage and principal current (Inductive load) showing reference points for definition of commutating voltage (dv/dt).

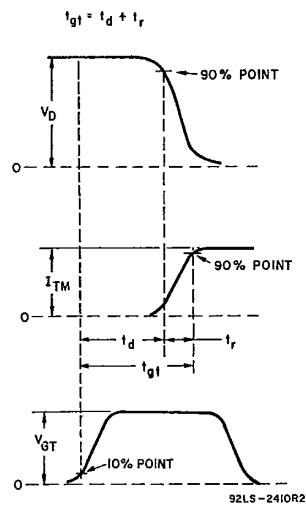


Fig. 14 - Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time ( $t_{gt}$ ).