



2M x 8 Static RAM

Features

- High speed
 - $t_{AA} = 8, 10, 12 \text{ ns}$
- Low active power
 - 1080 mW (max.)
- Operating voltages of $3.3 \pm 0.3V$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and \overline{CE}_2 features

Functional Description

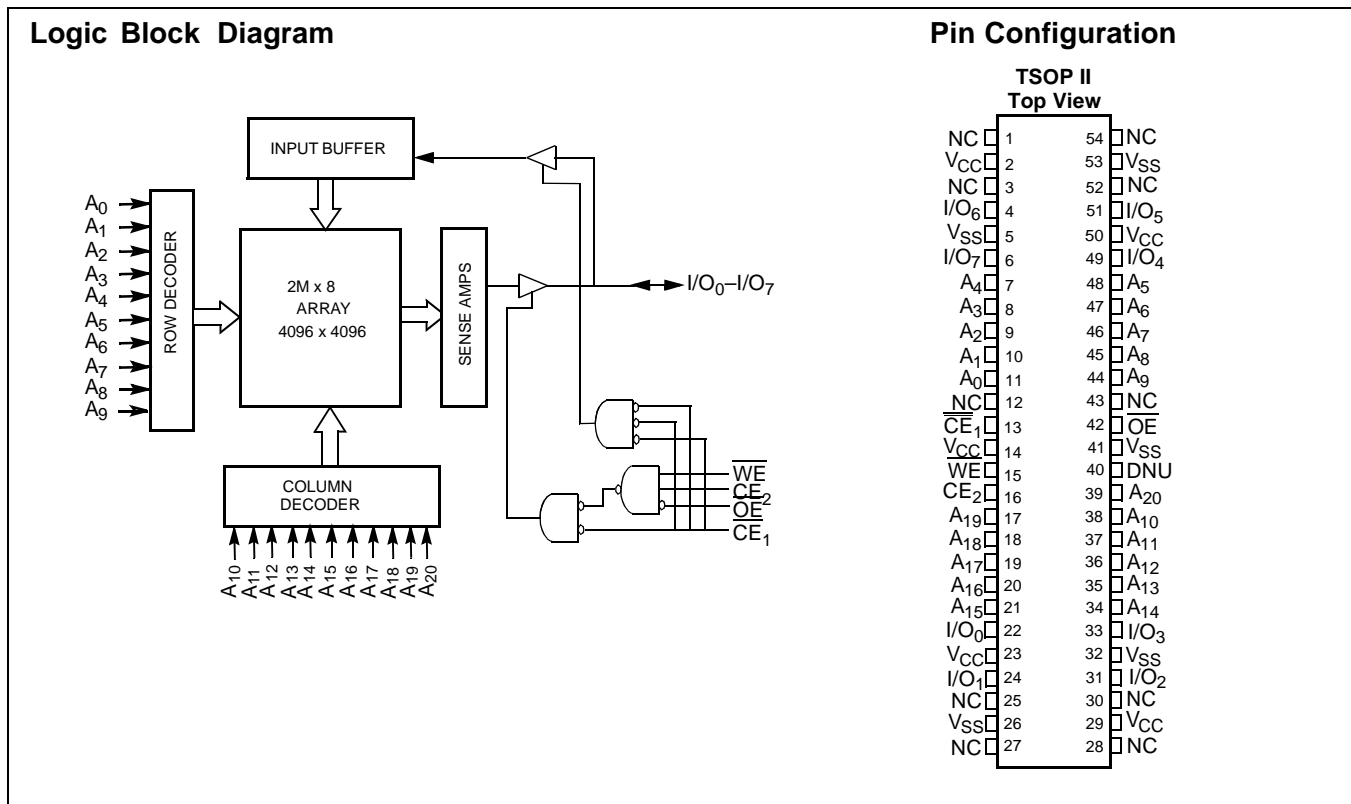
The CY7C1069AV33 is a high-performance CMOS Static RAM organized as 2,097,152 words by 8 bits. Writing to the

device is accomplished by enabling the chip (by taking \overline{CE}_1 LOW and \overline{CE}_2 HIGH) and Write Enable (\overline{WE}) inputs LOW.

Reading from the device is accomplished by enabling the chip (\overline{CE}_1 LOW and \overline{CE}_2 HIGH) as well as forcing the Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a Write operation (\overline{CE}_1 LOW, \overline{CE}_2 HIGH, and \overline{WE} LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and a 48-ball fine-pitch ball grid array (FBGA) package.

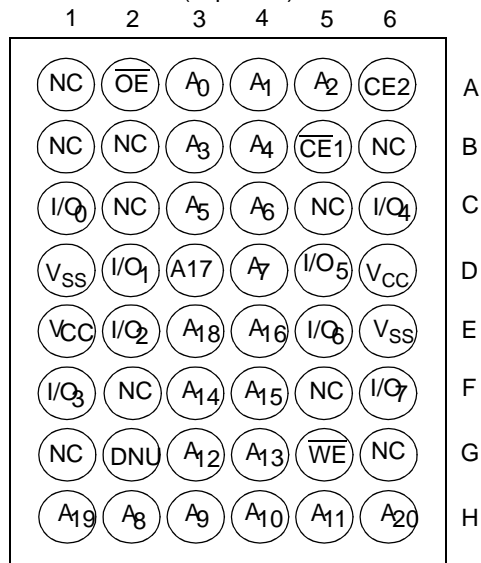


Selection Guide

		-8	-10	-12	Unit
Maximum Access Time		8	10	12	ns
Maximum Operating Current	Commercial	300	275	260	mA
	Industrial	300	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	50	mA

Pin Configurations
48-ball FBGA

(Top View)



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

 DC Voltage Applied to Outputs in High-Z State^[1] -0.5V to V_{CC} + 0.5V

 DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

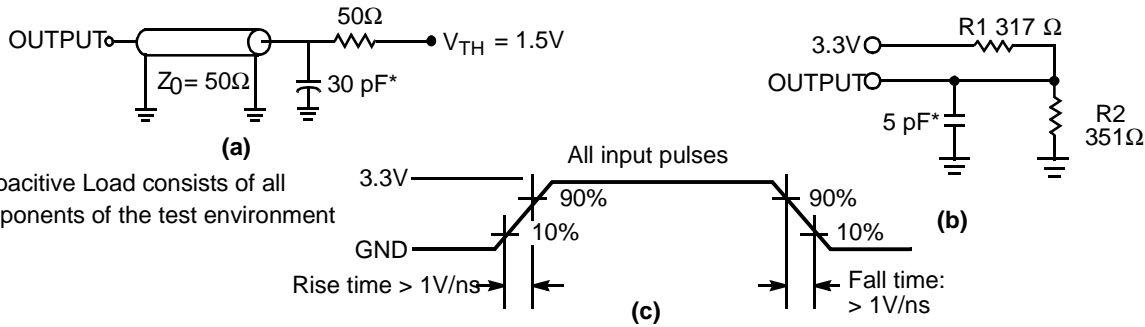
Parameter	Description	Test Conditions	-8		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	-1	+1	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}	Commercial	300		275		260	mA
			Industrial	300		275		260	mA
I _{SB1}	Automatic CE Power-down Current — TTL Inputs	CE ₂ ≤ V _{IL} , $\overline{\text{Max. V}}_{\text{CC}}, \text{SCE} \geq V_{\text{IH}}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		70		70		70	mA
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ₂ ≤ 0.3V Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Commercial/ Industrial	50		50		50	mA

Capacitance^[2]

Parameter	Package	Description	Test Conditions	Max.	Unit
C _{IN}	Z54	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	6	pF
	BA48			8	pF
C _{OUT}	Z54	I/O Capacitance		8	pF
	BA48			10	pF

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[3]


*Capacitive Load consists of all components of the test environment

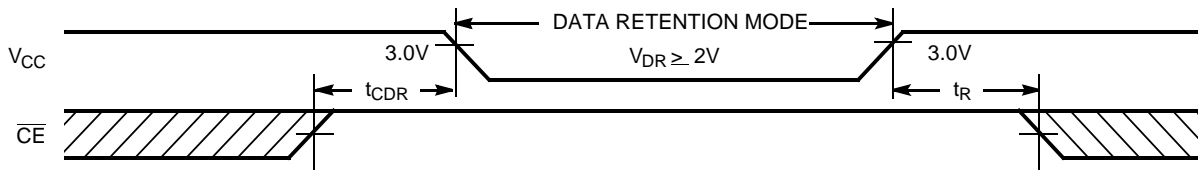
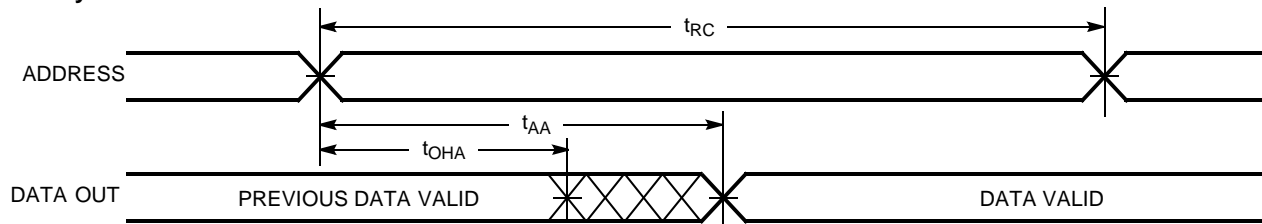
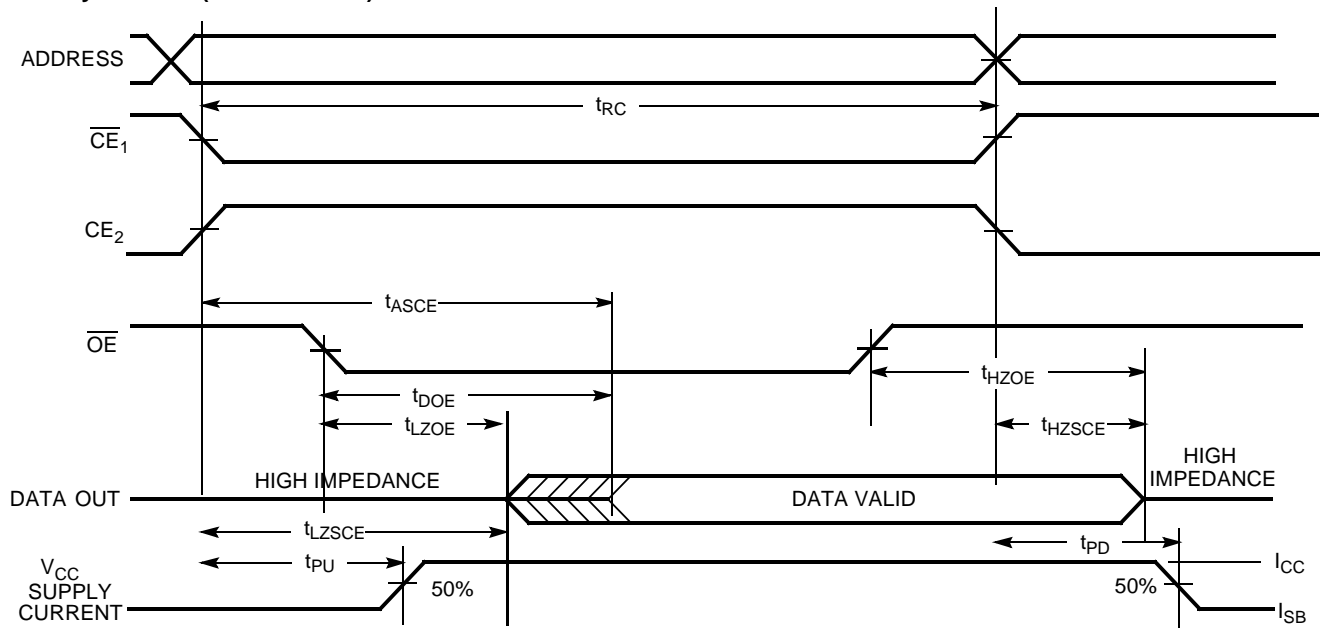
*Including jig and scope

AC Switching Characteristics Over the Operating Range^[4]

Parameter	Description	-8		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}	V_{CC} (typical) to the First Access ^[5]	1		1		1		ms
t_{RC}	Read Cycle Time	8		10		12		ns
t_{AA}	Address to Data Valid		10		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}_1$ LOW/ CE_2 HIGH to Data Valid		8		10		12	ns
t_{DOE}	OE LOW to Data Valid		5		5		6	ns
t_{LZOE}	OE LOW to Low-Z ^[6]	1		1		1		ns
t_{HZOE}	OE HIGH to High-Z ^[6]		5		5		6	ns
t_{LZCE}	$\overline{\text{CE}}_1$ LOW/ CE_2 HIGH to Low-Z ^[6]	3		3		3		ns
t_{HZCE}	$\overline{\text{CE}}_1$ HIGH/ CE_2 LOW to High-Z ^[6]		5		5		6	ns
t_{PU}	$\overline{\text{CE}}_1$ LOW/ CE_2 HIGH to Power-up ^[7]	0		0		0		ns
t_{PD}	$\overline{\text{CE}}_1$ HIGH/ CE_2 LOW to Power-down ^[7]		8		10		12	ns
Write Cycle^[8, 9]								
t_{WC}	Write Cycle Time	8		10		12		ns
t_{SCE}	$\overline{\text{CE}}_1$ LOW/ CE_2 HIGH to Write End	6		7		8		ns
t_{AW}	Address Set-up to Write End	6		7		8		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	6		7		8		ns
t_{SD}	Data Set-up to Write End	5		5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	WE HIGH to Low-Z ^[6]	3		3		3		ns
t_{HZWE}	WE LOW to High-Z ^[6]		5		5		6	ns

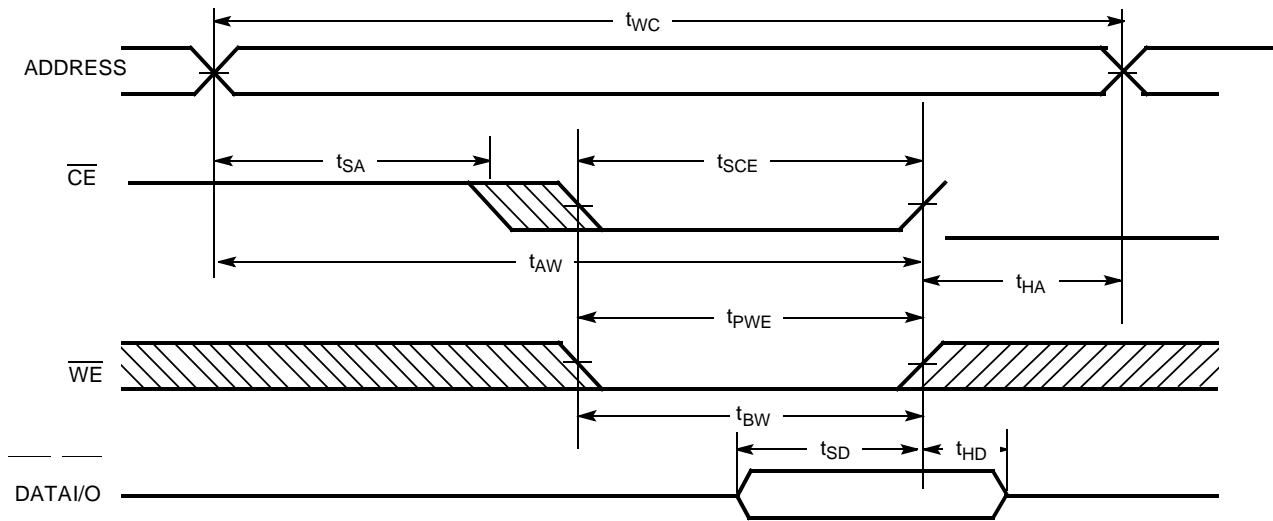
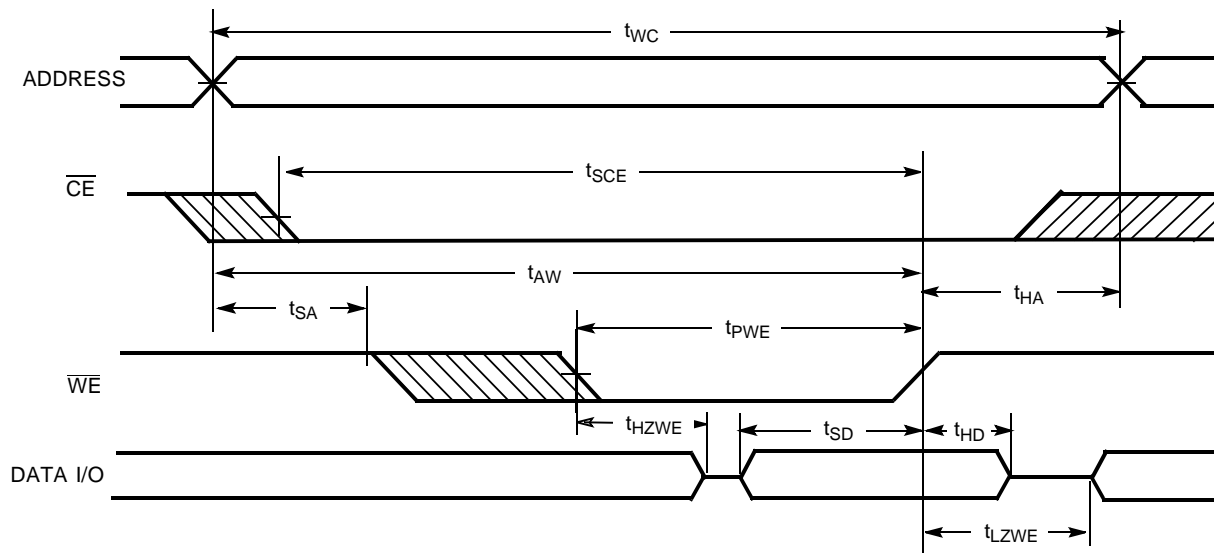
Notes:

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR} , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally. t_{power} time has to be provided initially before a Read/Write operation is started.
- t_{HZOE} , t_{HZSCE} , t_{HZWE} and t_{LZOE} , t_{LZCE} , and t_{LZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of $\overline{\text{CE}}_1$ LOW / CE_2 HIGH, and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}_1$ and $\overline{\text{WE}}$ must be LOW along with CE_2 HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ($\overline{\text{WE}}$ controlled, OE LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[10, 11]

Read Cycle No. 2 (\overline{OE} Controlled) [11, 12]

Notes:

10. Device is continuously selected. $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
11. \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE}_1 Controlled)^[13, 14, 15]

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)^[13, 14, 15]

Truth Table

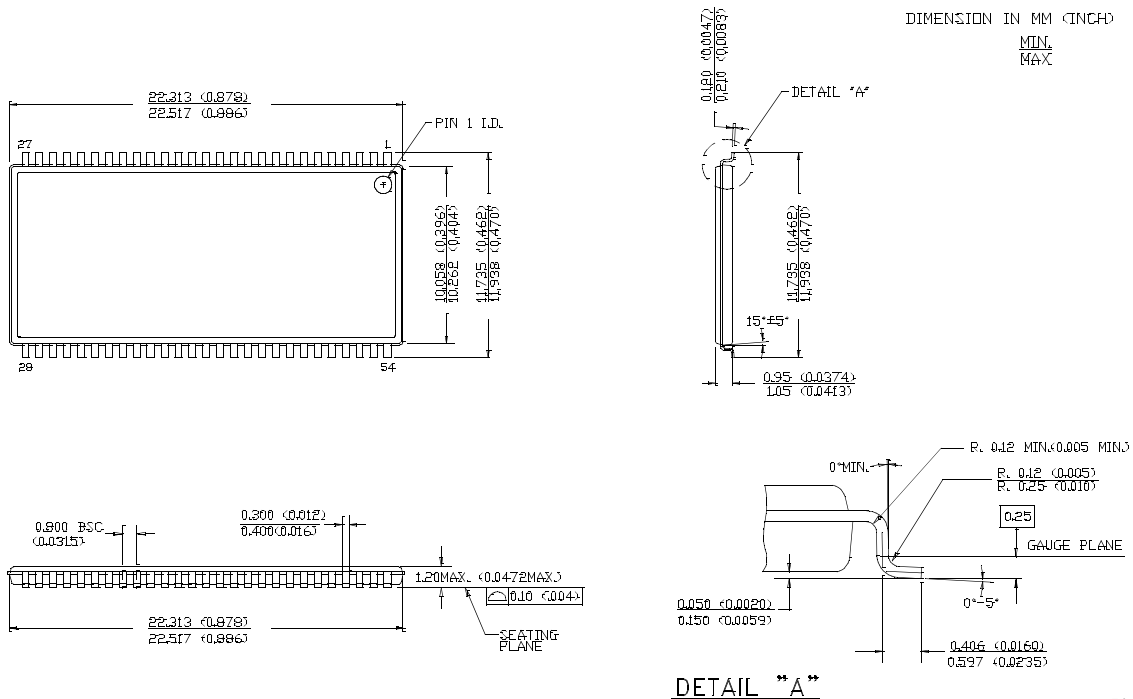
\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High-Z	Power-down	Standby (I_{SB})
X	L	X	X	High-Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read All Bits	Active (I_{CC})
L	H	X	L	Data In	Write All Bits	Active (I_{CC})
L	H	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Notes:

12. Address valid prior to or coincident with \overline{CE}_1 transition LOW and \overline{CE}_2 transition HIGH.
13. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
14. If \overline{CE}_1 goes HIGH / \overline{CE}_2 LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
15. \overline{CE} above is defined as a combination of \overline{CE}_1 and \overline{CE}_2 . It is active low.

Ordering Information

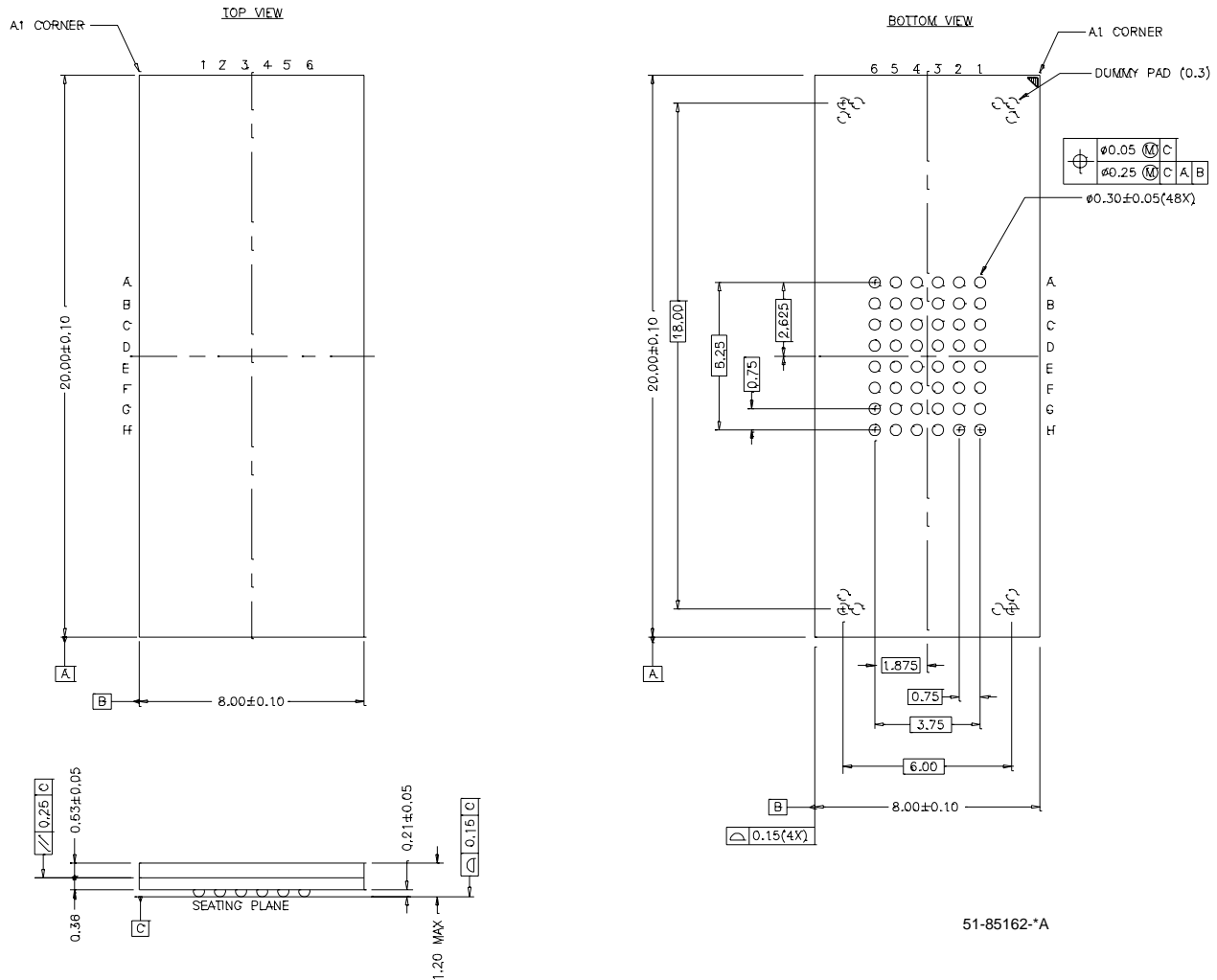
Speed (ns)	Ordering Code ^[16]	Package Name	Package Type	Operating Range
8	CY7C1069AV33-8ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-8ZI			Industrial
	CY7C1069AV33-8BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-8BAI			Industrial
10	CY7C1069AV33-10ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-10ZI			Industrial
	CY7C1069AV33-10BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-10BAI			Industrial
12	CY7C1069AV33-12ZC	Z54	54-pin TSOP II	Commercial
	CY7C1069AV33-12ZI			Industrial
	CY7C1069AV33-12BAC	BA48	48-ball Mini BGA	Commercial
	CY7C1069AV33-12BAI			Industrial

Package Diagrams
54-lead Thin Small Outline Package, Type II Z54-II


51-85160-**

Note:

16. Contact a Cypress Representative for availability of the 48-ball Mini BGA (BA48) package.

Package Diagrams (continued)
48-ball (8 mm x 20 mm x 1.2 mm) FBGA BA48G


51-85162-A

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Document History Page

Document Title: CY7C1069AV33 2M x 8 Static RAM				
Document Number: 38-05255				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113724	03/27/02	NSL	New Data Sheet
*A	117060	07/31/02	DFP	Removed 15-ns bin
*B	117990	08/30/02	DFP	Added 8-ns bin Changing I _{CC} for 8, 10, 12 bins t _{power} changed from 1 μs to 1 ms Load Cap Comment changed (for Tx line load) t _{SD} changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin #'s (t _{HZ} , t _{DOE} , t _{DBE}) Removed hz < lz comments
*C	120385	11/13/02	DFP	Final Data Sheet Added note 4 to "AC Test Loads and Waveforms" and note 7 to t _{pu} and t _{pd} Updated Input/Output Caps (for 48BGA only) to 8 pf/10 pf and for the 54-pin TSOP to 6/8 pf
*D	124441	2/25/03	MEG	Changed ISB1 from 100 mA to 70 mA Shaded the 48fBGA product offering information