



# LB1945H

## PWM Current Control Type Stepping Motor Driver

### Preliminary

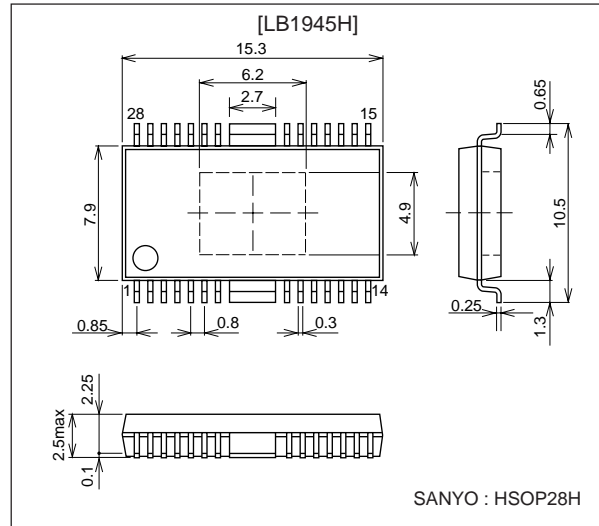
#### Features

- PWM current control (external excitation)
- Load current digital selection (1-2, W1-2, and 2 phase excitation drives possible)
- Built-in upper/lower diode
- Simultaneous ON prevention function (feedthrough current prevention)
- Built-in thermal shutdown circuit
- Built-in noise canceler

#### Package Dimensions

unit: mm

#### 3233-HSOP28H



### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

| Parameter                    | Symbol              | Conditions                           | Ratings                 | Unit |
|------------------------------|---------------------|--------------------------------------|-------------------------|------|
| Maximum motor supply voltage | V <sub>BB</sub> max |                                      | 30                      | V    |
| Output peak current          | I <sub>OPEAK</sub>  | tw ≤ 20 μs                           | 1.0                     | A    |
| Output continuous current    | I <sub>O</sub> max  |                                      | 0.8                     | A    |
| Logic supply voltage         | V <sub>CC</sub> max |                                      | 6.0                     | V    |
| Logic input voltage range    | V <sub>IN</sub> max |                                      | -0.3 to V <sub>CC</sub> | V    |
| Emitter output voltage       | V <sub>E</sub> max  |                                      | 1.0                     | V    |
| Allowable power dissipation  | P <sub>d</sub> max  | Ta = 25°C, with specified substrate* | 1.9                     | W    |
| Operating temperature        | T <sub>opr</sub>    |                                      | -20 to +90              | °C   |
| Storage temperature          | T <sub>stg</sub>    |                                      | -55 to +150             | °C   |

\* Specified substrate: 114.3 × 76.1 × 1.6 mm<sup>3</sup>, glass epoxy

#### Allowable Operating Ranges at Ta = 25°C

| Parameter            | Symbol           | Conditions | Ratings      | Unit |
|----------------------|------------------|------------|--------------|------|
| Motor supply voltage | V <sub>BB</sub>  |            | 10 to 28     | V    |
| Logic supply voltage | V <sub>CC</sub>  |            | 4.75 to 5.25 | V    |
| Reference voltage    | V <sub>REF</sub> |            | 1.5 to 5.0   | V    |

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## Electrical Characteristics at Ta = 25°C, VBB = 24V, VCC = 5V, VREF = 5.0V

| Parameter                    | Symbol                              | Conditions                          | Ratings   |      |     | Unit |      |      |    |
|------------------------------|-------------------------------------|-------------------------------------|---|------|-----|------|------|------|----|
|                              |                                     |                                     | min   | typ  | max |      |      |      |    |
| Output Block                 | Output stage supply current         | I <sub>BB ON</sub>                  | I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V, ENABLE = 0.8V           |      |     | 0.5  | 1.0  | 2.0  | mA |
|                              |                                     | I <sub>BB OFF</sub>                 | ENABLE = 3.2V   |      |     |      |      | 0.2  | mA |
|                              | Output saturation voltage           | V <sub>osat 1</sub>                 | I <sub>o</sub> = +0.5A sink   |      | 0.3 | 0.5  | V    |      |    |
|                              |                                     | V <sub>osat 2</sub>                 | I <sub>o</sub> = +0.8A sink   |      | 0.5 | 0.7  | V    |      |    |
|                              |                                     | V <sub>osat 3</sub>                 | I <sub>o</sub> = -0.5A source   |      | 1.6 | 1.8  | V    |      |    |
|                              |                                     | V <sub>osat 4</sub>                 | I <sub>o</sub> = -0.8A source   |      | 1.8 | 2.0  | V    |      |    |
|                              | Output leakage current              | I <sub>o1(leak)</sub>               | V <sub>o</sub> = V sink   |      |     |      | 50   | μA   |    |
|                              |                                     | I <sub>o2(leak)</sub>               | V <sub>o</sub> = 0V source  | -50  |     |      |      | μA   |    |
| Output sustain voltage       | V <sub>SUS</sub>                    | L = 3.9 mH I <sub>o</sub> = 1.0A *1 | 30  |      |     |      | V    |      |    |
| Logic Block                  | Logic supply current                | I <sub>CC ON</sub>                  | I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V, ENABLE = 0.8V           |      |     | 50.0 | 70.0 | 92.0 | mA |
|                              |                                     | I <sub>CC OFF</sub>                 | ENABLE = 3.2V   |      |     | 7.0  | 10.0 | 13.0 | mA |
|                              | Input voltage                       | V <sub>IH</sub>                     |   | 3.2  |     |      |      | V    |    |
|                              |                                     | V <sub>IL</sub>                     |   |      |     |      | 0.8  | V    |    |
|                              | Input current                       | I <sub>IH</sub>                     | V <sub>IH</sub> = 3.2V  | 35   | 50  | 65   |      | μA   |    |
|                              |                                     | I <sub>IL</sub>                     | V <sub>IL</sub> = 0.8V  | 7    | 10  | 13   |      | μA   |    |
|                              | Set current control threshold value | V <sub>ref</sub> /V <sub>sen</sub>  | I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V                          | 9.5  | 10  | 10.5 |      |      |    |
|                              |                                     |                                     | I <sub>1</sub> = 3.2V, I <sub>2</sub> = 0.8V                          | 13.5 | 15  | 16.5 |      |      |    |
|                              |                                     |                                     | I <sub>1</sub> = 0.8V, I <sub>2</sub> = 3.2V                          | 25.5 | 30  | 34.5 |      |      |    |
|                              | Reference current                   | I <sub>ref</sub>                    | V <sub>ref</sub> = 5.0V, I <sub>1</sub> = 0.8V, I <sub>2</sub> = 0.8V | 17.5 | 25  | 32.5 |      | μA   |    |
| CR pin current               | I <sub>CR</sub>                     | CR = 1.0V                           | -1.0  |      |     |      | mA   |      |    |
| Thermal shutdown temperature | T <sub>TSD</sub>                    |                                     |   | 170  |     |      | °C   |      |    |
| Temperature hysteresis width | ΔT <sub>TSD</sub>                   |                                     |   | 40   |     |      | °C   |      |    |

\*1: Assured design target value, not measured

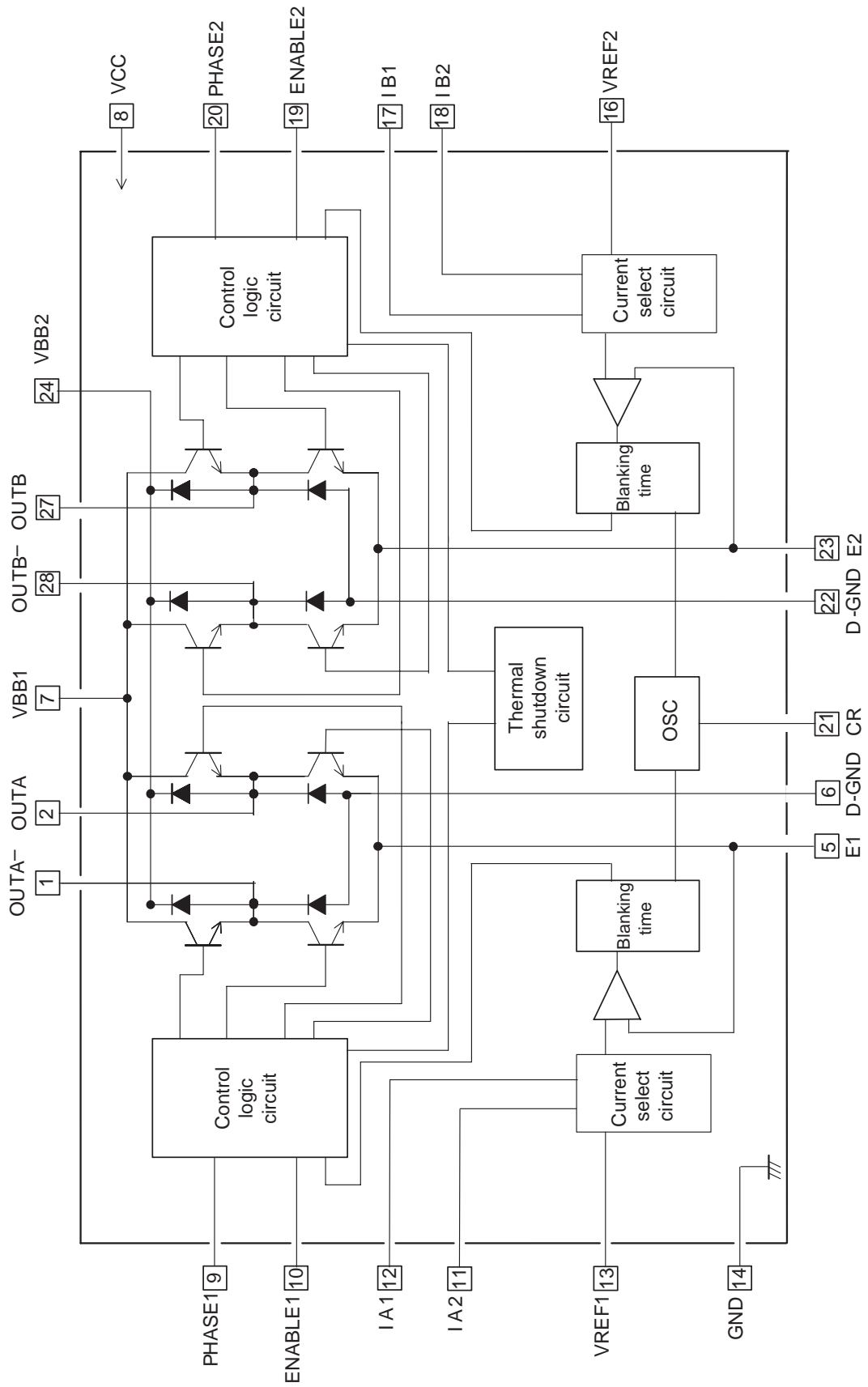
### Truth Table

| ENABLE | PHASE | OUTA | OUTA <sup>-</sup> |
|--------|-------|------|-------------------|
| L      | H     | H    | L                 |
| L      | L     | L    | H                 |
| H      | -     | OFF  | OFF               |

| I1 | I2 | Output current                                   |
|----|----|--|
| L  | L  | $V_{ref} / (10 \times R_E) = I_{out}$            |
| H  | L  | $V_{ref} / (15 \times R_E) = I_{out} \times 2/3$ |
| L  | H  | $V_{ref} / (30 \times R_E) = I_{out} \times 1/3$ |
| H  | H  | 0  |

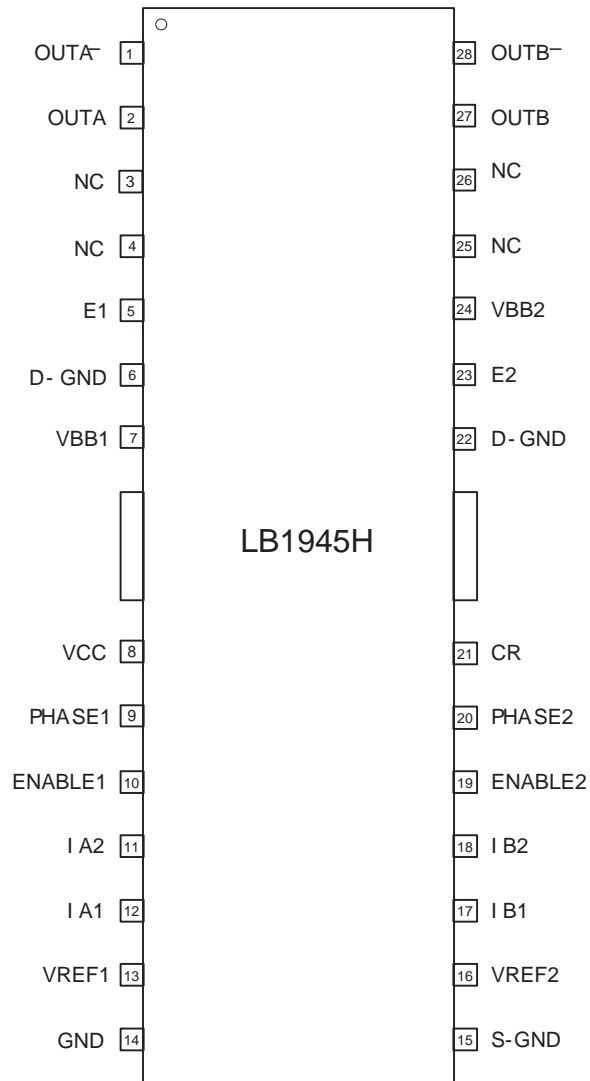
Note: Output is OFF when ENABLE = H or when I1 = I2 = H.

Block Diagram



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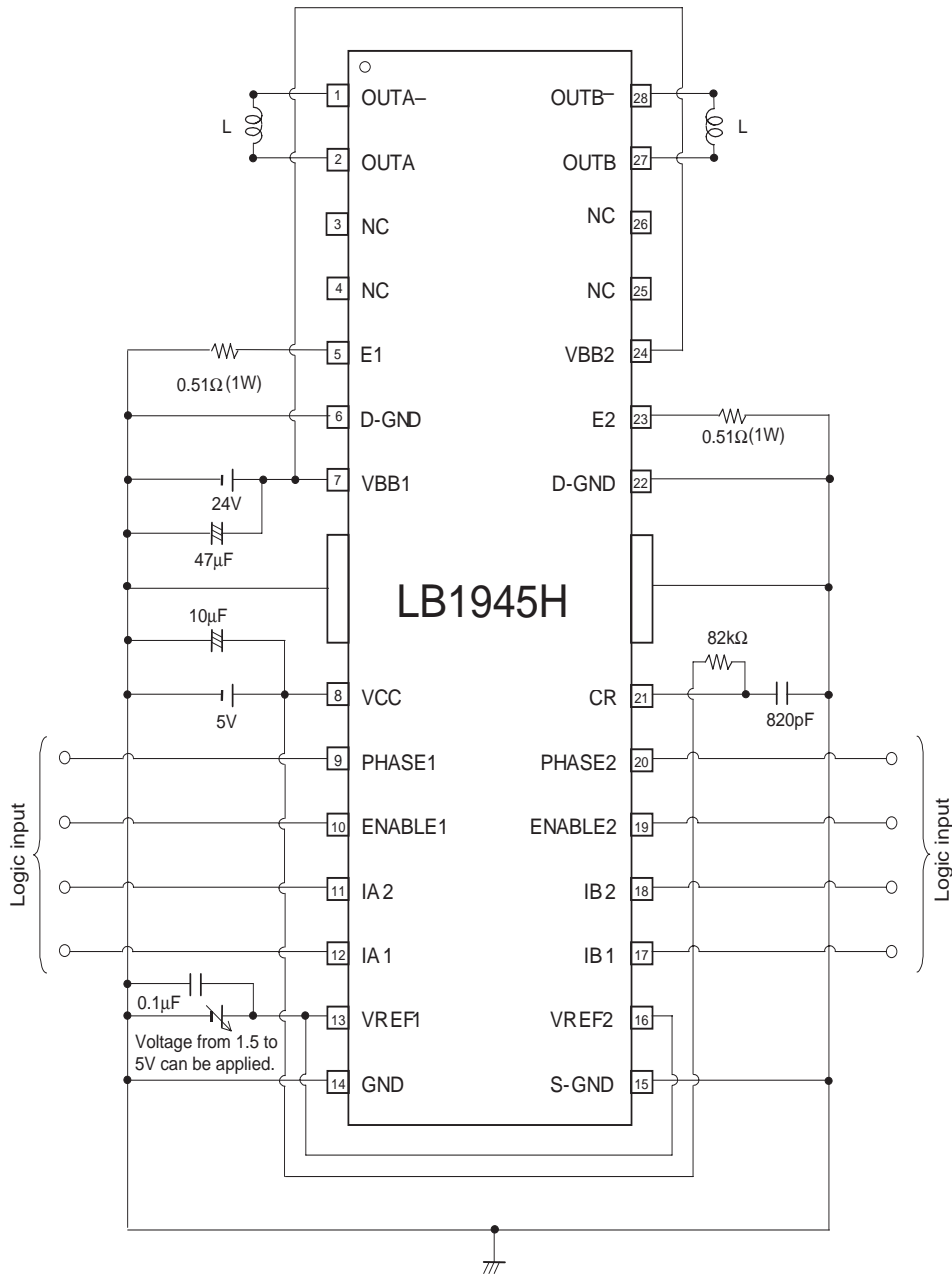
## Pin Assignment



Top view

# LB1945H

## Sample Application Circuit



The fin on the bottom of HSOP-28H package and the fins between pins 7 and 8 and 21 and 22 should be grounded.

**Pin Description**

| Pin name          | Pin number | Function  |
|-------------------|------------|---|
| V <sub>BB1</sub>  | 7          | Output stage power supply voltage pin.  |
| V <sub>BB2</sub>  | 24         | Cathode pin for the upper-side diodes.  |
| E1                | 5          | Insert resistor R <sub>E</sub> between these pins and ground to control set current.  |
| E2                | 23         |   |
| OUTA              | 2          | Output pins.  |
| OUTA <sup>-</sup> | 1          |   |
| OUTB              | 27         |   |
| OUTB <sup>-</sup> | 28         |   |
| GND               | 14         | Ground pin.   |
| S-GND             | 15         | Sense ground pin.   |
| D-GND             | 6          | Lower-side internal diode ground (anode)  |
|                   | 22         |   |
| CR                | 21         | Triangular wave chopping with CR constant setting.<br>Triangular wave OFF time is noise cancel time.                        |
| V <sub>REF1</sub> | 13         | Output current setting pins.<br>(Output current is set by inputting a 1.5V to 7.5V voltage.)                                |
| V <sub>REF2</sub> | 16         |   |
| PHASE1            | 9          | Output phase select input pin.<br>High input: OUTA = H, OUTA <sup>-</sup> = L<br>Low input: OUTA = L, OUTA <sup>-</sup> = H |
| PHASE2            | 20         |   |
| ENABLE1           | 10         | Output ON/OFF setting input pins.<br>High input: output OFF<br>Low input: output ON   |
| ENABLE2           | 19         |   |
| IA1, IA2          | 12, 11     | Output current setting digital input pins.  |
| IB1, IB2          | 17, 18     | Current is set to 1/3, 2/3, 1 by High and Low combinations.   |
| V <sub>CC</sub>   | 8          | Logic block power supply voltage pin.   |

Usage Notes

1. V<sub>REF</sub> pin

Because the V<sub>REF</sub> pin is used as reference voltage input pin for the current setting, care must be taken to prevent noise from affecting the input.

2. GND pin

Because this IC switches large currents, the ground pattern must be designed with care. The fin on the bottom of the package and the fins between pins 7 and 8 and 21 and 22 should be grounded. Low-impedance patterns should be used in blocks where large currents flow, and these blocks should be separated from low-level signal blocks. In particular, the ground of the sense resistor R<sub>E</sub> at pin E should be located close to the IC ground. Pattern layout should be designed so that the capacitors between V<sub>CC</sub> and ground and V<sub>BB</sub> and ground are close to V<sub>CC</sub> and V<sub>BB</sub>.

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