LR38581

Timing Generator IC for 270 k/320 k-pixel Color CCDs with Dual-power-supply Operation

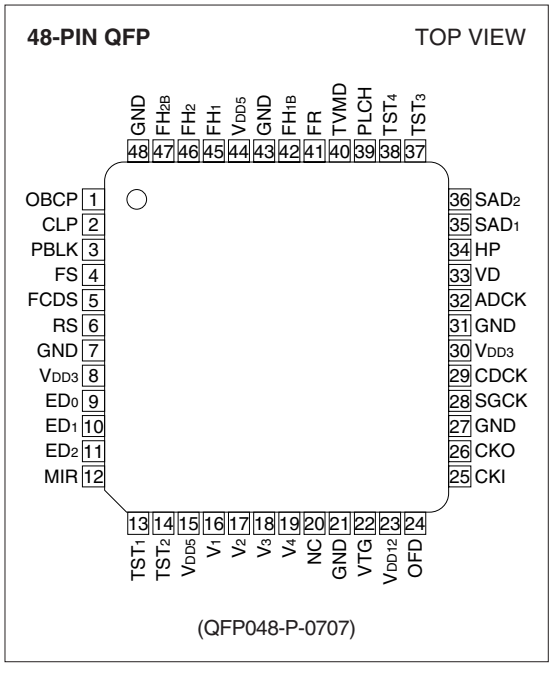
DESCRIPTION

The LR38581 is a CMOS timing generator IC which generates timing pulses for driving 270 k/320 k-pixel color CCD area sensors with a dual-power-supply operation and processing pulses for color video signals.

FEATURES

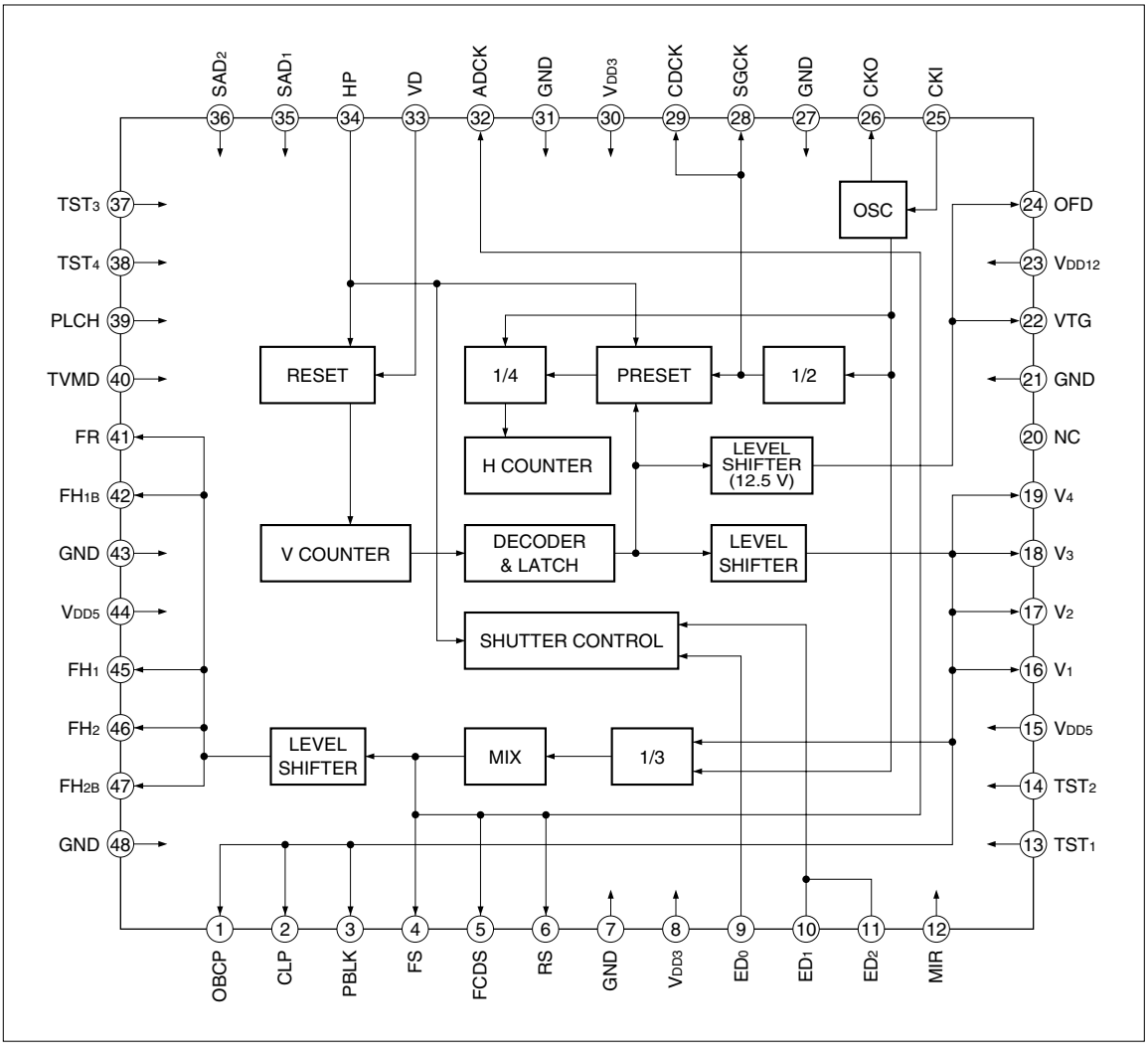
- Designed for 270 k/320 k-pixel color CCD area sensors with a dual-power-supply-operation
- Switchable between NTSC and PAL modes
- Switchable between normal and mirror images
- Level shifter for readout and shutter pulses included
- +3.3 V, +5 V and +12.5 V power supplies
- Package :
  48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

PIN CONNECTIONS

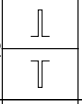
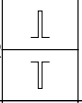
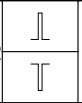


(QFP048-P-0707)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION
1	OBCP	O4MA3		Optical black clamp pulse output	A pulse to clamp the optical black signal. This pulse stays low during the absence of effective pixels within the vertical blanking. The polarity can be changed by PLCH (pin 39).
2	CLP	O4MA3		AD input signal clamp pulse output	A pulse to clamp the AD input signal. The polarity can be changed by PLCH (pin 39).
3	PBLK	O4MA3		Pre-blanking pulse output	A pulse that corresponds to the cease period of the horizontal transfer pulse.
4	FS	O4MA32		CDS pulse output 1	A pulse to sample-hold the signal from CCD. The polarity can be changed by PLCH (pin 39). The output phase of FS is selected by serial data.
5	FCDS	O4MA32		CDS pulse output 2	A pulse to clamp the feed-through level from CCD. The polarity can be changed by PLCH (pin 39). The output phase of FCDS is selected by serial data.
6	RS	O4MA32		S/H pulse output	A pulse to sample-hold the signal from CDS circuit. The polarity can be changed by PLCH (pin 39). The output phase of RS is selected by serial data.
7	GND	–	–	Ground	A grounding pin.
8	V_{DD3}	–	–	Power supply	Supply of +3.3 V power.
9	ED_0	ICSU3	–	Shift register clock input	An input pin for the clock of the shift register, to control the functions of LR38581. For details, see "**Serial Data Control**."
10	ED_1	ICSU3	–	Shift register data input	An input pin for the data of the shift register, to control the functions of LR38581. For details, see "**Serial Data Control**."
11	ED_2	ICSU3	–	Strobe pulse input	An input pin for the strobe pulse, to control the functions of LR38581. For details, see "**Serial Data Control**."
12	MIR	ICU3	–	Mirror mode selection	An input pin to select mirror or normal image mode L level : Normal image mode H level or open : Mirror image mode MIR / L (Normal mode) / H or open (Mirror mode) FH_{1B} / ≒ FH_1 / ≒ FH_2 FH_{2B} / ≒ FH_2 / ≒ FH_1
13	TST_1	ICD5	–	Test pin 1	A test pin. Set open or to L level in the normal mode.
14	TST_2	ICD5	–	Test pin 2	A test pin. Set open or to L level in the normal mode.
15	V_{DD5}	–	–	Power supply	Supply of +5 V power.
16	V_1	O4MA52		Vertical transfer pulse output 1	A pulse to drive vertical CCD shift register. Connect to ϕV_1 pin of CCD.
17	V_2	O4MA52		Vertical transfer pulse output 2	A pulse to drive vertical CCD shift register. Connect to ϕV_2 pin of CCD.
18	V_3	O4MA52		Vertical transfer pulse output 3	A pulse to drive vertical CCD shift register. Connect to ϕV_3 pin of CCD.

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>I/O</th><th>POLARITY</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>19</td><td>V_4</td><td>O4MA52</td><td></td><td>Vertical transfer pulse output 4</td><td>A pulse to drive vertical CCD shift register.
Connect to ϕV_4 pin of CCD.</td></tr>
<tr><td>20</td><td>NC</td><td>–</td><td>–</td><td>No connection</td><td>No connection</td></tr>
<tr><td>21</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>A grounding pin.</td></tr>
<tr><td>22</td><td>VTG</td><td>O12MHV</td><td>  </td><td>Readout pulse output</td><td>A pulse that transfers the charge of the photo-diode to the vertical shift register.
Connect to VTG pin of CCD.</td></tr>
<tr><td>23</td><td>V_{DD12}</td><td>–</td><td>–</td><td>Power supply</td><td>Supply of +12.5 V power.</td></tr>
<tr><td>24</td><td>OFD</td><td>O12MHV</td><td></td><td>OFD pulse output</td><td>A pulse that sweeps the charge of the photo-diode for electronic shutter. Connect to OFD pin of CCD.
Held at L level at normal mode.</td></tr>
<tr><td>25</td><td>CKI</td><td>OSCI3</td><td>–</td><td>Clock input</td><td>An input pin for reference clock oscillation.
Connect to CKO (pin 26) with R.
The frequencies are as follows :
<table><tr><th>TVMD</th><th>Frequency</th></tr><tr><td>L</td><td>28.63636 MHz (1820 fH)</td></tr><tr><td>H</td><td>28.37500 MHz (1816 fH)</td></tr></table>fH = Horizontal frequency</td></tr>
<tr><td>26</td><td>CKO</td><td>OSCO3</td><td>–</td><td>Clock output</td><td>An output pin for reference clock oscillation.
The output is the inverse of CKI (pin 25).</td></tr>
<tr><td>27</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>A grounding pin.</td></tr>
<tr><td>28</td><td>SGCK</td><td>O4MA32</td><td>  </td><td>SSG clock output</td><td>An output pin to generate HP and VD pulses.
The frequencies are as follows :
<table><tr><th>TVMD</th><th>Frequency</th></tr><tr><td>L</td><td>14.31818 MHz (910 fH)</td></tr><tr><td>H</td><td>14.18750 MHz (908 fH)</td></tr></table></td></tr>
<tr><td>29</td><td>CDCK</td><td>O4MA32</td><td>  </td><td>DSP clock output</td><td>An output pin for DSP IC.
The frequencies are as follows :
<table><tr><th>TVMD</th><th>Frequency</th></tr><tr><td>L</td><td>9.5035 MHz (1820/3 fH)</td></tr><tr><td>H</td><td>9.4375 MHz (1816/3 fH)</td></tr></table></td></tr>
<tr><td>30</td><td>V_{DD3}</td><td>–</td><td>–</td><td>Power supply</td><td>Supply of +3.3 V power.</td></tr>
<tr><td>31</td><td>GND</td><td>–</td><td>–</td><td>Ground</td><td>A grounding pin.</td></tr>
<tr><td>32</td><td>ADCK</td><td>O4MA32</td><td>  </td><td>AD clock output</td><td>An output pin for AD converter.
The frequencies are as follows :
<table><tr><th>TVMD</th><th>Frequency</th></tr><tr><td>L</td><td>9.5035 MHz (1820/3 fH)</td></tr><tr><td>H</td><td>9.4375 MHz (1816/3 fH)</td></tr></table>The output phase of ADCK is selected by SAD_1 (pin 35) and SAD_2 (pin 36).</td></tr>
</table>

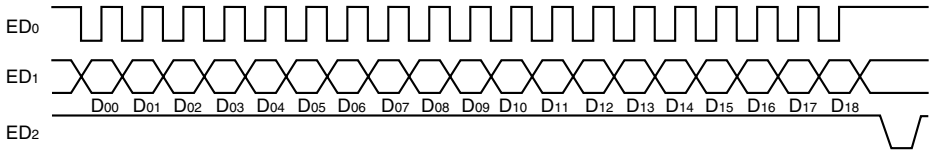
PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION
33	VD	IC3		Vertical reference pulse input	An input pin for reference of vertical pulse. Connect to VD pin of DSP IC.
34	HP	IC3		Horizontal reference pulse input	An input pin for reference of horizontal pulse. Connect to HD pin of DSP IC.
35	SAD_1	ICU3	–	ADCK phase control input 1	An input pin to select the phase of ADCK.
36	SAD_2	ICU3	–	ADCK phase control input 2	
37	TST_3	ICD5	–	Test pin 3	A test pin. Set open or to L level in the normal mode.
38	TST_4	ICD5	–	Test pin 4	A test pin. Set open or to L level in the normal mode.
39	PLCH	ICU5	–	Polarity selection input	An input pin to select the polarity of OBCP (pin 1), CLP (pin 2), FS (pin 4), FCDS (pin 5) and RS (pin 6).
40	TVMD	ICU5	–	TV mode selection input	An input pin to select TV standards. L level : NTSC mode H level or open : PAL mode
41	FR	O4MA53		Reset pulse output	A pulse to reset the charge of output circuit. Connect to ϕ_R pin of CCD through the DC offset circuit. The output phase of FR is selected by serial data.
42	FH_{1B}	O4MA52		Horizontal transfer pulse output 1B	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H1B} pin of CCD.
43	GND	–	–	Ground	A grounding pin.
44	V_{DD5}	–	–	Power supply	Supply of +5 V power.
45	FH_1	O4MA53		Horizontal transfer pulse output 1	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H1} pin of CCD.
46	FH_2	O4MA53		Horizontal transfer pulse output 2	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H2} pin of CCD.
47	FH_{2B}	O4MA52		Horizontal transfer pulse output 2B	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H2B} pin of CCD.
48	GND	–	–	Ground	A grounding pin.

SAD_1	L	H or open	L	H or open
SAD_2	L	L	H or open	H or open
Phase	0˚	60˚ delay	180˚ delay	240˚ delay

IC3 : Input pin (CMOS level)
ICU3 : Input pin (CMOS level with pull-up resistor)
ICSU3 : Input pin (CMOS schmitt-trigger level with pull-up resistor)
ICU5 : Input pin (CMOS level with pull-up resistor)
ICD5 : Input pin (CMOS level with pull-up resistor)
O4MA3 : Output pin (V_{DD} = 3.3 V)
O4MA32 : Output pin (V_{DD} = 3.3 V)
O4MA52 : Output pin (V_{DD} = 5 V)
O4MA53 : Output pin (V_{DD} = 5 V)
O12MHV : Output pin (V_{DD} = 12.5 V)
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

Serial Data Control

SERIAL DATA INPUT TIMING



The serial data ED_1 is shifted by ED_0 and is latched at the rising edge of ED_2.
The shutter mode data SMD_1 and SMD_2 of serial data are latched at the rising edge of the horizontal line in which VTG is active, the shutter speed data SD_0 to SD_8 are latched at the rising edge of the next horizontal line in which VTG is active.

SERIAL DATA INPUTS

DATA	NAME	FUNCTIONS
D_{00}	SD_0	Electronic shutter speed control
D_{01}	SD_1	
D_{02}	SD_2	
D_{03}	SD_3	
D_{04}	SD_4	
D_{05}	SD_5	
D_{06}	SD_6	
D_{07}	SD_7	
D_{08}	SD_8	

DATA	NAME	FUNCTIONS
D_{09}	SMD_1	Electronic shutter mode control
D_{10}	SMD_2	
D_{11}	MR_1	Phase control
D_{12}	MR_2	
D_{13}	MC_1	
D_{14}	MC_2	
D_{15}	MS_1	
D_{16}	MS_2	
D_{17}	MF_1	
D_{18}	MF_2	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD3}, V_{DD5}	−0.3 to +6.0	V
	V_{DD12}	−0.3 to +15.0	V
Input voltage	V_{I3}	−0.3 to V_{DD3} + 0.3	V
	V_{I5}	−0.3 to V_{DD5} + 0.3	V
Output voltage	V_{O3}	−0.3 to V_{DD3} + 0.3	V
	V_{O5}	−0.3 to V_{DD5} + 0.3	V
	V_{O12}	−0.3 to V_{DD12} + 0.3	V
Operating temperature	T_{OPR}	−20 to +70	˚C
Storage temperature	T_{STG}	−55 to +150	˚C

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD3} = 3.3±0.33 V, V_{DD5} = 5.0±0.5 V, V_{DD12} = 12.5±0.5 V, T_{OPR} = −20 to +70 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL3}				$0.3V_{DD3}$	V	1, 2
Input "High" voltage	V_{IH3}		$0.7V_{DD3}$			V	
Input "Low" voltage	V_{IL5}				1.5	V	4, 5
Input "High" voltage	V_{IH5}		3.5			V	
Input "Low" voltage	V_{T+}				$0.75V_{DD3}$	V	3
Input "High" voltage	V_{T-}		$0.02V_{DD3}$			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		$0.045V_{DD3}$			V	
Input "Low" current	$\lvert I_{IL3-1} \rvert$	V_I = 0 V			1.0	µA	1
Input "High" current	$\lvert I_{IH3-1} \rvert$	$V_I = V_{DD3}$			1.0	µA	
Input "Low" current	$\lvert I_{IL3-2} \rvert$	V_I = 0 V	3.0		30	µA	2, 3
Input "High" current	$\lvert I_{IH3-2} \rvert$	$V_I = V_{DD3}$			2.0	µA	
Input "Low" current	$\lvert I_{IL5-1} \rvert$	V_I = 0 V	8.0		60	µA	4
Input "High" current	$\lvert I_{IH5-1} \rvert$	$V_I = V_{DD5}$			2.0	µA	
Input "Low" current	$\lvert I_{IL5-2} \rvert$	V_I = 0 V			2.0	µA	5
Input "High" current	$\lvert I_{IH5-2} \rvert$	$V_I = V_{DD5}$	8.0		60	µA	
Output "Low" voltage	V_{OL3-1}	I_{OL} = 1.5 mA			0.4	V	6
Output "High" voltage	V_{OH3-1}	I_{OH} = −1.5 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-2}	I_{OL} = 2 mA			0.4	V	7
Output "High" voltage	V_{OH3-2}	I_{OH} = −1.5 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-3}	I_{OL} = 4 mA			0.4	V	8
Output "High" voltage	V_{OH3-3}	I_{OH} = −3 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL5-1}	I_{OL} = 9 mA			0.4	V	9
Output "High" voltage	V_{OH5-1}	I_{OH} = −6 mA	V_{DD5} − 0.5			V	
Output "Low" voltage	V_{OL5-2}	I_{OL} = 12 mA			0.4	V	10
Output "High" voltage	V_{OH5-2}	I_{OH} = −9 mA	V_{DD5} − 0.5			V	
Output "Low" voltage	V_{OL12}	I_{OL} = 12 mA			0.4	V	11
Output "High" voltage	V_{OH12}	I_{OH} = −12 mA	V_{DD12} − 0.5			V	

NOTES :

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICU3).
3. Applied to input (ICSU3).
4. Applied to input (ICU5).
5. Applied to input (ICD5).
6. Applied to output (OSCO3). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or V_{DD3}.)
7. Applied to output (O4MA3).
8. Applied to output (O4MA32).
9. Applied to output (O4MA52).
10. Applied to output (O4MA53).
11. Applied to output (O12MHV).

PACKAGE

(Unit : mm)

48 QFP (QFP048-P-0707)