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MC92602

Quad 1.25 Gbaud

Reduced Interface SERDES

Reference Manual

Devices Supported:
MC92602ZTA

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Motorola Japan Ltd.
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About This Book

The primary objective of this reference manual is to describe the functionality of the MC92602 for software and hardware developers.

Information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

Audience

It is assumed that the reader has the appropriate general knowledge regarding the design and layout requirements for high speed (Gbps) digital signaling and understanding of the basic principles of Ethernet and Fibre Channel communications protocols to use the information in this manual.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Introduction," gives an overview of the device features and shows a block diagram of the major functional blocks of the part.
- Chapter 2, "Transmitter," describes the MC92602 transmitter, its interfaces and operational options.
- Chapter 3, "Receiver," gives a description of the receiver.
- Chapter 4, "Rate Adaption of Packet Data Streams," describes how rate adaption is performed when receiving Ethernet packets.
- Chapter 5, "System Design Considerations," describes the system considerations for the MC92602, including clock configuration, device startup and initialization, and proper use of the configuration control signals.
- Chapter 6, "Test Features," covers the JTAG implementation and the system accessible test modes.
- Chapter 7, "Electrical Specifications and Characteristics," describes the DC and AC electrical characteristics.

- Chapter 8, “Package Description,” provides the package parameters and mechanical dimensions and signal pin to ball mapping tables for the MC92602 device.
- Appendix A, “Ordering Information,” provides the Motorola part numbering nomenclature for the MC92602 transceiver.
- Appendix B, “8B/10B Coding Scheme,” provides tables of the fibre channel-specific 8B/10B encoding and decoding is based on the ANSI FC-1 fibre channel standard.
- “Glossary of Terms and Abbreviations” contains an alphabetical list of terms, phrases, and abbreviations used in this book.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

General Information

The following documentation, published by Morgan-Kaufmann Publishers, 340 Pine Street, Sixth Floor, San Francisco, CA, provides useful information about the PowerPC architecture and computer architecture in general:

- *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition, by International Business Machines, Inc.

  For updates to the specification, see http://www.austin.ibm.com/tech/ppc-chg.html.
- *Computer Architecture: A Quantitative Approach,* Second Edition, by John L. Hennessy and David A. Patterson
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, David A. Patterson and John L. Hennessy

Related Documentation

Motorola documentation is available from the sources listed on the back cover of this manual; the document order numbers are included in parentheses for ease in ordering:

- Reference manuals—These books provide details about individual device implementations. The *MC92602DVB Reduced Interface SERDES Design Verification Board Reference Manual* (MC92602DVBRM/D) describes how to use the design verification board and should be read in conjunction with this manual, the *MC92602 Quad 1.25 Gbaud Reduced Interface SERDES Reference Manual* (MC92602RM/D).
- Addenda/errata to reference manuals—Because some devices have follow-on parts an addendum is provided that describes the additional features and functionality changes. These addenda are intended for use with the corresponding reference’s manuals.

- Hardware specifications—Hardware specifications provide specific data regarding bus timing, signal behavior, and AC, DC, and thermal characteristics, as well as other design considerations. This manual contains all the hardware specifications for the MC92602.
- Application notes—These short documents address specific design issues useful to programmers and engineers working with Motorola processors.
- White Paper-These documents provide detail on a specific design platform and are useful to programmers and engineers working on a specific product. *MC92610 3.125 Gbaud Reference Design Platform* (BR1570/D) describes the technical design process used in developing a high-speed backplane reference design.
- Additional literature is published as new processors become available. For a current list of documentation, refer to http://www.motorola.com/semiconductors.

Conventions

This document uses the following notational conventions:

	Book titles in text are set in italics
	Internal signals are set in italics, for example, *loop_back_data*
0x	Prefix to denote hexadecimal number
0b	Prefix to denote binary number
x	In some contexts, such as signal encodings, an un-italicized x indicates a don’t care.
x	An italicized *x* indicates an alphanumeric variable.
n	An italicized *n* indicates an numeric variable.

Signals

A bar over a signal name indicate that the signal is active low—for example, $\overline{\text{XMIT\_A\_IDLE}}$ and $\overline{\text{XMIT\_B\_IDLE}}$. Active low signals are referred to as asserted (active) when they are low and negated when they are high. Signals that are not active low, such as XMIT_EQ_EN and DROP_SYNC are referred to as asserted when they are high and negated when they are low.

Chapter 1
Introduction

This reference manual explains the functionality of the MC92602 Quad 1.25 Gbaud Reduced Interface SERDES transceiver and enables its use by software and hardware developers. The audience for this publication, therefore, consists of hardware designers and application programmers who are building data path switches and high-speed backplane intercommunication applications. The remainder of this document will refer to the term reduced interface as DDR.

1.1 Overview

The MC92602 is a high-speed, full-duplex, serializer/deserializer (SERDES) data interface device that can be used to transmit data between chips across a board, through a backplane, or through cabling. The MC92602 has four transceivers that transmit and receive coded data at a rate of 1.0 gigabit per second (Gbps) through each 1.25 gigabaud link. The MC92602 is designed specifically for high-density board applications where reduction of interface signals is a primary concern.

The MC92602 is built upon the proven transceiver technology in the Quad MC92600 device and is carefully designed for low power consumption. Its 0.25µ CMOS implementation nominally consumes approximately 1.2 Watts with all links operating at full speed.

Signal I/O count is reduced relative to the MC92600 device by operating the parallel interfaces at 125 MHz Double Data Rate (DDR) 4-bits wide per channel, per direction. HSTL class-I source terminated I/O is an accepted signalling method for 125 MHz DDR data for FR-4 board traces up to 8 inches. The MC92602 also includes the addition of transmit FIFOs and source-synchronous transmit clocks per channel to further simplify interfacing. This aggressive signaling scheme and packaging in a 196 pin fine pitch BGA offers excellent board density without making unreasonable signal integrity demands of the ASIC device to which it interfaces.

An **IEEE Std 802.3 - 2002** ® compatibility mode has been included to enable non-intrusive operation with packet streams. And finally, **IEEE Std 1149.1** ™ JTAG boundary scan and built in PRBS generator/analyzers are provided for board test support.

1.2 Features

The following are the features of the MC92602:

- General Features
  - — Four full-duplex differential data links.
  - — Selectable speed range: 1.25 Gbaud or 0.625 Gbaud.
  - — Rate adaption compatibility with packet data streams
  - — Context sensitive rate adaption during receipt of idle and data code groups
  - — Supports Jumbo frame lengths of up to 16K BYTES
  - — Supports frame bursting
  - — Differential reference clock input with single-ended clock input option.
  - — Low power, approximately 1.2W under typical conditions, while operating all transceivers at full speed.
  - — Unused transceiver channels may be individually disabled.
  - — IEEE 1149.1 JTAG support and full-speed built in self test, (BIST), functions.
  - — Package: 196pin MAPBGA (15x15mm body size, 1.0 mm ball pitch).
- Data Interface Features
  - — Internal 8B10B encoder/decoder that may be bypassed in Ten-Bit Interface mode where external coding is used.
  - — Double Data Rate (DDR), source synchronous, 4-bit and 5-bit HSTL Class-I parallel interfaces.
  - — Transmit data clock is selectable between per-channel transmit clock or channel ‘A’ transmit clock.
  - — Link-to-link synchronization supports aligned, multi-channel, word transfers. The synchronization mechanism tolerates up to 40 bit-times of link-to-link media skew.
  - — Selectable Idle character alignment mode enables aligned transfers with automatic realignment or unaligned data transfers (if in 10 bit mode).
  - — Received data may be clocked to the recovered clock or to the reference clock frequencies.
  - — Compatibility mode enables non-intrusive operation with packet data streams.
- Link Interface Features
  - — Drives 50Ω or 75Ω media (100Ω or 150Ω differential) for lengths of up to 1.5 meters board/backplane, or 10 meters of coax.
  - — Link inputs have on-chip receiver termination and are “hot swap” compatible.
  - — Tolerates a frequency offset between the transmitter and receiver in excess of $\pm$250ppm.

1.3 Block Diagram

The MC92602 is a highly integrated device containing all of the logic needed to facilitate the application and test of a high-speed serial interface. No external components, other than the normal power supply decoupling network are required.

A block diagram of the MC92602 device is shown in Figure 1-1.

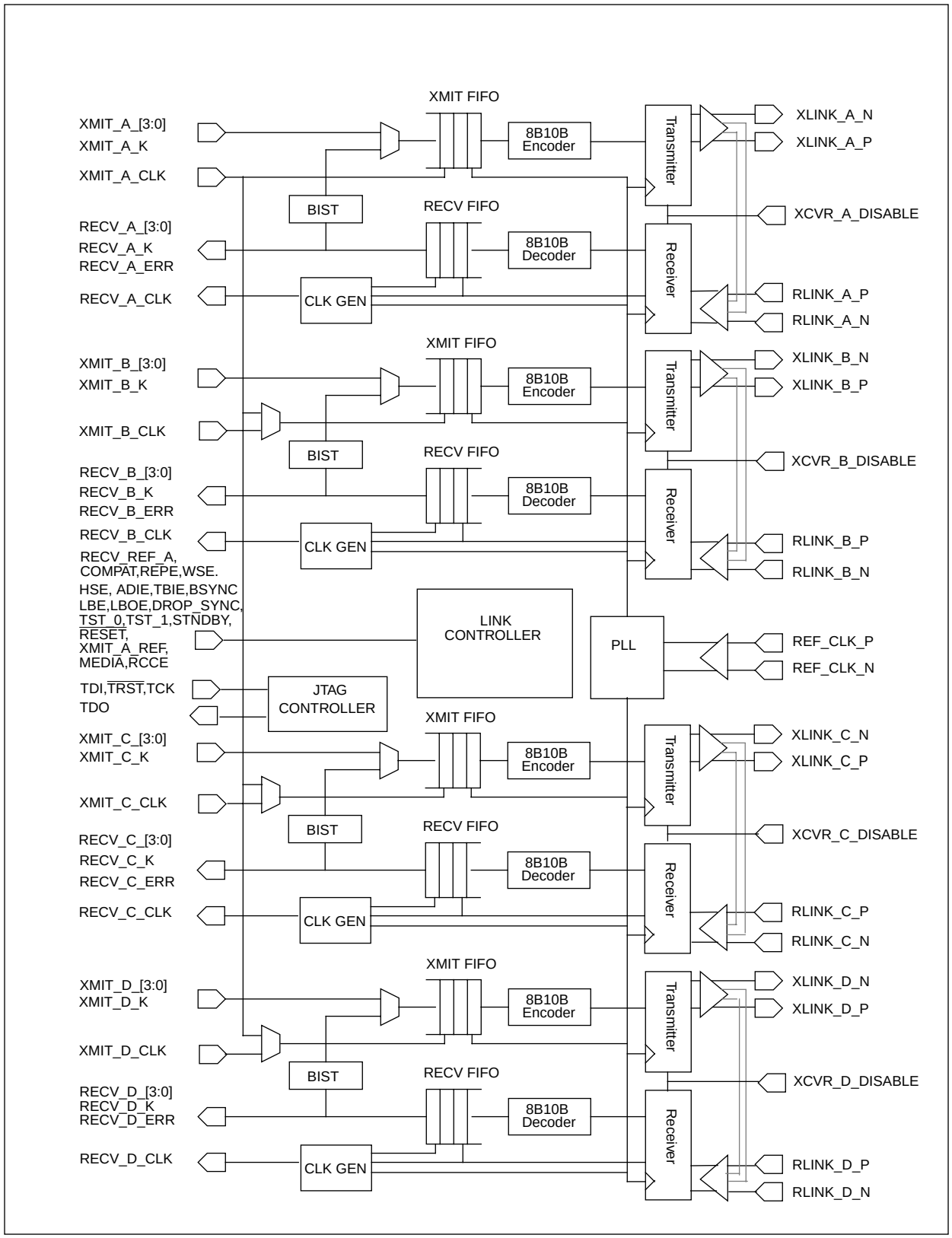


Figure 1-1. MC92602 Block Diagram

1.4 References

This section contains the indexed references in the document.

[1] *Fibre Channel, Gigabit Communications and I/O for Computer Networks*, Brenner, 1996.

[2] *Byte Oriented DC Balanced 8B/10B Partitioned Block Transmission Code*, U.S. Patent #4,486,739, Dec. 4, 1984.

[3] *High Speed Transceiver Logic (HSTL), A 1.5V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits*, EIA/JEDIC Standard EIA/JESD8-6, Aug. 1995.

[4] *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Std. 1149.1-1990 (Includes IEEE Std. 1149.1a-1993), Oct. 1993.

[5] *IEEE Standard Carrier Sense Multiple-Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*, IEEE Std. 802.3-2000.

1.5 Revision History

Table 1-1 contains a brief description of the technical updates made to this document.

Table 1-1. MC92602 SERDES Reference Manual Revision History

Revision Level	Change
0	First release of the MC92602 SERDES reference manual.

Chapter 2
Transmitter

This chapter describes the MC92602 transmitter, its interfaces and operation. The chapter consists of the following sections:

- Section 2.1, “Transmitter Block Diagram”
- Section 2.2, “Transmitter Interface Signals”
- Section 2.3, “Functional Description.”

The transmitter takes data presented at its source synchronous parallel data input port, creates an encoded transmission character (if not pre-encoded), and serially transmits the character out of the differential link output pads. A detailed explanation of the 8B/10B coding scheme is offered in Appendix B, “8B/10B Coding Scheme.”

2.1 Transmitter Block Diagram

Figure 2-1 shows a block diagram of the MC92602 transmitter.

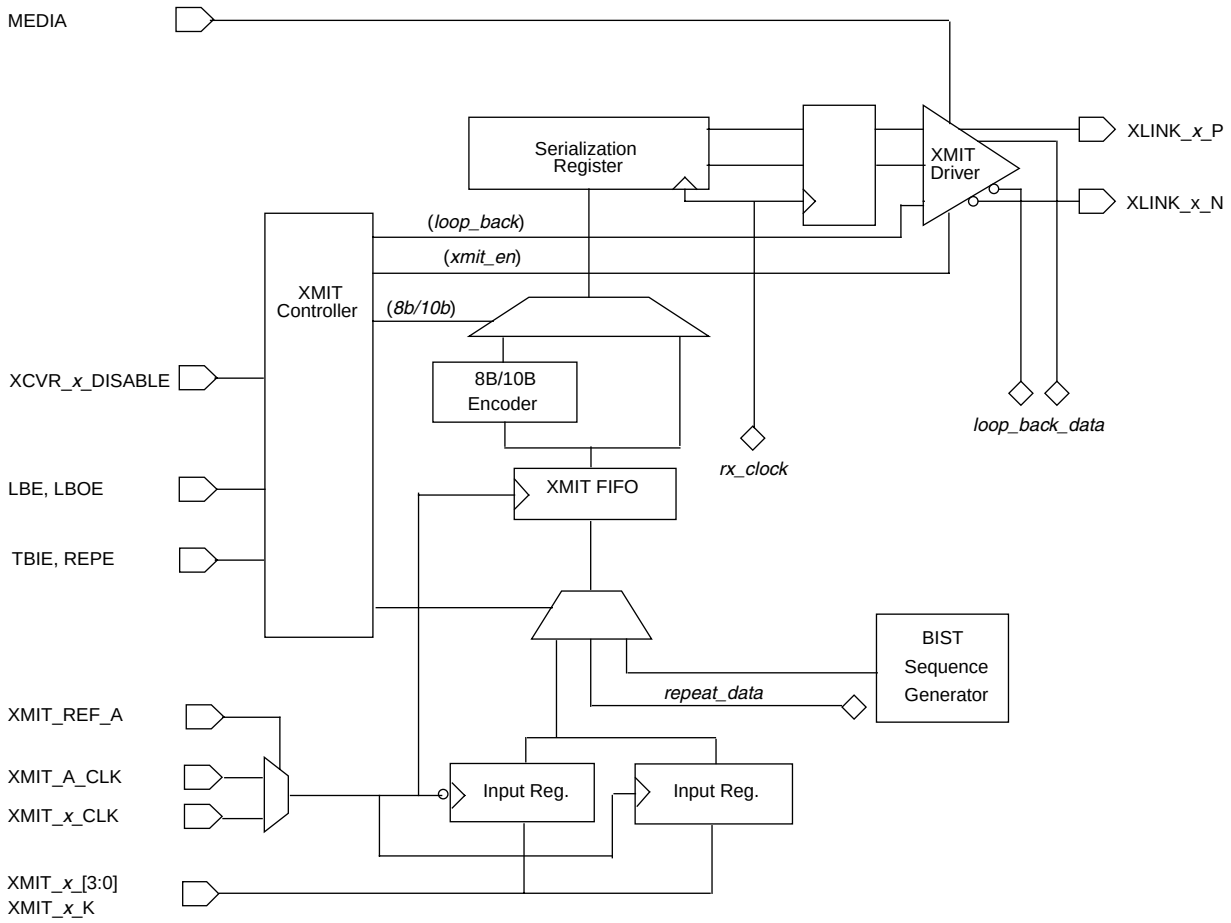


Figure 2-1. MC92602 Transmitter Block Diagram

2.2 Transmitter Interface Signals

This section describes the interface signals of the MC92602 transmitters. Each signal is described, including its name, function, direction, and active state in Table 2-1. The table's signal names use the letter "*x*" as a place holder for the Link identifier letter "A" through "D". Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 2-1. MC92602 Transmitter Interface Signals

Signal Name	Description	Function	Direction	Active State
XMIT_*x*_3 through XMIT_*x*_0	Transmit Nibble	If TBIE is low these are 4 bits of uncoded data to transmit. Bits 3 through 0 on rising edge of clock. Bits 7 through 4 on falling edge of clock. If TBIE is high these 4 bits are coded data to transmit. Bits 3 through 0 on rising edge of clock. Bits 8 through 5 on falling edge of clock.	Input	-
XMIT_*x*_K	Transmit Control Bit	If TBIE is low this is the “K” (special char) input on the rising edge of clock and the IDLE (Idle indicator) on the falling edge of clock. If TBIE is high this is data bit 4 on the rising edge of clock and data bit 9 on the falling edge of clock	Input	-
XMIT_*x*_CLK	Channel Transmit Clock	Clock to which transmit interface signals are timed.	Input	-
XMIT_REF_A	Transmit Interface Clock Select	Indicates that the transmit interface signals are timed to XMIT_A_CLK instead of their own transmit clock.	Input	High
XCVR_*x*_DISABLE	Transceiver Disable	Indicates that the transmitter and receiver for this transceiver are disabled. The link outputs are not driven. (see Section 2.3.4 for details).	Input	High
TBIE	Ten-Bit Interface Enable	Indicates that pre-coded 10-bit data is at inputs and to bypass internal 8B/10B coding.	Input	High
REPE	Repeater Mode Enable	Test feature only. Must be disabled (low) during normal operation.	Input	High
HSE	Half Speed Enable	When enabled, link is operated at half-speed. Both data and link interfaces run at half speed.	Input	High
LBE	Loop Back Enable	Activate digital loopback path, such that data transmitted is looped back to its receiver.	Input	High
LBOE	Loop Back Output Enable	Indicates that link outputs remain active when LBE is asserted. When LBOE is low, link outputs are disabled when LBE is asserted.	Input	High
TST_1, TST_0	Test mode config inputs	Decoded to define various test modes (see Chapter 6 for details).	Input	-
MEDIA	Media Impedance Select	Indicates the impedance of the transmission media. Low indicates 50Ω and high indicates 75Ω.	Input	-

Table 2-1. MC92602 Transmitter Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
XLINK_*x*_N/ XLINK_*x*_P	Link Serial Transmit Data	Differential serial transmit data output pads.	Output	-
Internal Signals				
rx_clock	High Speed Transceiver Clock	Internal, differential high speed clock used to transmit and receive link data.	Input	-
repeat_data	Repeater Data	Internal data from the receiver to be used when REPE is active.	Input	-
loop_back_data	Loop Back Data	Differential loop back transmit data.	Output	-

2.3 Functional Description

The transmitter takes the data byte presented at its data input, creates a transmission character using its 8B/10B encoder (if not in Ten-Bit Interface mode), and serially transmits the character out of the differential link output pads. The following sections provide a detailed description of the transmitter and its various modes of operation.

2.3.1 Transmit Data Input Register Operation

Transmit data is sampled and stored in the input register on the rising and falling edge of the appropriate transmit clock. This results in the accumulation of 10 transmit bits per complete clock cycle.

The transmit data input register accepts data to be transmitted and synchronizes it to the internal clock domain. Transmit data may be uncoded 8-bit data or coded 10-bit data, depending upon the state of the control input, TBIE. The Ten-Bit Interface mode, TBI, is enabled by asserting Ten-Bit Interface Enable, TBIE, high. Table 2-2 and Table 2-3 describe the meaning of each transmit data bit depending upon the state of TBIE.

Table 2-2. Conversion of Transmitter Inputs to Internal Transmit Data (TBIE = low)

Clock Edge	XMIT_*x*_K	XMIT_*x*_3	XMIT_*x*_2	XMIT_*x*_1	XMIT_*x*_0
Rising	K	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Falling	$\overline{\text{Idle}}$	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4

Table 2-3. Conversion of Transmitter Inputs to Internal Transmit Data (TBIE = high)

Clock Edge	XMIT_*x*_K	XMIT_*x*_3	XMIT_*x*_2	XMIT_*x*_1	XMIT_*x*_0
Rising	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Falling	Data Bit 9 (MSB)	Data Bit 8	Data Bit 7	Data Bit 6	Data Bit 5

2.3.1.1 Transmitting Uncoded Data

If TBIE is low the transmit data is to be treated as uncoded 8 bit data, that must be encoded by the on-chip 8B/10B encoder. 8B/10B coding ensures DC balance across the link and sufficient transition density to facilitate reliable data recovery.

The state of XMIT_*x*_K on the rising edge of the transmit clock will be referred to as the "K" bit. The state of XMIT_*x*_K on the falling edge of the transmit clock will be referred to as the "$\overline{\text{Idle}}$" bit. Data transmitted as a function of these two bits are as indicated in Table 2-4.

If K is low this 8 bit data is then coded into a 10-bit data character.

If K is high and $\overline{\text{Idle}}$ is low, then the remaining data bits are ignored and the on-chip 8B/10B encoder creates an IDLE character (K28.5) with the appropriate disparity.

Special control codes may be transmitted by asserting K high, and $\overline{\text{Idle}}$ high The transmit byte is assumed to be a control code in this state.

Table 2-4. Transmitter Control States (TBIE=low)

$\overline{\text{IDLE}}$	K	Description
Don't care	Low	Transmit data present on internal Data Bits 7 through 0.
Low	High	Transmit Idle (K28.5), ignore internal Data Bits 7 through 0.
High	High	Transmit control present on internal Data Bits 7 through 0.

2.3.1.2 Transmitting Coded Data

Ten-bit coded data may be transmitted, bypassing the internal 8B/10B encoder. The Ten-Bit Interface, TBI, mode is enabled by asserting TBIE high. In this mode, the ten bits of data to transmit are presented on the internal Data Bits 9 through 0 as previously shown in Table 2-3.

Special care must be taken when using TBI mode. The 10-bit pre-coded data must exhibit the same properties as 8B/10B coded data. DC balance must be maintained and there must be sufficient transition density to ensure reliable data recovery at the receiver.

The receiver requires that the K28.5 Idle character be periodically transmitted to enable byte and word synchronization. This 10-bit pattern, '0011111010' or '1100000101' (ordered from least significant bit, bit-0, through most significant bit, bit-9) is used for alignment and channel synchronization when operating in any of the byte or word synchronization modes. The pattern of Idles and data required to achieve byte or word synchronization depends on the configuration of the receiver. The appropriate sequence must be applied through the Ten-Bit Interface.

2.3.1.3 Transmit Interface Clock Configuration

The transmitter data interface operates at high frequency (up to 125MHz double data rate). Data is clocked into the transmitter on both the rising and falling edges of the transmit clock. In order to ease development of devices that interact with the MC92602, all of its data interfaces are source-synchronous. The data for each transmitter has its own dedicated clock input. This allows the clock at the source of the data to be routed with the data ensuring matched delay and timing. However, if per-transmitter clock sources are not available or deemed unnecessary, all transmitters may be clocked by a common clock source. This is enabled by asserting XMIT_REF_A high. When XMIT_REF_A is high, the XMIT_A_CLK becomes the interface clock for all active channels.

The configuration settings of the MC92602 affect the legal range of clock frequencies at which it may be operated. Table 5-1 shows legal transmit interface clock frequencies for all modes of operation. All transmit interface clock inputs, XMIT_*x*_CLK, and the PLL reference clock, REF_CLK, inputs must have identical frequencies. The transmit data interface tolerates $\pm 180^{o}$ of transmit interface clock phase drift relative to the PLL reference clock.

2.3.2 8B/10B Encoder Operation

The 8B/10B Encoder encodes 8-bit data/control from the input register into 10-bit *transmission characters*. The Fibre Channel 8B/10B coding standard is followed [1,2]. Running disparity is maintained and the appropriate transmission characters are produced, maintaining DC balance and sufficient transition density to allow reliable data recovery at the receiver.

The inputs to the 8B/10B Encoder are the data byte (internal Data Bits 7 through 0), special code signal (K) and transmit idle signal ($\overline{\text{IDLE}}$).

Data and legal control bytes are coded according to the 8B/10B method. Illegal control bytes produce unpredictable transmission characters, which may lead to disparity and coding errors, thereby reducing link reliability.

The 8B/10B encoder produces an Idle character (K28.5) of proper running disparity when K is high and $\overline{\text{IDLE}}$ is low, as indicated in Table 2-4.

The 8B/10B Encoder is bypassed if TBIE is asserted high.

2.3.3 Transmit Driver Operation

The Transmit Driver drives transmission characters serially across the link. Two bits per transceiver clock, one each on the rising and falling transceiver clock (rx_clock) edges, are transmitted differentially from the XLINK_*x*_P/XLINK_*x*_N outputs. The internal *rx_clock* runs at 625 MHz for 1 Gbps (1.25 Gbaud) operation and 312.5 MHz for 500 Mbps (625 Mbaud) operation.

The Transmit Driver is a controlled impedance driver. The impedance of the driver is programmable to 50Ω or 75Ω through the MEDIA signal. Drive impedance is 50Ω when the control signal, MEDIA, is low and 75Ω when MEDIA is high.

2.3.4 Transceiver Disable

Each individual transceiver may be disabled with the appropriate XCVR_*x*_DISABLE signal. The XCVR_*x*_DISABLE control signal also has a secondary function when used in association with the receiver control signal DROP_SYNC that allows external forcing of loss of byte synchronization on an individual channel basis. The relationship of these two control signals is shown in Table 2-5.

Table 2-5. Transceiver Disable - Channel Drop Sync Operation

XCVR_*x*_DISABLE	DROP_SYNC	ACTION
low	low	Transceiver Channel Active - normal operation
high	low	Transceiver channel "*x*" disabled
low	high	Transceiver channel active - normal operation
high	high	Transmitter "*x*" active; Receiver "*x*" is forced to "Drop Sync"

When Drop_Sync is high, XCVR_*x*_DISABLE has no effect on the function of the transmitter. Rather when asserted high it is used to perform the loss of synchronization on the selected channel

NOTE

Since DROP_SYNC and XCVR_*x*_DISABLE are asynchronous signals (relative to the internal clocks) they must be asserted for two or more cocks. DROP_SYNC should be raised prior to XCVR_*x*_DISABLE and lowered after XCVR_*x*_DISABLE. To assure proper action raise DROP_SYNC on clock #1, raise XCVR_*x*_DISABLE on clock #2, lower XCVR_*x*_DISABLE on Clock #n (n must be 4 or greater), then lower DROP_SYNC on Clock #n+1.

2.3.5 Loop-Back Test Mode

A special loop-back mode is supported for test. Asserting LBE high, enables loop-back mode causing the data being driven on the link outputs to be looped back, internally, to the input amplifier of the link's receiver.

Loop-back data is processed the same as normally received data. Loop-back enables at-speed self-test to be implemented for production test and for in-system self-test. The loop-back signals are electrically isolated from the link output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally.

When in loop-back mode, the loop-back output Enable signal, LBOE, controls the action of the link output signals. When LBOE is low, the link outputs are undriven and are high-impedance. When LBOE is high, the link output signals operate normally.

LBOE has no affect on the operation of the device when LBE is low.

See Section 6.2 for more information on system accessible test modes.

2.3.6 Repeater Mode

Repeater mode is not recommended for application use. It is used for factory engineering and manufacturing test purposes only. The repeater enable signal, REPE, should be configured low during normal operation.

Chapter 3
Receiver

This chapter describes the MC92602 receiver, its interfaces, and operation. This chapter has the following sections:

- Section 3.1, “Receiver Block Diagram”
- Section 3.2, “Receiver Interface Signals”
- Section 3.3, “Functional Description”

The receiver is a dual data rate receiver, operating at 1Gbps or 500Mbps rates (1.25 or 0.625 Gbaud) and is based upon an oversampled transition tracking loop data recovery method. The receiver takes a high speed differential serial data stream input, over samples it and recovers the data and clock, decodes it and presents it on a source synchronous, double data rate, reduced interface (5-bit) output data port.

3.1 Receiver Block Diagram

Figure 3-1 shows a block diagram of the MC92602 receiver.

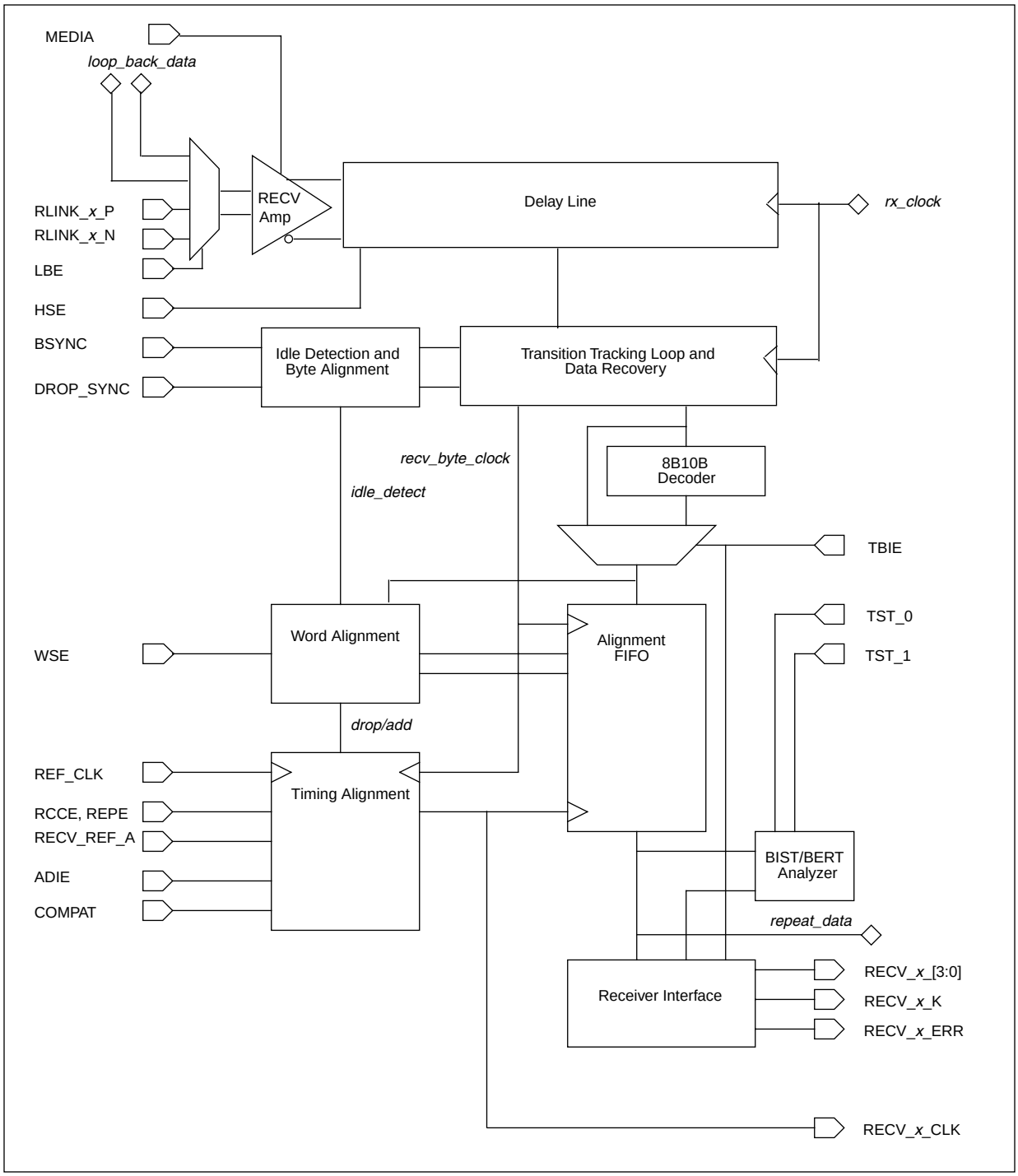


Figure 3-1. MC92602 Receiver Block Diagram

3.2 Receiver Interface Signals

This sections describes the interface signals of the MC92602 receiver. Each signal is described, including its name, function, direction and active state in Table 3-1. The table's signal names use the letter "*x*" as a place holder for the link identifier letter "A" through

“D”. Internal signals are not available at the I/O of the device, but are presented to illustrate device operation.

Table 3-1. MC92602 Receiver Interface Signals

Signal Name	Description	Function	Direction	Active State
RECV_*x*_3 through RECV_*x*_0	Received Nibble	If TBIE is low these are 4 bits of uncoded data received. Bits 3 through 0 on rising edge of clock. Bits 7 through 4 on falling edge of clock. If TBIE is high these 4 bits are coded data received. Bits 3 through 0 on rising edge of clock. Bits 8 through 5 on falling edge of clock.	Output	-
RECV_*x*_K	Special Data Indicator	If TBIE is low, both rising edge and falling edge states are used to encode status out. See Table 3-4. If TBIE is high this is data bit 4 on rising edge and data bit 9 on falling edge.	Output	-
RECV_*x*_ERR	Receiver Error	Receiver status out. If TBIE is low it is used in conjunction with RECV_*x*_K. If TBIE is high then it is the only status bit. See Table 3-6 and Table 3-7.	Output	-
RECV_*x*_CLK	Receiver Clock	Internally generated clock used for reading receiver outputs. This signal may be derived from the REF_CLK, receiver A’s recovered clock, or this receiver’s recovered clock.	Output	-
TBIE	Ten-Bit Interface Enable	Indicates that the Receiver Interface is in ten-bit mode and that the 8B/10B decoder is bypassed.	Input	High
HSE	Half Speed Enable	Indicates to operate link at half-speed. Both data and link interfaces run at half speed.	Input	High
WSE	Word Synchronization Enable	Indicates that all enabled receivers are being used in unison to receive synchronized data.	Input	High
BSYNC	Byte Alignment Mode	Indicates that byte alignment is required, if low no byte alignment is done.	Input	-
RCCE	Recovered Clock Enable	Indicates that the output data is synchronized to a recovered byte clock.	Input	High
REPE	Repeater Mode Enable	Test feature only. Must be disabled (low) during normal operation.	Input	High
RECV_REF_A	Receiver A Clock Enable	Indicates that if RCCE is also high that the data will be synchronized to Channel A’s recovered clock.	Input	High

Table 3-1. MC92602 Receiver Interface Signals (continued)

Signal Name	Description	Function	Direction	Active State
ADIE	Add/Delete Idle Enable	Indicates that the receiver is free to add/delete Idle characters to/from the output data stream to maintain alignment. Special character addition and deletion rules are followed in compatibility mode. See section 3.3.7.2 for more information.	Input	High
COMPAT	Compatibility Mode Enable	Indicates that the receiver follows special character addition and deletion rules to maintain alignment that are non-intrusive to packet data streams. SeeChapter 4, “Rate Adaption of Packet Data Streams,” for more information.	Input	High
LBE	Enable Loopback	Indicates that data into the receiver is to be taken from the local transmitter instead of the RLINK_n_P/N inputs.	Input	High
DROP_SYNC	Drop Synchronization Enable	Enables control such that current byte and word alignment be invalidated and new alignment acquired. DROP_SYNC enables XCVR_*x*_DISABLE to force loss of alignment.	Input	High
XCVR_*x*_DIASABLE	XCRV Disable or channel drop sync.	Asserted when DROP_SYNC is high will invalidate current byte and word alignment. (see Section 2.3.4)	Input	High
TST_0/ TST_1	Test Mode	Indicates operating/test mode of the chip. See Chapter 6.	Input	-
REF_CLK_P/N	PLL Reference Clock	PLL input reference clock. Provides reference frequency for the receiver interface when Recovered Clock mode is disabled (RCCE is low).	Input	-
RLINK_*x*_N/ RLINK_*x*_P	Link Serial Receive Data	Differential serial receive data input pads.	Input	-
Internal Signals				
rx_clock	High Speed Clock	Internal, differential high speed clock used to transmit and receive link data.	Input	-
loop_back_data	Loop Back Data	Differential loop back receive data.	Input	-
repeat_data	Repeater Data	Data received that is available to the transmitter if in repeater mode (REPE is high)	Output	-

3.3 Functional Description

The MC92602 receiver receives differential data in one of two operating ranges. It may be operated in full rate range with a maximum data rate of 1.0 Gbps (1.25 gigabaud) or at

half-rate at 500 Mbps (0.625 gigabaud). The operating range is determined by the state of the HSE input and the frequency of the reference clock, see Table 5-1.

Transmitted data is recovered using an oversampled transition tracking method. The received serial data is accumulated into ten-bit characters. The ten-bit characters are forwarded to the 8B/10B decoder where the original data is obtained. Alternately, the decoder can be bypassed and the ten-bit character is forwarded to the Receiver Interface in the ten-bit interface (TBI) mode.

The receiver provides for byte (character) alignment. Alignment assures that the byte as presented at the input of the transmitter is preserved when the byte is presented by the receiver. Optionally, alignment may be disabled.

The receiver also provides for word synchronization. In this mode, all of the receivers are being used cooperatively to receive 32-bit (40 bit in TBI mode) words. Word synchronization assures that the receivers present the four bytes of a word simultaneously.

The Receiver Interface, where the received bytes and status codes are obtained, has several modes of operation and timing to allow it to be used in a variety of applications. The following sections provide a detailed description of the receiver and its modes of operation.

3.3.1 Input Amplifier

The input amplifiers connect directly to the link input pads RLINK_*x*_P and RLINK_*x*_N. It is a differential amplifier with integrated analog multiplexer for loop-back testing. Link termination resistors are integrated with the amplifier. The termination resistance is either 100Ω or 150Ω differential depending upon the state of the MEDIA input.

The input amplifier facilitates a loop-back path for production and in-system testing. When the MC92602 is in loop-back mode (Loop Back Enable, LBE, is high), the input amplifier selects the loop-back differential input signals and ignores the state on the RLINK_*x*_P and RLINK_*x*_N signals. This allows in-system loop-back BIST independent of the current input state. See Chapter 6 for more information on test modes.

3.3.2 Transition Tracking Loop and Data Recovery

The received differential data from the input amplifier is sent to the transition tracking loop for data recovery. The MC92602 uses an oversampled transition tracking loop method for data recovery. The differentially received data is sampled and processed digitally providing for low bit error rate (better than 10 -12) data recovery of a distorted bit stream.

The transition tracking loop is tolerant of frequency offset between the transmitter and receiver. The MC92602 reliably operates with ±250 ppm of frequency offset. The transition tracking loop method is different than the typical PLL clock recovery method. Its receiver compensates for overrun and underrun due to frequency offset by modulating the

duty-cycle and period of the received byte clock such that it matches the frequency of the received data (see Section 3.3.7.1 for more information).

Recovered data is accumulated into 10-bit characters. The characters are aligned to their original 10-bit boundaries if a Byte Alignment mode is enabled.

3.3.3 Byte Alignment

The receiver supports two modes of Byte Alignment as defined by the BSYNC signal. Table 3-2 shows the settings to activate each mode.

Table 3-2. Byte Synchronization Modes

Byte Alignment Mode	BSYNC
Byte Aligned	High
Non-Aligned	Low

3.3.3.1 Byte-Aligned

At power-up, the receiver starts an alignment procedure, searching for the 10-bit pattern defined by the 8B/10B Idle code. Synchronization logic checks for the distinct Idle sequence, ‘0011111010’ and ‘1100000101’ (ordered bit 0 to bit 9), characteristic of the K28.5 Idle pattern. The search is done on the 10-bit data in the receiver, and is therefore independent of the TBIE input. Alignment requires a minimum of four, error-free, received Idle characters to ensure proper alignment and lock. Non-Idle characters may be interspersed with the Idle characters. The disparity of the Idle characters is not important to alignment and can be positive, negative or any combination.

The receiver begins to forward received characters once locked on an alignment. However, if Word Synchronization Enable is asserted, WSE=high, received characters are not forwarded to the Receiver Interface until the first, valid, non-idle character is received. Alignment remains locked until any one of three events occur that indicate loss of alignment:

- Alignment is lost when a misaligned Idle sequence is detected. A misaligned Idle sequence is defined as four Idle characters with an alignment different than the current alignment. Non-Idle characters may be dispersed between the four misaligned Idles, however, a properly aligned Idle character breaks the sequence. Although alignment is lost by this condition, the receiver automatically changes alignment to the newly detected alignment. However, status out will be reported as “Not Byte Sync” as described in Section 3.2.6.6 for a few recovered clocks to allow the receiver FIFO to re-align. Data will be lost while “Not Byte Sync” status is being reported. The actual number of clocks that “Not Byte Sync” will be reported will vary depending upon the number of bytes in the FIFO when realignment occurs.

- Alignment is also lost when the number of received characters with 8B/10B coding errors outnumbers the non-errored characters by four. Credit for non-errored characters in excess of errored characters is limited to four, such that alignment is lost after four consecutive errored characters. Misalignment detection of this type is not available in TBI mode. The receiver restarts its alignment procedure and halts data flow until a new alignment is established.
- Alignment is lost when DROP_SYNC followed by XCVR_*x*_DISABLE are both asserted high for at least two clocks (see Section 2.3.4 for details on performing drop sync). Current alignment is invalidated, the receiver restarts its alignment procedure and halts data flow until a new alignment is achieved.

When establishing byte alignment, or when data flow is halted due to misalignment, the "Not Byte Sync" error is reported as described in Section 3.3.6.3.

3.3.3.2 Non-Aligned

In this mode no attempt is made to align the incoming data stream. The bits are simply accumulated into 10-bit characters and forwarded. This mode should be used only with Ten-Bit Interface mode, TBIE set high, and with Word Synchronization disabled, WSE set low.

3.3.4 Word Synchronization

The four receivers in the MC92602 can be used cooperatively to receive aligned multi-channel word transfers. Word alignment is enabled by asserting Word Synchronization Enable input, WSE, high.

Word synchronization is possible in Byte Interface mode or in TBI mode. However, word synchronization is dependent on the detection of simultaneously transmitted word synchronization events that contain Idle characters. Therefore, if operating in TBI mode, the Idle character must be a supported member of the code set.

If WSE is high, then all enabled receivers (those that have XCVR_*x*_DISABLE set low) will be aligned into a 16, 24, or 32 bit word (depending upon the states of the various XCVR_*x*_DISABLE signals). If the receiver on Channel A is disabled, then do not select the clock from Channel A as the recovered clock for all the channels.

The word synchronization event is four (or more) consecutive (K28.5) Idles followed by a non-Idle. Word synchronization events must be generated at all concerned transmitters simultaneously in order for synchronization to be achieved. Word synchronization events must be received at all concerned receivers within 40 bit-times of each other.

Word synchronization events are used to establish a relationship between the received bytes in each of the receivers. The bytes of a word are matched and presented simultaneously at the Receiver Interface. Once synchronization is achieved the receiver tolerates $\pm$6 bit-times

of drift between receivers. If drift exceeds ±6 bit-times the receiver will continue to operate. However, the received bytes will no longer be synchronized properly because the receiver remains locked on the initially established synchronization. Word synchronization remains locked until an event occurs that indicates loss of synchronization.

Word synchronization lock is lost when one or more of the receivers change or lose byte alignment (byte alignment loss is described in Section 3.3.3.1). Lock is also lost when overrun/underrun is detected on one or more of the receivers, see Section 3.3.7.1 for more about overrun/underrun.

Word synchronization lock is lost when explicitly invalidated by asserting DROP_SYNC and XCVR_*x*_DISABLE high for at least two clocks (see Section 2.3.4 for details on performing drop sync). When lock is lost, word synchronization must be re-established before data flow through the receiver resumes.

The Receiver Interface is disabled during initial word synchronization. No data is produced at its outputs until word synchronization is achieved and the first non-idle character is received. When establishing word synchronization, or when word synchronization is lost, “Not Word Sync” error is reported as described in Section 3.3.6.3.

3.3.4.1 Recommended Settings for Word Synchronization

Word synchronization can only be used with certain operating modes and has limited application in others. Table 3-3 describes the relationship between modes and word synchronization.

Table 3-3. Word Synchronization Settings

Mode	Signals	Recommended State	Description
Word Synchronization	WSE	High	Enables word synchronization.
Byte Synchronization	BSYNC	High	Word synchronization depends upon Idle character detection. Byte alignment is required for Idle detection.
Add/Delete Idle	ADIE	High	When enabled, allows the receiver to add/delete Idle patterns in order to maintain word synchronization. This is the recommended operating mode when the Reference Clock is used to time the receiver interface (RCCE set low) and there is a frequency offset between the transmitter and receiver. Idles are added or dropped to maintain word alignment.
ICompatibility Mode	COMPAT	Low	Word synchronization is not supported in compatibility mode.
Ten-Bit Interface	TBIE	n/a	When enabled, the Idle character must be part of the TBI code set. When disabled, the Idle is naturally supported by the 8B/10B codes.

Table 3-3. Word Synchronization Settings (continued)

Mode	Signals	Recommended State	Description
Recovered Clock	RCCE	n/a	Does not affect word synchronization.
Receiver A recovered Clock select	RECV_REF_A	High (if RCCE is high)	RECV_REF_A must be high if RCCE is enabled. The receiver A's recovered clock must be used for all receivers. The data at the receiver interfaces will be skewed if the individual receiver recovered clocks are used to time the receiver interfaces.
Half-Speed Enable	HSE	n/a	Does not affect word synchronization.

3.3.5 8B/10B Decoder

The 8B/10B decoder takes the 10-bit character from the Transition Tracking Loop and decodes it according to the 8B/10B coding standard [1,2]. The decoder does two types of error checking. First it checks that all characters are a legal member of the 8B/10B coding space. The decoder also checks for running disparity errors. If the running disparity exceeds the limits set in the 8B/10B coding standard then a disparity error is generated.

An illegal character or disparity error results in a “Code Error” or “Disparity Error” being reported as described in Section 3.3.6.3. It is difficult to determine the exact byte that causes a disparity error, so the error should not be associated with a particular received byte. It is rather a general indicator of the improper operation of the link. Its intended use is for the system to monitor link reliability.

The 8B/10B decoder is bypassed when operating in Ten-Bit Interface mode (TBIE set high.)

NOTE

8B/10B coding is meant only to improve data transmission characteristics and is not a good error detection code. Many 8B/10B characters alias to other valid 8B/10B characters in the presence of bit errors. Error detection and correction techniques must be applied outside of the MC92602 if better than 10^{-12} bit error rate is required.

3.3.6 Receiver Interface

Data in the alignment FIFO is presented at the Receiver Interface as double data rate, DDR, on the rising and falling edge of the appropriate receiver clock, RECV_*x*_CLK. Along with the data, information is also provided on the status of the link. Table 3-1 describes each of the signals involved in receiver operation.

The Receiver Interface, through which received data is obtained, may be operated in Byte mode or in Ten-Bit Interface mode. There are several timing mode options for the receiver interface. Each of the operating modes are described below.

3.3.6.1 Byte Interface

The Receiver Interface may be operated in Byte mode or in Ten-Bit Interface, TBI, mode. Received data is a byte (8 bits) of uncoded data when in Byte mode. The internal 8B/10B decoder is used to decode data from the 10-bit character received. Byte interface mode is enabled by setting TBIE low.

Table 3-4, shows how data and status will appear on the receiver interface when in Byte Mode.

Table 3-4. Byte Mode (TBIE = low) Receiver Outputs

Clock Edge	RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_3	RECV_*x*_2	RECV_*x*_1	RECV_*x*_0
Rising	E_0	K_0	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Falling	E_1	K_1	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4

NOTE

Do not use Non-Aligned mode in Byte mode. Non-aligned mode is only valid if TBIE is high.

3.3.6.2 Ten-Bit Interface

Received data is ten-bits of pre-coded data when in the Ten-Bit Interface, TBI, mode. The internal 8B/10B decoder is not used and it is assumed that decoding is done externally. Ten-Bit Interface mode is enabled by setting TBIE high.

Table 3-5, shows how data and status will appear on the receiver interface when in 10-bit mode.

Table 3-5. 10 Bit Mode (TBIE = high) Receiver Outputs

Clock Edge	RECV_*x*_ERR	RECV_*x*_K	RECV_*x*_3	RECV_*x*_2	RECV_*x*_1	RECV_*x*_0
Rising	E_0	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Falling	E_1	Data Bit 9 (MSB)	Data Bit 8	Data Bit 7	Data Bit 6	Data Bit 5

3.3.6.3 Receiver Interface Error Codes

The receiver's status and data error conditions are coded on the RECV_*x*_ERR and RECV_*x*_K signals (see Table 3-4 and Table 3-5).

When in Byte mode (TBIE is low) E_0, E_1, K_0, and K_1 indicate the receiver operating status. Table 3-6 describes the encoding and meaning of the status and error conditions for Byte mode.

Table 3-6. Receiver Interface Error Codes (Byte Interface, TBIE = low)

E_0	E_1	K_0	K_1	Priority	Description
Low	Low	Low	Don't care	8	Normal operation, valid data character received.
Low	Low	High	Low	7	Normal operation, valid control character received.
Low	Low	High	High	6	Normal operation, valid Idle (K28.5) character received.
Low	High	Low	Low	4	Code Error: The 8B/10B decoder detected an illegal character.
Low	High	Low	High	5	Disparity Error: The 8B/10B decoder detected a disparity error.
Low	High	High	Low	3	Underrun: The receiver interface synchronization logic detected an underrun condition. Data has been repeated.
Low	High	High	High	3	Overrun: The receiver interface synchronization logic detected an overrun condition. Data has been dropped.
High	Low	Don't care	Don't care	1	Not Byte Sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	Don't care	Don't care	2	Not Word Sync: The receiver is byte synchronized but has not achieved or has lost word synchronization and is searching for synchronization.

When in 10-bit mode (TBIE is high) E_0, and E_1 indicate the receiver operating status. Table 3-7describes the encoding and meaning of the status and error conditions for TBI mode.

Table 3-7. Receiver Interface Error Codes (Ten-bit Interface, TBIE = high)

E_0	E_1	Priority	Description
Low	Low	4	Normal operation, non-Idle character received.
Low	High	3	Normal operation, Idle (K28.5) character received.
High	Low	1	Overrun/Underrun: The receiver interface synchronization logic detected and overrun/underrun condition. Data may be dropped or repeated.
High	High	2	Not Byte/Word Sync: The receiver is in start-up or has lost byte or word alignment and is searching for alignment.

The Priority column in the tables show the error that is reported if multiple errors occur at the same time. The lower the Priority numbered errors are reported first.

3.3.7 Receiver Interface Clock Timing Modes

The receiver interface is double data rate, source synchronous. Each of the receiver's six output signals are timed relative to the rising and falling edges of the receiver interface clock output, RECV_*x*_CLK. The receiver interface clock frequency may be selected between its own recovered clock frequency, receiver A's recovered clock frequency, or the frequency of the reference clock input REF_CLK.

The recovered clock enable signal, RCCE, determines if the receiver interface is timed to the recovered clock or to the local reference clock. Asserting RCCE enables timing relative to the recovered clock, and set low enables timing relative to the reference clock. When RCCE is asserted high, then the signal RECV_REF_A is used to select the recovered clock to be used. If RECV_REF_A is asserted then Channel A's recovered clock is used for all four channels. If it is low then each channel uses its own recovered clock.

The receiver interface clock signals, RECV_*x*_CLK, will always be present when the PLL is in lock. This is true even if there is no signal present on the serial inputs or if the receiver has not achieved alignment or byte sync. The frequency of the receiver clock will be the local reference clock. The clock signals however, are not present during power up or when the MC92602 is in reset mode and the PLL is not locked.

3.3.7.1 Recovered Clock Timing Mode

With RCCE asserted, the recovered clock signal, RECV_*x*_CLK, is generated by the receiver and, on average, runs at the reference clock frequency of the transmitter at the other end of the link. The recovered clock is not generated by a clock recovery PLL, but is generated by the receiver bit-accumulation and byte-alignment logic.

In order to track a transmitter frequency that is offset from the receiver's reference clock frequency, the duty cycle and period of the recovered clock is modulated. The MC92602 is designed to tolerate up to a 250 ppm of frequency offset between transmitter and receiver.

For example: If the transmitter is sending data at a rate faster than the receiver, then a shortened cycle is generated as needed to track the incoming data rate. Alternately, if the transmitter is running slower than the receiver, then a long cycle is generated.

The recovered clock duty cycle may be reduced or increased by 2.5% in order to match the transmitter frequency. For example, if the reference clock frequency is 125MHz, this means that the minimum recovered clock cycle time is 7.8ns and the maximum recovered clock cycle is 8.2ns.

NOTE

Devices that interface to a MC92602 that is run in recovered clock mode must be able to tolerate this modulated clock.

All receiver channel outputs are source synchronous with their respective RECV_*x*_CLK outputs. If the receivers are being operated in word synchronization mode (WSE = high), the data for all four receivers are timed relative to link A's recovered clock RECV_A_CLK. In word synchronization all four clocks are derived from channel A and may be used if necessary.

When operating in the recovered clock timing mode, the addition or deletion of Idles is inappropriate.

NOTE

If RCCE is asserted (recovered clock timing mode), the add/delete idle enable (ADIE) signal must be low.

3.3.7.2 Reference Clock Timing Mode

Data is timed relative to the local reference clock frequency when RCCE is low. Synchronization between the recovered clock and the reference clock is handled by the receiver interface. Frequency offset between the transmitter's reference clock and the receiver's reference clock causes overrun/underrun situations. Overrun occurs when the transmitter is running faster than the receiver. Underrun occurs when the transmitter is running slower than the receiver.

In an overrun situation, data must be dropped in order to maintain synchronization between the clock domains. If the control signal, add drop idle enable, ADIE, is asserted high, the receiver interface searches for a pair of idle bytes to drop when overrun is imminent. Two idle bytes are dropped to assure that running disparity is not affected. If sufficient idle patterns are not available to drop, receiver overrun may occur. When overrun occurs, the "Overrun" error is reported as described in Section 3.3.6.3, for one byte clock period and one character of data is dropped. An overrun error is also reported if ADI mode is disabled and overrun occurs, even if Idles are available to drop.

NOTE

The compatibility mode control signal, COMPAT, set high, instructs the receivers to follow a different set of rules for the addition and deletion of characters that are non-intrusive to packet data streams, but still enable the device to maintain synchronization between the clock domains. See Section 5.4 for more information.

A sufficient number of Idles must be transmitted to guard against overrun. The frequency of Idles can be computed based upon the maximum frequency offset between transmitter and receiver in the system. The number of bytes (characters) that can be transmitted between Idles is:

$(2*10^6 / N) - 1$ bytes

where: N is the frequency offset in ppm.

In an underrun situation, data must be added in order to maintain synchronization between the clock domains. If ADIE is high the receiver interface adds a pair of Idle bytes when underrun is imminent. **The pair of Idles will be inserted prior to the next pair of Idles in the data stream.** This allows the user to establish “packets” of data that do not contain Idles and the MC92602 will NOT insert Idles in the middle of these “packets”. The Idle frequency to prevent underruns is identical to the frequency to prevent overruns, so the same conditions apply. If ADIE is disabled and an underrun occurs, the “Underrun” error is reported as described in Section 3.3.6.3 for one byte clock period.

The proper phase of the REF_CLK will be provided on RECV_n_CLK.

NOTE

When operating in “Word” mode all configured channels must add/delete Idles simultaneously. Therefore Idles must appear in the data stream for all channels simultaneously, so that Idles may be inserted (adjacent to existing Idles) or deleted.

3.3.8 Half-Speed Mode

Half Speed mode, Enabled when HSE is asserted high, operates the receiver in its lower speed range. In half speed mode, the link speed is 500 Mbps (625 Mbaud.) The receiver interface operates at half speed as well, in pace with received data.

3.3.9 Repeater Mode

Repeater mode is not recommended for application use. It is used for factory engineering and manufacturing test purposes only. The repeater enable signal, REPE, should be configured low during normal operation.

Chapter 4
Rate Adaption of Packet Data Streams

This chapter describes how the MC92602 performs rate adaption in applications where the device is used to transmit and receive PCS, PMA, type 1000BASE-X packet streams. When the MC92602 is being operated in reference clock mode, as described in Section 3.3.7, rate adaption is performed to account for frequency offset between the transmitter and receiver. In backplane applications, rate adaption is accommodated by adding K28.5 Idle code groups (characters) to, or deleting K28.5 Idle code groups from, the data stream to match the incoming data rate to the receiver data rate as defined by its reference clock frequency. This indiscriminate addition or deletion of K28.5 Idle characters from an 802.3 packet stream would interfere with proper system operation.

NOTE

Rate adaption is necessary only if the MC92602 is being operated in the reference clock mode (RCCE = low).

The MC92602 compatibility mode, COMPAT, allows for rate adaption using methods compatible with 802.3 packet streams and does not interfere with proper system operation. The following are the features of compatibility mode:

- Context sensitive rate adaption during receipt of configuration, idle and data code groups.
- Tolerates up to +/- 100 ppm frequency offset.
- Supports *Jumbo* frame lengths of up to 16k bytes.
- Supports frame bursting.
- Internal or external 8B/10B encoding/decoding may be used.
- Compatible with specification of Media Access Control function.
- Compatible with 36 specification of the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer function.
- Compatible with specification of the Auto-Negotiation function.

The MC92602's compatibility mode is enabled by asserting the control signal, COMPAT, high.

4.1 Rate Adaption Method

The MC92602 utilizes a FIFO in its receiver to act as an *elastic buffer* for the receive data interface. The elastic buffer allows for proper operation of the interface in the presence of jitter and frequency offset. However, frequency offset will eventually lead to elastic buffer overrun or underrun. In order to prevent underrun and overrun, one or more code groups must be added to or deleted from the packet stream.

The MC92602 must determine the proper type of code groups to add or delete and do it at an appropriate time to ensure compatibility with packet data streams. The code group type and timing is determined by the current context of the packet stream. There are three contexts considered: configuration, idle and data transmission.

4.1.1 Configuration Context

The configuration context is when the transceivers are transmitting configuration ordered sets typically in support of auto-negotiation. A configuration ordered set consists of alternating /C1/ and /C2/ code group sets as shown below:

/C1/: /K28.5/D21.5/Dxx.x/Dxx.x

/C2/: /K28.5/D2.2/Dxx.x/Dxx.x

where /Dxx.x/Dxx.x/ represent the 16-bit contents of the configuration register. During auto-negotiation only alternating /C1/ and /C2/ code group sets are expected and the duration of the auto-negotiation sequence is not bounded. Therefore, rate adaption is accomplished through the addition and deletion of /C1/ and /C2/ code group sets.

The MC92602, upon detection of an imminent overflow, searches for and deletes two /C1/C2/ code group sets, removing a total of 16 code groups (characters) from the packet stream. The auto-negotiation function is tolerant of missing two complete sets because of its handshaking protocol. Two complete /C1/C2/ code groups sets must be deleted, because, for a constant configuration register value, a single /C1/C2/ code group set toggles running disparity. Removing two /C1/C2/ code group sets maintains proper running disparity.

Upon detection of an imminent underflow, the MC92602 searches for two adjacent /C1/C2/ code group sets with a constant configuration register value and inserts a copy of them into the packet stream, adding a total of 16 code groups. The auto-negotiation function is tolerant of additional, valid, sets because of its handshaking protocol. In order to maintain proper running disparity as described above, two complete /C1/C2/ code group sets must be added to the packet stream.

4.1.2 Idle Context

The idle context is when the transceivers are transmitting idle ordered sets when the link is idle or during inter-packet gaps (IPG). An idle ordered set consists of two types of code group pairs:

/I1/: /K28.5/D5.6

/I2/: /K28.5/D16.2

where /I1/ is a *correcting* idle and /I2/ is a *preserving* idle. However, there is a more general definition of an idle ordered set as any pair of code groups where the first code group is a /K28.5/ followed by a /Dxx.x/ code group where /Dxx.x/ is not /D21.5/ or /D2.2/. The rules for the insertion of idle ordered sets into a packet stream dictate that the resulting running disparity be negative after the idle code group is inserted. A correcting idle, /I1/, toggles positive running disparity to negative; a preserving idle, /I2/, maintains negative running disparity. These rules are in place specifically to allow the addition or deletion of preserving idle ordered sets by repeaters to accommodate retiming. Therefore, rate adaption in the idle context is accomplished through the addition and deletion of preserving idle ordered sets.

The MC92602, upon detection of an imminent overflow, searches for and deletes an /I2/ ordered set, removing a total of two code groups from the packet stream. The packet stream tolerates deletion of /I2/ as described above. Deleting /I2/ raises concerns about IPG shrinkage. The IEEE Std 802.3 specification [5], clause 4.4.2.4, requires the IPG on transmit to be at least 12 code groups in duration, including the end of packet delimiter (EPD). The received IPG is only required to be at least 8 code groups in duration, leaving 4 code groups available to remove per IPG.

NOTE

The MC92602 does not verify that the IPG meets minimum length requirements after removal of the /I2/ code groups. It assumes that the IPG is at least 12 code groups in length when received.

Upon detection of an imminent underflow, the MC92602 searches for an /I2/ ordered set and inserts an /I2/ adjacent to it into the packet stream, adding a total of 2 code groups. The packet stream tolerates additional /I2/ ordered sets because maximum IPG length is not limited.

Special consideration is given to IPG in the data context to accommodate Jumbo frames and frame bursting. These are described in the next section.

4.1.3 Data Context

The data context is when the transceivers are transmitting MAC frames encapsulated into code group packets. The code groups in the packet can not be disturbed, therefore, rate

adaption is accomplished in the IPG as described above. There are two special cases that must be considered in the data context: Jumbo frames and frame busting.

Jumbo frames are not supported in the real standard, but are rather a de facto standard. Jumbo frames violate the untagged maximum frame size of 1518 code groups and increases the size to 16k code groups. Given a maximum total frequency offset of 200 ppm and the size of the MC92602's elastic buffers, a Jumbo frame could lead to a surplus or deficit of 3.3 code groups for which rate adaption must account.

The MC92602, upon detection of an imminent overflow, searches for and deletes an /I2/ ordered set, removing a total of two code groups from the IPG. If a Jumbo frame is detected by evidence of a large surplus, two /I2/ ordered sets are deleted, removing a total of four code groups.

Similarly, upon detection of an imminent underflow, the MC92602 searches for a /I2/ ordered set and inserts an /I2/ adjacent to it into the IPG, adding a total of two code groups. If a Jumbo frame is detected by evidence of a large deficit, two /I2/ ordered sets are inserted, adding a total of four code groups.

The size of the elastic buffers are increased by 8 to accommodate accumulation of four code groups to guard against later deficit, and to allow for the accumulation of an additional four surplus code groups.

In half-duplex mode of operation as defined by the standard, frame bursting is allowed. Frame bursting is an artifact of the CSMA/CD media access mechanism where idle ordered sets in the IPG are used to signal availability of the medium. Frame bursting allows the transmitter to retain ownership of the medium by inserting carrier extend, /R/, ordered sets in the IPG in place of idle ordered sets. A frame burst can be as long as 65k bits (8k code groups). An idle-based IPG must exist between frame bursts. Frame bursts are shorter than Jumbo frames, therefore, frame bursting is supported using the same mechanism as Jumbo frames just described.

4.2 Error Handling

The receiver interface error reporting mechanisms as described in Section 3.3.6.3 are used in compatibility mode with one exception; overrun/underrun errors are processed differently.

Overrun may occur when an appropriate code group to remove can not be identified. In this situation, one data code group is removed from the packet stream. The received packet stream continues normally thereafter. The code group immediately following the removed code group is reported as an overrun error as described in Section 3.3.6.3. The MAC sublayer should detect the missing code group as a CRC error.

Underrun may occur when an appropriate code group to insert can not be identified. In this situation, one data code group is repeated in the packet stream. The received packet stream

continues normally thereafter. The repeated code group is reported as an underrun error as described in Section 3.3.6.3. The MAC sublayer should detect the repeated code group as a CRC error.

4.3 Special Considerations

When the compatibility mode is enabled by setting COMPAT high, special rules for rate adaption are followed as described above. Additionally, the receiver's elastic buffers operate differently to account for Jumbo frames. In order to ensure against starvation of the elastic buffer in the presence of Jumbo frames, the elastic buffers are allowed to accumulate four additional code groups, leading to longer receiver latency. Receiver latency increases by four code groups, 40 bit-times, when in the compatibility mode.

Word synchronization, as described in Section 3.3.4, is not supported in the compatibility mode. Each channel is considered to be an independent packet stream.

If the MC92602 is being operated in recovered clock mode, see Section 3.3.7.1, then rate adaption is not performed by the device and the data stream is transferred unmodified. The compatibility mode would have no effect on device operation and is not required.

The compatibility mode should not be used in backplane applications that are not utilizing standard protocol.

Chapter 5
System Design Considerations

This chapter describes general system considerations for the MC92602 Quad DDR, including device-startup, initialization and the proper use of the configuration and control signals, the reference clock configuration, and general recommendations.

5.1 Reference Clock Configuration

The clock inputs REF_CLK_P and REF_CLK_N are the differential reference clock inputs for the MC92602. The frequency of the clock signal applied to these inputs along with the settings on the configuration inputs determine the speed at which the serial links operate. Also, the legal ranges of reference clock frequencies vary depending on the configuration selected. Table 5-1 shows the ranges allowed for each configuration.

Table 5-1. Legal Reference Clock Frequency Ranges

HSE	Reference Frequency Min (MHz)	Reference Frequency Max (MHz)	Link Transfer Rate (Gigabaud)
Low	95.00	135.0	0.95 - 1.35
High	47.50	67.50	0.475 - 0.675

NOTE

The device must be reset by setting $\overline{\text{RESET}}$ low, if the reference clock configuration, HSE, is changed after power-up.

The clock inputs REF_CLK_P and REF_CLK_N are normally driven with a differential clock source. However, the reference clock may also be driven with a single-ended source. In this situation, the REF_CLK_P signal is driven by the single-ended clock source and the REF_CLK_N signal is held at the HSTL reference voltage as defined in Section 5.8. The REF_CLK_N signal may be connected to its own reference voltage circuit or may share the reference voltage circuit used for the HSTL_VREF signal, if board layout allows.

5.2 Startup

The MC92602 begins a startup sequence upon application of the reference clock (REF_CLK_N/P input) to the device. This is considered a *cold* startup. The cold startup sequence is as follows:

1. PLL Startup
2. Receiver Initialization and Byte Alignment
3. Word Alignment (if enabled)
4. Run

The expected duration of each step in the startup sequence is shown in Table 5-2. A cold startup can be initiated at any time by setting $\overline{\text{RESET}}$ low. It is recommended that $\overline{\text{RESET}}$ be low at initial startup, however, it is not strictly required.

Table 5-2. Startup Sequence Step Duration

Startup Step	Typical Duration (in bit times)	Note
PLL Startup	10,2400 + 25 µs	
Receiver Initialization	50	**WSE** = low
	160	**WSE** = high
Word Alignment	50	**WSE** = low
	160	**WSE** = high

5.3 Standby Mode

Standby mode puts the MC92602 into a low power, inactive state. When STNDBY is asserted high, the device will force all transmitter link outputs to their disabled state as defined in Section 2.3.3, and will disable all internal clocking. An important feature of standby mode is that the internal PLL is not disabled. It remains operating and locked to the reference clock. This greatly reduces the time needed to recover from standby mode to run mode, as only the receiver initialization and word alignment startup steps are required.

5.4 Configuration and Control Signals

The MC92602 has many configuration and control signals that are asynchronous to all inputs clocks. Most of the signals affect the internal configuration state and must be set at power-up. If their state is changed after power-up, some require that the chip be reset by setting $\overline{\text{RESET}}$ low and then releasing high. While other configuration signals are meant to be changed during normal operation and do not require chip reset. However, these signals may still affect device operation. Table 5-3 lists all of the MC92602's asynchronous

configuration and control signals and describes the effect of changing their state after power up.

Table 5-3. Asynchronous Configuration and Control Signals

Signal Name	Description	Effect of Changed State
XCVR_*x*_DISABLE	Transceiver Disable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
DROP_SYNC	Drop Synchronization	Receiver must re-establish byte and word synchronization.
XMIT_REF_A	Transmitter Reference Clock A Select	Device must be reset.
RECV_REF_A	Receiver Reference Clock A Select	Device must be reset.
TBIE	Ten-Bit Interface Enable	Device must be reset.
HSE	Half-Speed Enable	Device must be reset.
BSYNC	Byte Synchronization Mode	Device must be reset.
ADIE	Add/Drop Idle Enable	Device must be reset.
COMPAT	Compatibility Mode	Device must be reset.
REPE	Repeater Mode Enable	Must be low and remain low during normal operation.
RCCE	Recovered Clock Enable	Device must be reset.
WSE	Word Synchronization Enable	Device must be reset.
TST_0, TST_1	Test Mode Identifiers	Must be low and remain low during normal operation.
LBE	Loop Back Enable	Receiver must acquire new bit phase alignment; byte and word synchronization must be re-established.
LBOE	Loop Back Output Enable	Enable/disable transmit links during testing (LBOE = high), no recovery action necessary.
STNDBY	Puts PLL in Standby Mode	Receiver must re-establish byte and word synchronization.
$\overline{\text{RESET}}$	System Reset Bar	Device is reset.

5.5 Power Supply Requirements

The recommended board for the MC92602 has a minimum of two solid planes of one ounce copper. One plane is to be used as a ground plane and the second plane is to be used for the 1.8V supply. It is recommended that the board has its own 1.8V and 1.5V regulators with less than 50mV ripple.

5.6 Phase Locked Loop (PLL) Power Supply Filtering

An analog power supply is required. The PLLAVDD signal provides power for the analog portions of the PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 5-1. For maximum effectiveness, the filter circuit is placed as close as possible to the PLLAVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the PLLAGND ball. The 0.01µF capacitor is closest to the ball, followed by the 1 µF capacitor, and finally the 1 Ω resistor to Vdd on the 1.8V power plane. The capacitors are connected from PLLAGND to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

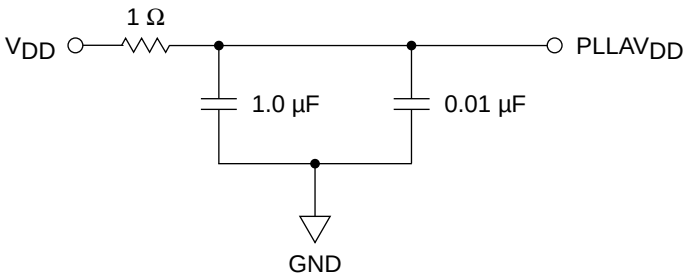


Figure 5-1. PLL Power Supply Filter Circuits

5.7 Power Supply Decoupling Recommendations

The MC92602 requires a clean, tightly regulated source of power to ensure low jitter on transmit, and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used, to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

First, the board should have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 1.8v (Vdd and XVdd) balls of the device. The board should also have about 10 x 10nF SMT ceramic chip capacitors as close as possible to the 1.5v (V_{DDQ}) balls of the device. Where the board has blind vias, these capacitors should be placed directly below the MC92602 supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the MC92602, as close to the supply and ground connections as possible.

Second, there should be a 1uF ceramic chip capacitor on each side of the MC92602 device. This should be done for both the 1.8v supply and the 1.5v supply.

Third, between the MC92602 device and the voltage regulator, there should be a 10uF, low equivalent series resistance (ESR) SMT tantalum chip capacitor, and a 100uF, low ESR

SMT tantalum chip capacitor. This should be done for both the 1.8v supply and the 1.5v supply.

5.8 HSTL Reference Voltage Recommendation

The MC92602 uses HSTL Class-I inputs and outputs for all of its high-frequency parallel interface signals. The HSTL Class-I interfaces are compatible with the EIA/JEDEC standard EIA/JESD8-6 [3].

HSTL Class-I inputs define their switching thresholds about a reference voltage supplied at an input of the device. The reference voltage is applied to the HSTL_VREF input of the MC92602. The reference voltage, referred to as V_{REF} in Table 7-3, must fall within the minimum and maximum voltages as specified and must have no more than 2 percent peak-to-peak AC noise. In practice, V_{REF} for the HSTL inputs should track the variations in the DC value of V_{DDQ} of the sending device for best noise margin. The value of V_{REF} is to be selected by the user to provide optimum noise margin. Figure 5-2 shows a recommended circuit topology to generate V_{REF} with recommended ceramic chip filter capacitor.

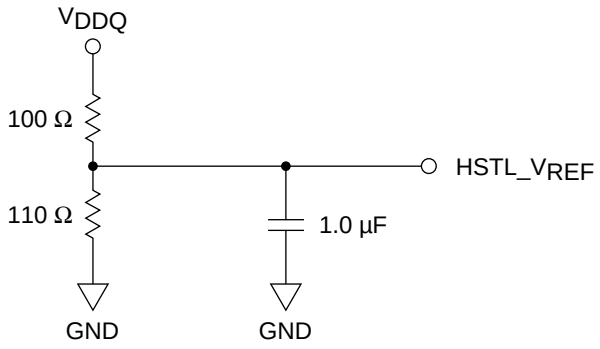


Figure 5-2. HSTL Class-I V_{REF} Circuit

Chapter 6
Test Features

The MC92602, supports several test modes for Built In System Test, BIST, and production testing. The MC92602 also has an IEEE Std. 1149.1 [4] compliant Test Access Port and Boundary Scan Architecture implementations. This chapter covers the JTAG implementation and the system accessible test modes.

6.1 IEEE Std. 1149.1 Implementation

This section describes the IEEE Std. 1149.1 compliant Test Access Port and Boundary Scan Architecture implementation in the MC92602.

6.1.1 Test Access Port (TAP) Interface Signals

Table 6-1 lists the interface signals for the TAP.

Table 6-1. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test Clock	Test logic clock.	Input	-
TMS	Test Mode Select	TAP mode control input.	Input	-
TDI	Test Data In	Serial test instruction/data input.	Input	-
$\overline{\text{TRST}}$	Test Reset Bar	Asynchronous test controller reset.	Input	Low
TDO	Test Data Out	Serial test instruction/data output.	Output	-

NOTE

There are 10K Ohm pull-ups on the TMS, TDI and $\overline{\text{TRST}}$. If $\overline{\text{TRST}}$ is not held low during power-up or does not receive an active low reset after power-up, the test logic may assume an indeterminate state disabling some of the normal transceiver functions. It is recommended that $\overline{\text{TRST}}$ be terminated in one of the following ways:

1. $\overline{\text{TRST}}$ be driven by a TAP controller that provides a reset after power-up.

2. Connect $\overline{\text{TRST}}$ to $\overline{\text{RESET}}$.

3. Terminate $\overline{\text{TRST}}$ with a 1K Ohm resistor (or hard wire) to ground.

6.1.2 Instruction Register

Bit Position	3	2	1	0
Field	IR			
Capture-IR Value	0	0	0	1

Figure 6-1. Instruction Register

6.1.3 Instructions

Table 6-2 lists the public instructions provided in the implementation and their instruction codes.

Table 6-2. Tap Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	1111	Bypass Register
CLAMP	1100	Bypass Register
EXTEST	0000	Boundary Scan Register
HIGHZ	1001	Bypass Register
IDCODE	0001	ID Register
SAMPLE	0010	Boundary Scan Register

Table 6-3 lists the Private instruction codes that if executed could be hazardous to device operation. The user should not execute these instructions.

Table 6-3. Tap Controller Private Instruction Codes

Instruction Code	Instruction Code
0011	1000
0100	1010
0101	1011
0110	1110
0111	-

6.1.4 Boundary-Scan Register

A full description of the boundary scan register may be found in the BSDL file provided by Motorola upon request.

6.1.5 Device Identification Register (0x0281601D)

Bit Position	31			28	27													12	11									0
Field	VERSION				PART NUMBER														MANUFACTURER ID									
Value	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-2. Device Identification Register

6.1.6 Performance

The performance and electrical properties of the tap controller, boundary scan, and JTAG inputs and outputs are described in Chapter 7, “Electrical Specifications and Characteristics.

6.2 System Accessible Test Modes

System accessible test modes are selected through the TST_0, TST_1 and LBE signals. Table 6-4 shows test mode state selection.

Table 6-4. Test Mode State Selection

TST_1	TST_0	LBE	Description
Low	Low	Low	Normal operation. No test mode enabled.
Low	Low	High	Loop back system test mode.
Low	High	Low	BIST sequence system test mode with IDLEs inserted for rate adaption.
Low	High	High	Loop back BIST sequence system test mode.
High	Low	Low	BIST sequence system test mode without IDLEs inserted for rate adaption.
High	Low	High	Reserved.
High	High	Low	Reserved.
High	High	High	Reserved.

6.2.1 Loop Back System Test

The MC92602 can be configured in loop back mode where the transmitted data is looped back to its receiver independent of the receiver’s link inputs. This is enabled by setting Loop Back Enable, LBE, high. The characters transmitted are controlled by the normal transmitter controls. If the transceiver is working properly, the data/control characters

transmitted are received by the receiver. This allows system logic to use various data sequences to test the operation of the transceiver.

The loop-back signals are electrically isolated from the XLINK_*x*_P or XLINK_*x*_N output signals. Therefore, if the outputs are shorted, or otherwise restricted, the loop-back signals still operate normally. When in loop-back mode, the loop-back output enable, LBOE, signal controls the action of the link output signals. When LBOE is low, the XLINK_*x*_P or XLINK_*x*_N output signals are disabled and are high-impedance. When LBOE is high, the link output signals continue to operate normally.

The receiver's link input signals, RLINK_*x*_P and RLINK_*x*_N, are electrically isolated during loop back mode, such that their state does not affect the loop back path.

6.2.2 BIST Sequence System Test Mode

The MC92602's transmitter has an integrated, 23rd order, Pseudo-Noise (PN) pattern generator. Stimulus from this generator may be used for system testing. The receiver, has a 23rd order signature analyzer that is synchronized to the incoming PN stream and may be used to count character mismatch errors relative to the internal PN reference pattern.

This implementation of the 23-bit PN generator and analyzer uses the polynomial:

$$f = 1 + x^5 + x^{23}$$

The total mismatch error count is reset to zero when BIST mode is entered. The count is updated continuously while in BIST mode. The value of the count is presented on the receiver interface signals: RECV_*x*_3 through RECV_*x*_0 (as interpreted and shown in Table 3-4), making up the eight-bit error count, ordered bits 7 through 0, respectively. The value of the count is *sticky* in that the count will not wrap to zero upon overflow, but rather, stays at the maximum count value (11111111).

The RECV_*x*_ERR, RECV_*x*_K (as interpreted and shown in Table 6-5), have special meaning during this test mode. They report the status of the receiver and PN analysis logic. Table 6-5 describes the BIST error codes and their meaning. E_0 and K_0 are the values on RECV_*x*_ERR and RECV_*x*_K, respectively, on the rising edge of the recovered clock. E_1 and K_1 are the values of RECV_*x*_ERR and RECV_*x*_K, respectively, on the falling edge of the recovered clock

Table 6-5. BIST Error Codes

E_0	E_1	K_0	K_1	Description
Low	Low	Don't care	Don't care	BIST running, no PN mismatch this character.
Low	High	Low	Low	BIST running, PN mismatch error this character.
Low	High	Low	High	Receiver byte/word synchronized, PN analyzer is not locked.

Table 6-5. BIST Error Codes

High	Low	Don't care	Don't care	Not Byte Sync: The receiver is in start-up or has lost byte alignment and is searching for alignment.
High	High	Don't care	Don't care	Not Word Sync: The receiver is byte synchronized but has not achieved or has lost word alignment and is searching for alignment.

The BIST sequence makes use of the 8B/10B encoder/decoder. Therefore, this test mode overrides the setting on TBIE signal and forces Byte Interface mode. Additionally, the BIST sequence requires that a normal byte alignment mode be used. The setting of BSYNC is overridden, forcing the device into the Byte Aligned mode (forces BSYNC high internally).

BIST is run at the speed indicated by the frequency of the reference clock and by the speed range selected by half-speed mode (HSE). The settings of WSE, RCCE, RECV_REF_A are not altered and BIST will follow their setting.

In order to properly use this test mode, the system must provide the proper stimulus in a special sequence. The sequence is as follows:

Step 1: Enter test mode by setting the test mode inputs as described in Table 6-4.

Step 2: Transmit 4096 IDLEs (K28.5 characters).

Step 3: Transmit to the receiver an 8B/10B encoded PN sequence as described above.

The transmitter will automatically go through steps 2 and 3 upon entering this test mode. When testing is complete, the device will need to be reset before normal operation can resume.

There are two test configurations for BIST as defined in Table 6-4. One operates as just described above. The second mode, (TST_1 = low, TST_0 = high, LBE = low), inserts 2 IDLES every 2048 characters during step 3. The signature analyzers ignore the Idle character.

NOTE

The receiver signature analyzers assume all four channels are being exercised. If BIST testing is being performed between devices, or by means of external loop back on selected channels, the unused channel receivers must be disabled or the analyzers will not go into the PN Sync state. That is, receivers not having an PN stimulus must have XCVR_*x*_DISABLE asserted.

6.3 Loop-Back BIST Sequence System Test Mode

The test mode is the combination of the Loop-Back and BIST Sequence System Test Modes. The device operates as described in Section 6.2.1 and Section 6.2.2. However, the need to go through the startup sequence is eliminated because the transmitter automatically goes through the proper sequence.

Chapter 7
Electrical Specifications and Characteristics

This chapter explains the electrical specifications and characteristics of the MC92602 device. This chapter consists of the following sections:

- Section 7.1, “General Characteristics,”
- Section 7.2, “DC Electrical Specifications,” and
- Section 7.3, “AC Electrical Characteristics.”

7.1 General Characteristics

This section presents the general technical parameters, the maximum and recommended operating conditions for the MC92602.

7.1.1 General Parameters

The following provides a summary of the general parameters of the MC92602:

- Technology—0.25µ lithography, HiP4 CMOS, 5 layer metal
- Package—196 MAPBGA, 15x15 mm Body Size, 1mm Ball Pitch
- Core Power Supply—1.8V $\pm$ 0.15V dc
- HSTL I/O Power Supply—1.5V $\pm$ 0.1 V dc *or* 1.8V $\pm$ 0.15V dc
- Link I/O Power Supply—1.8V $\pm$ 0.15

7.1.2 Absolute Maximum Rating

Table 7-1, in this section, describes the MC92602's, absolute maximum DC electrical ratings.

Table 7-1. Absolute Maximum Ratings

Characteristics [1]	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	-0.3	2.2	V
PLL Supply Voltage	AV_{DD}	-0.3	2.2	V
HSTL I/O Supply Voltage	V_{DDQ}	-0.3	2.2	V
Link I/O Supply Voltage	XV_{DD}	-0.3	2.2	V
HSTL Input Voltage	V_{in}	-0.3	V_{DDQ} + 0.3	V
CMOS Input Voltage	V_{in}	-0.3	V_{DD} + 0.3	V
Link Input Voltage	V_{in}	-0.3	XV_{DD} + 0.3	V
Storage Temperature Range	T_{stg}	-55	150	^{o}C
ESD Tolerance	HBM	2,000	-	V
	MM	200	-	V

[1] Functional and tested operating conditions are given in Table 7-2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums are not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

7.1.3 Recommended Operating Conditions

Table 7-2 in this section describes the recommended operating conditions for the MC92602.

Table 7-2. Recommended Operating Conditions

Characteristic [1, 2]	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.65	1.95	V
PLL Supply Voltage	AV_{DD}	1.65	1.95	V
HSTL I/O Supply Voltage (1.5V Operation)	V_{DDQ}	1.40	1.60	V
HSTL I/O Supply Voltage (1.8V Operation)	V_{DDQ}	1.65	1.95	V
Link I/O Supply Voltage	XV_{DD}	1.65	1.95	V
HSTL Input Voltage	V_{in}	0	V_{DDQ}	V
CMOS Input Voltage	V_{in}	0	V_{DD}	V
Link Input Voltage	V_{in}	0	XV_{DD}	V

Table 7-2. Recommended Operating Conditions (continued)

Characteristic [1, 2]	Symbol	Min	Max	Unit
Junction Temperature	T_j	-40	105	^oC
Ambient Temperature [3]	T_a	–	–	^oC

1 These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2 Recommended supply power-up order is V_{DD}, AV_{DD}, V_{DDQ}, XV_{DD}, however, any order is acceptable as long as Maximum Ratings are not exceeded.
3 Operating Ambient Temperature is dependent on proper thermal management to meet operating Junction Temperature

7.2 DC Electrical Specifications

Table 7-3 in this section describes the MC92602 DC electrical characteristics.

Table 7-3. DC Electrical Specifications

Characteristic [1]	Symbol	Min	Max	Unit
Core Supply Current [2]	I_{DD}	—	650	mA
PLL Supply Current [2]	AI_{DD}	—	10	mA
HSTL I/O Supply Current [2]	I_{DDQ}	—	108	mA
Link I/O Supply Current [2]	XI_{DD}	—	47	mA
Total Power Dissipation [3]	P_D	—	—	mW
HSTL Reference Voltage	V_{REF}	0.68	0.9	V
HSTL Input High Voltage (DC)	V_{IH} DC	V_{REF} + 0.1	—	V
HSTL Input Low Voltage (DC)	V_{IL} DC	-	V_{REF} - 0.1	V
HSTL Input High Voltage (AC)	V_{IH} AC	V_{REF} + 0.2	-	V
HSTL Input Low Voltage (AC)	V_{IL} AC	-	V_{REF} - 0.2	V
HSTL Input Leakage Current, $V_{in} = V_{DDQ}$	I_{IH}	-	80	µA
HSTL Input Leakage Current, V_{in} = GND	I_{IL}	-	275	µA
HSTL Output High Voltage	V_{OH}	V_{DDQ} - 0.4	-	V
HSTL Output Low Voltage	V_{OL}	-	0.4	V
HSTL Input Capacitance	C_{in}	-	8	pF
HSTL Output Impedance, Vout = $V_{DDQ}/2$	R_{out}	35	55	Ω
CMOS Input High Voltage	V_{IH}	1.0	-	V
CMOS Input Low Voltage	V_{IL}	-	0.5	V

Table 7-3. DC Electrical Specifications (continued)

Characteristic [1]	Symbol	Min	Max	Unit
CMOS Input Leakage Current, $V_{in} = V_{DDQ}$	I_{IH}	-	10	µA
CMOS Input Leakage Current, V_{in} = GND	I_{IL}	-	10	µA
CMOS Input Capacitance	C_{in}	-	10	pF
Link Common Mode Input Impedance	R_{cm}	2	4	kΩ
Link Differential Input Impedance (MEDIA = low/high)	R_{diff}	85/127.5	130/195	Ω
Link Common Mode Input Level [4]	V_{cm}	0.725	1.225	V
Link Differential Input Amplitude	ΔV_{in}	0.4	3.2	V_{p-p}
Link Input Capacitance	C_{in}	-	3	pF
Link Common Mode Output Level	V_{cm}	0.725	1.075	V
Link Differential Output Amplitude, (100/150Ω diff load, MEDIA = low/high)	ΔV_{out}	1.3	2.2	Vp-p
Link Differential Output Impedance (MEDIA = low/high) typical	R_{out}	100/150 [5]		Ω

1 $V_{DD} = AV_{DD} = XV_{DD} = 1.8 \pm 0.15$ V dc, $V_{DDQ} = 1.5 \pm 0.1$ V dc, GND = 0 V dc, $-40 \le T_j \le 105°C$.

2 Currents maximums at $V_{DD} = AV_{DD} = XV_{DD} = V_{DDQ}$ =1.95 V dc, all links operating at full-speed.

3 Typical P_D (mWatts) = 95.4 + 37.8n + 0.3nf + 6.4f; where n = number of active channels and f = Reference frequency in MHz.

4 Subject to absolute voltage on link input pin remaining in recommended range per Table 7-2.

5 Typical values

7.3 AC Electrical Characteristics

The figures and tables in this section describe the AC electrical characteristics of MC92602. All specifications stated are for T_j = -40°C to 105°C, $V_{DD} = AV_{DD} = XV_{DD}$ = 1.65V to 1.95V, V_{DDQ} = 1.4V to 1.6V

7.3.1 Parallel Port Interface Timing

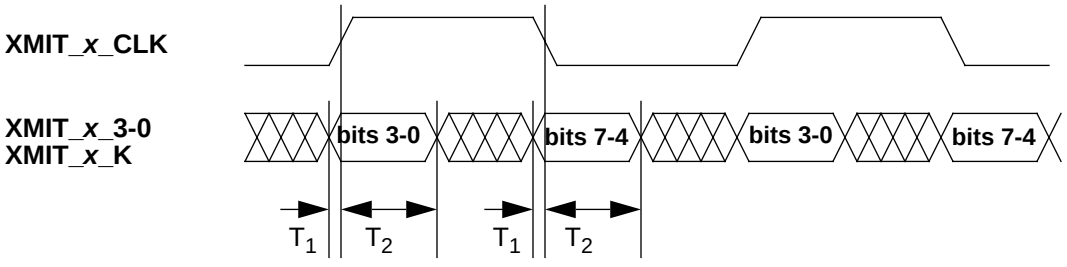


Figure 7-1. Transmitter DDR Interface Timing Diagram

Table 7-4. Transmitter DDR Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1	Setup time to rising/falling edge of XMIT_*x*_CLK	0	-	ns
T_2	Hold time to rising/falling edge of XMIT_*x*_CLK	0.960 [1]	-	ns
		1.3 [2]		ns
Φ_{drift}	Phase drift between XMIT_*x*_CLK and REF_CLK_P	-180	180	degrees

1 Synchronous to channel's transmit interface clock, **XMIT_REF_A**=Low.

2 Synchronous to **XMIT_A_CLK**, **XMIT_REF_A** = High.

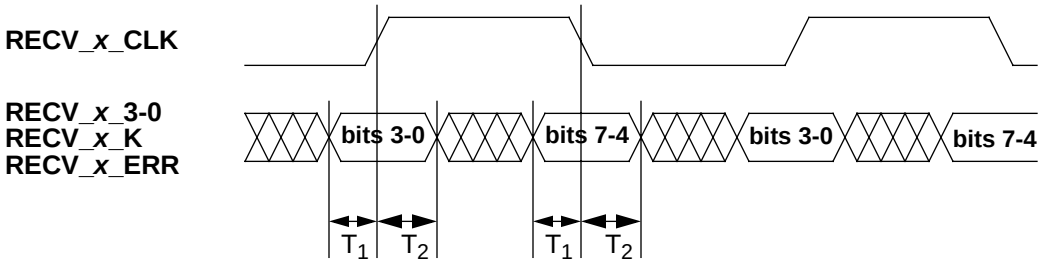


Figure 7-2. Receiver Interface DDR Timing Diagram

Table 7-5. Receiver DDR Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1	Output valid time before rising/falling edge of RECV_*x*_CLK	1.3 [1]	-	ns
		1.3 [2]	-	ns
T_2	Output valid time after rising/falling edge of RECV_*x*_CLK	1.3 [1]	-	ns
		5.3 [2]	-	ns
T_f	Output fall time [3]	-	1.0	ns
T_r	Output rise time [3]	-	1.0	ns

1 Full speed, 125MHz operation (HSE = low).

2 Half-speed, 62.5MHz operation (HSE = high).

3 10pF output load.

7.3.2 Reference Clock Timing

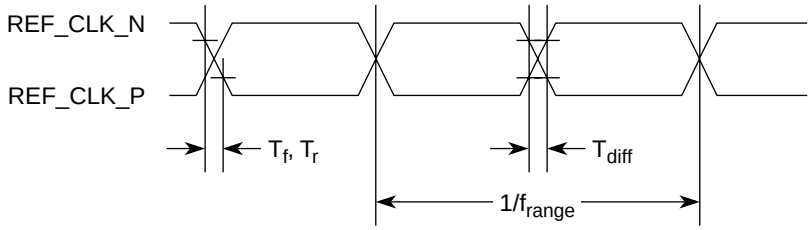


Figure 7-3. Reference Clock Timing Diagram

Table 7-6. Reference Clock Specification

Symbol	Characteristic	Min	Max	Unit
T_r	**REF_CLK_P/N** rise time [1]	-	2.0	ns
T_f	**REF_CLK_P/N** fall time [1]	-	2.0	ns
f_{range}	**REF_CLK_P/N** frequency range [2, 3]	95	135	MHz
f_{range}	**REF_CLK_P/N** frequency range [2, 4]	47.5	67.5	MHz
T_D	**REF_CLK_P/N** duty cycle	45	55	Percent
T_{diff}	**REF_CLK_P** to **REF_CLK_N** differential skew	-	1.0	ns
f_{tol}	**REF_CLK_P/N** frequency tolerance	-200	200	ppm
T_j	**REF_CLK_P/N** input jitter [5]	-	80	ps
T_{lock}	PLL lock time [6]	-	20,480 + 25 µs	bit-times

1 Measured between 10-90 percent points.
2 Measured between 50-50 percent points.
3 Full speed operation (HSE = low).
4 Half speed operation (HSE = high).
5 Total peak-to-peak jitter.
6 Lock time after compliant REF_CLK_P/N signal applied.

7.3.3 Receiver Recovered Clock Timing

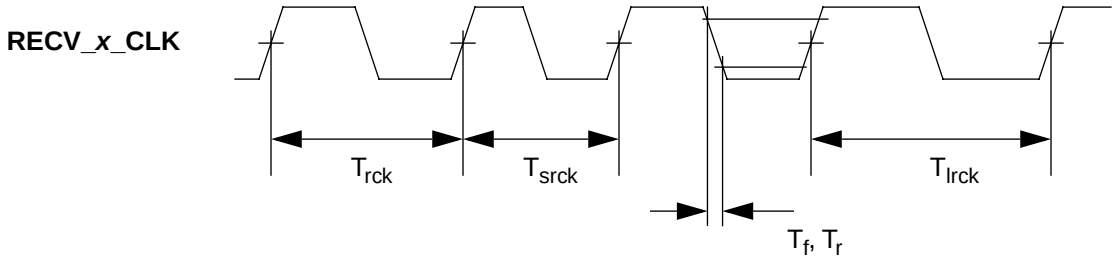


Figure 7-4. Recovered Clock Timing Diagram

Table 7-7. Recovered Clock Specification

Symbol	Characteristic	Min	Max	Unit
T_{rck}	RECV_*x*_CLK period (normal cycle) [1, 2]	8.0 [3]	-	ns
		16.0 [4]	-	ns
T_{srck}	RECV_*x*_CLK period (short cycle) [1, 2]	7.8 [3]		ns
		15.6 [4]		ns
T_{lrck}	RECV_*x*_CLK period (long cycle) [1, 2]	8.2 [3]		ns
		16.4 [4]		ns
T_r	RECV_*x*_CLK rise time [5]	-	1.0	ns
T_f	RECV_*x*_CLK fall time [5]	-	1.0	ns
T_D	RECV_*x*_CLK duty cycle	45	55	%
T_j	RECV_*x*_CLK jitter [6]	-	200 [3]	ps
		-	400 [4]	ps

1 Measured between 50-50 percent points, 125MHz REF_CLK.
2 Includes jitter component.
3 Normal speed
4 Half speed
5 Measured between 10-90 percent points.
6 Total peak-to-peak jitter.

7.3.4 Serial Data Link Timing

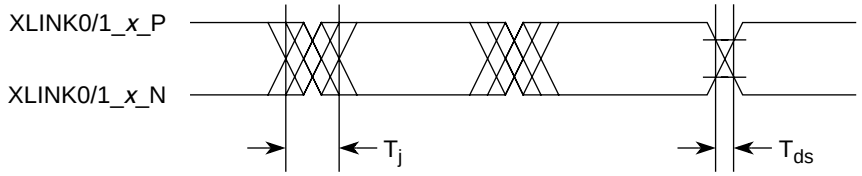


Figure 7-5. Link Differential Output Timing Diagram

Table 7-8. Link Differential Output Specification

Symbol	Characteristic	Min	Max	Unit
T_j	Total jitter [1]	-	0.24	UI
T_{dj}	Deterministic jitter [1]	-	0.12	UI
T_{ds}	Differential skew [1]	-	25	ps
$X_{la\ t}$	Transmit latency [2]	-	67	bit-times

1 Measured between 50-50 percent points.

2 Rising edge REF_CLK_P to bit 0 transmit.

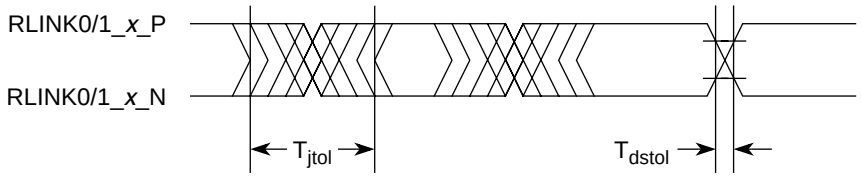


Figure 7-6. Link Differential Input Timing Diagram

Table 7-9. Link Differential Input Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_r	Link input rise time [1]	300		ps
T_f	Link input fall time [1]	300		ps
T_{jtol}	Total jitter tolerance [2, 3]	0.71	-	UI
T_{djtol}	Deterministic jitter tolerance [2, 3]	0.45	-	UI
T_{dstol}	Differential skew tolerance [2, 3]	175	-	ps
R_{lat}	Receive latency [4]	-	190	bit-times
T_{acq}	Receiver phase acquisition time	-	300 [5]	bit-times

1 Measured between 10-90 percent points

2 Measured between 50-50 percent points, 125 MHz REF_CLK, 1.25 Gbaud

3 Per IEEE 802.3z specification

[4] Bit 0 at receiver input to parallel data out

[5] Measured with worst-case eye opening, Idle pattern, and reference PLL locked.

7.3.5 JTAG Test Port Timing

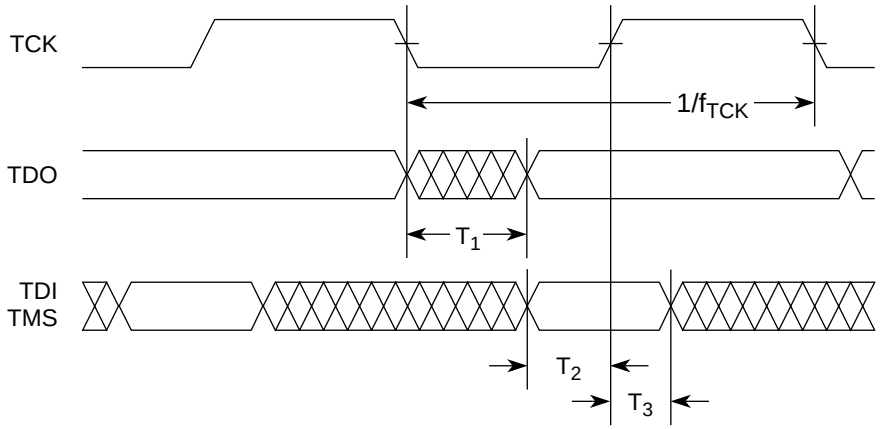


Figure 7-7. JTAG I/O Timing Diagram

Table 7-10. JTAG I/O Timing Specification

Symbol	Characteristic	Min	Max	Unit
T_1	Output propagation time after falling edge of TCK [1]	1.0	8.0	ns
T_2	Setup time to rising edge of TCK	1.0	-	ns
T_3	Hold time to rising edge of TCK	0.5	-	ns
f_{TCK}	TCK frequency	-	20	MHz
T_D	TCK duty cycle	35	65	Percent

[1] 10 pF output load

Chapter 8
Package Description

The following section provides the package parameters and mechanical dimensions of the MC92602 device. The MC92602 is offered in a 196 MAPBGA package. The 196 MAPBGA utilizes an aggressive 1 mm ball pitch and 15 mm body size for application where board space is limited.

8.1 196 MAPBGA Package Parameter Summary

- Package Type—Fine pitch ball grid array
- Package Outline—15 mm x 15 mm
- Package Height—1.60 mm Max
- Number of Balls—196
- Ball Pitch—1 mm
- Ball Diameter—0.45–0.55 mm

8.2 Nomenclature and Dimensions of the 196 MAPBGA Package

Figure 8-1 provides the bottom surface nomenclature and package outline drawing of the 196 MAPBGA package. Figure 8-2 provides the package dimensions. Figure 8-3 provides a graphic of the package pin signal mappings.

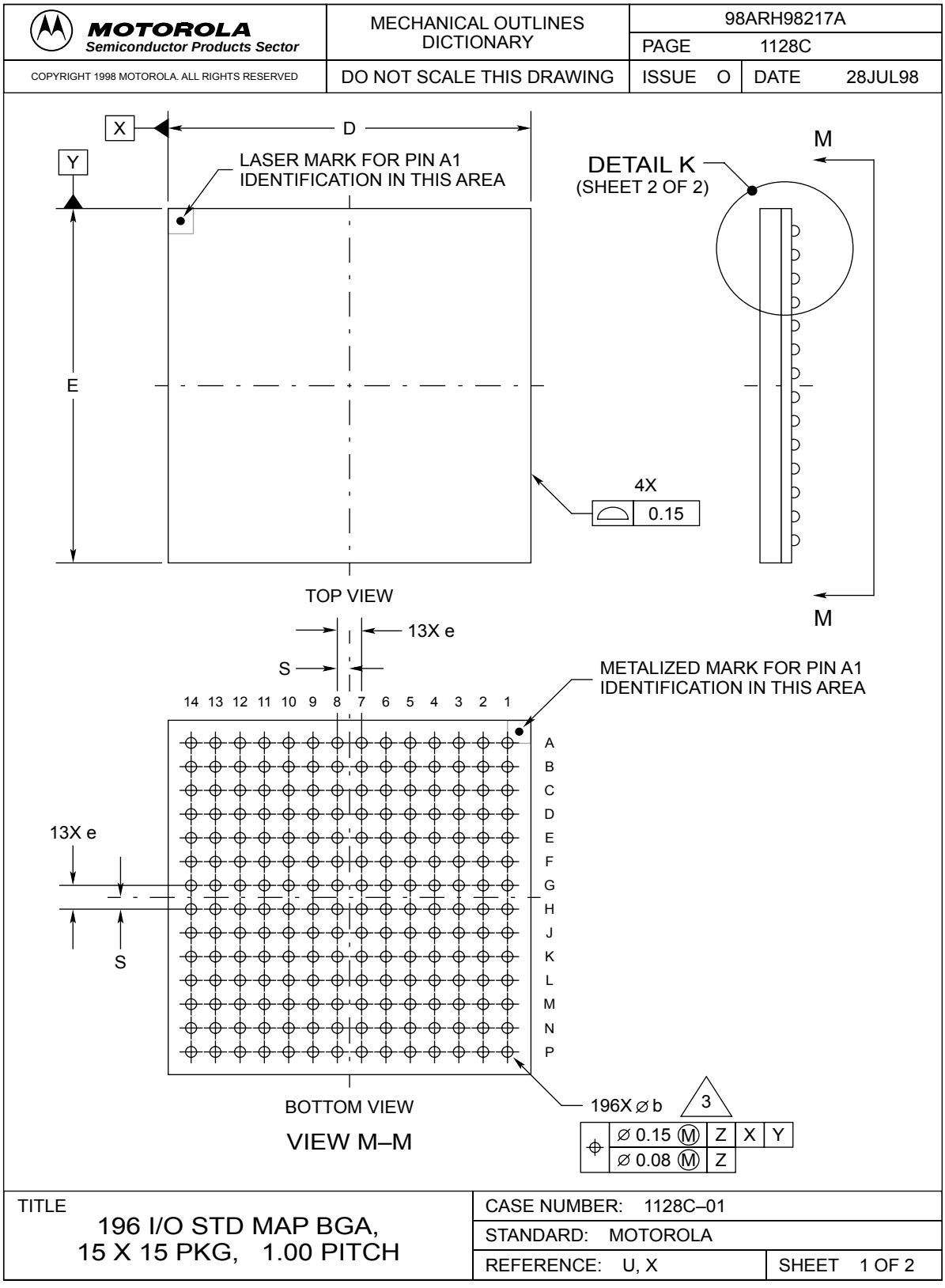
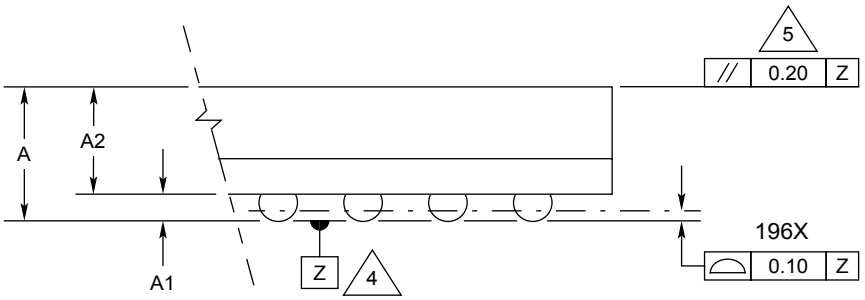


Figure 8-1. 196 MAPBGA Nomenclature

MOTOROLA Semiconductor Products Sector	MECHANICAL OUTLINES DICTIONARY	98ARH98217A	
		PAGE 1128C	
	DO NOT SCALE THIS DRAWING	ISSUE O	DATE 28JUL98



DETAIL K
VIEW ROTATED 90° CLOCKWISE

DIM	MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00	
E	BSC	
e	15.00	
S	BSC	
	1.00 BSC	

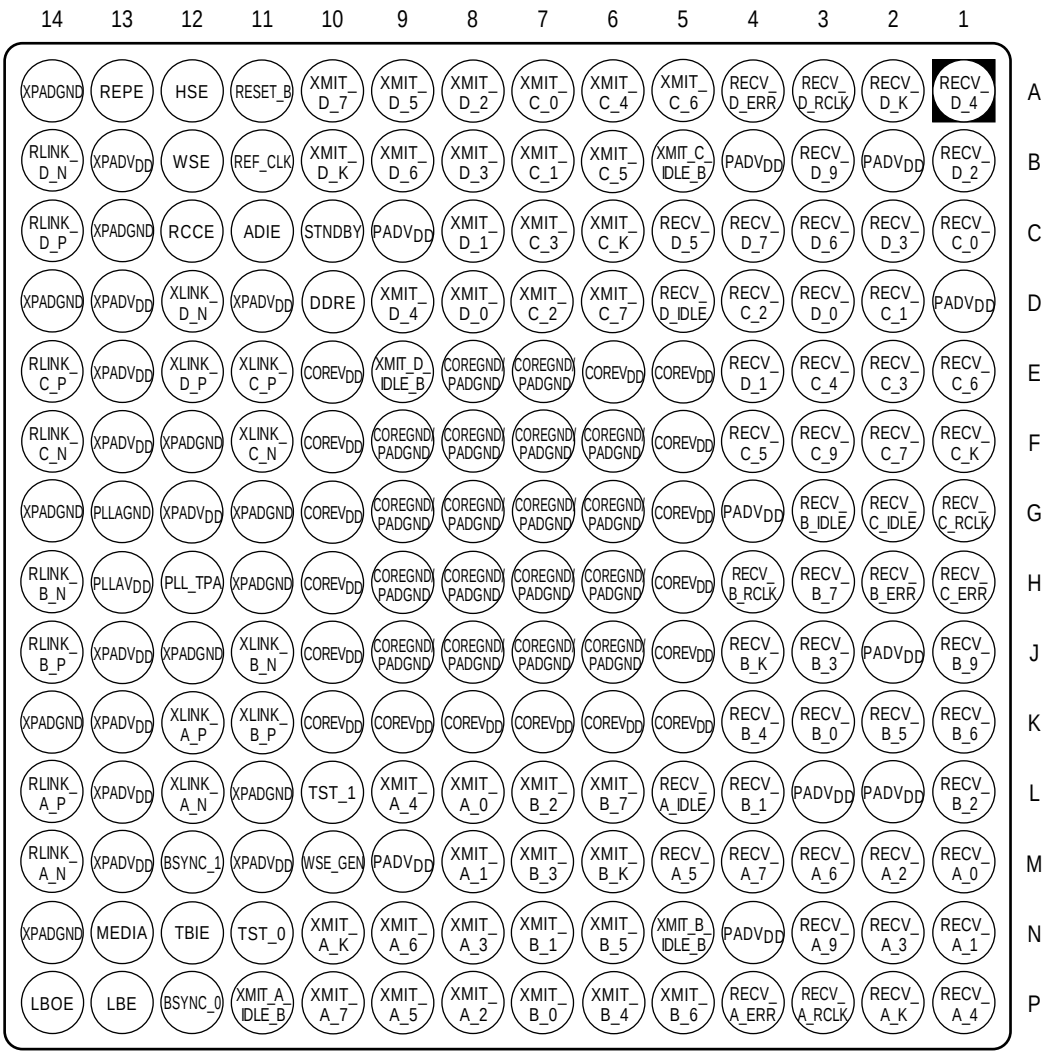
NOTES

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL

TITLE	CASE NUMBER: 1128C–01	
196 I/O STD MAP BGA 15 X 15 PKG, 1.00 PITCH	STANDARD: MOTOROLA	
	REFERENCE: U, X	SHEET 2 OF 2

Figure 8-2. 196 MAPBGA Dimensions

.



View G-G (Bottom View)

Figure 8-3. 196 MAPBGA Package

8.3 Package Thermal Characteristics

Thermal values for the 196 pin MAPBGA are listed below in Table 8-1. The values listed below assume the customer will be mounting the packages on a thermally enhanced mother board. This is defined as a minimum 4-layer board with one ground plane. The values listed below were measured in accordance with established JEDEC (Joint Electron Device Engineering Council) standards.

Table 8-1. MC92602 Package Option Thermal Resistance Values

Symbol	Description	196 MAPBGA	Units
θ_{ja-0}	Thermal resistance from junction to ambient, still air	38	$^{o}C/W$
θ_{ja-2}	Thermal resistance from junction to ambient, 200 LFM [1]	34	$^{o}C/W$
θ_{ja-4}	Thermal resistance from junction to ambient, 400 LFM[1]	33	$^{o}C/W$

[1] Linear feet per minute

8.4 MC92602 Chip Pinout Listing

The MC92602 is offered in a 196 MAPBGA package. Table 8-2 list the MC92602 signal to ball location mapping for the package. Also shown are signaling direction (input or output), and the type of logic interface.

Table 8-2. 196 Signal to Ball Mapping

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
XMIT_A_0	Transmitter A, data bit 0	L8	Input	TTL
XMIT_A_1	Transmitter A, data bit 1	M8	Input	TTL
XMIT_A_2	Transmitter A, data bit 2	P8	Input	TTL
XMIT_A_3	Transmitter A, data bit 3	N8	Input	TTL
XMIT_A_4	Transmitter A, data bit 4	L9	Input	TTL
XMIT_A_5	Transmitter A, data bit 5	P9	Input	TTL
XMIT_A_6	Transmitter A, data bit 6	N9	Input	TTL
XMIT_A_7	Transmitter A, data bit 7	P10	Input	TTL
XMIT_A_K	Transmitter A, special character (data bit 8 for TBI mode)	N10	Input	TTL
$\overline{\text{XMIT\_A\_IDLE}}$	Transmitter A, idle enable bar, (data bit 9 for TBI mode)	P11	Input	TTL

Table 8-2. 196 Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
RECV_A_0	Receiver A, data bit 0	M1	Output	TTL
RECV_A_1	Receiver A, data bit 1	N1	Output	TTL
RECV_A_2	Receiver A, data bit 2	M2	Output	TTL
RECV_A_3	Receiver A, data bit 3	N2	Output	TTL
RECV_A_4	Receiver A, data bit 4	P1	Output	TTL
RECV_A_5	Receiver A, data bit 5	M5	Output	TTL
RECV_A_6	Receiver A, data bit 6	M3	Output	TTL
RECV_A_7	Receiver A, data bit 7	M4	Output	TTL
RECV_A_K	Receiver A, special character (data bit 8 for TBI mode)	P2	Output	TTL
RECV_A_9	Receiver A, data bit 9 for TBI mode	N3	Output	TTL
RECV_A_IDLE	Receiver A, idle detect	L5	Output	TTL
RECV_A_ERR	Receiver A, error detect	P4	Output	TTL
RECV_A_RCLK	Receiver A, receive data clock	P3	Output	TTL
RLINK_A_P	Receiver A, positive link input	L14	Input	Link
RLINK_A_N	Receiver A, negative link input	M14	Input	Link
XLINK_A_P	Transmitter A, positive link out	K12	Output	Link
XLINK_A_N	Transmitter A, negative link out	L12	Output	Link
XMIT_B_0	Transmitter B, data bit 0	P7	Input	TTL
XMIT_B_1	Transmitter B, data bit 1	N7	Input	TTL
XMIT_B_2	Transmitter B, data bit 2	L7	Input	TTL
XMIT_B_3	Transmitter B, data bit 3	M7	Input	TTL
XMIT_B_4	Transmitter B, data bit 4	P6	Input	TTL
XMIT_B_5	Transmitter B, data bit 5	N6	Input	TTL
XMIT_B_6	Transmitter B, data bit 6	P5	Input	TTL
XMIT_B_7	Transmitter B, data bit 7	L6	Input	TTL
XMIT_B_K	Transmitter B, special character (data bit 8 for TBI mode)	M6	Input	TTL
$\overline{\text{XMIT\_B\_IDLE}}$	Transmitter B, idle enable bar, (data bit 9 for TBI mode)	N5	Input	TTL
RECV_B_0	Receiver B, data bit 0	K3	Output	TTL
RECV_B_1	Receiver B, data bit 1	L4	Output	TTL
RECV_B_2	Receiver B, data bit 2	L1	Output	TTL
RECV_B_3	Receiver B, data bit 3	J3	Output	TTL

Table 8-2. 196 Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
RECV_B_4	Receiver B, data bit 4	K4	Output	TTL
RECV_B_5	Receiver B, data bit 5	K2	Output	TTL
RECV_B_6	Receiver B, data bit 6	K1	Output	TTL
RECV_B_7	Receiver B, data bit 7	H3	Output	TTL
RECV_B_K	Receiver B, special character (data bit 8 for TBI mode)	J4	Output	TTL
RECV_B_9	Receiver B, data bit 9 for TBI mode	J1	Output	TTL
RECV_B_IDLE	Receiver B, idle detect	G3	Output	TTL
RECV_B_ERR	Receiver B, error detect	H2	Output	TTL
RECV_B_RCLK	Receiver B, receive data clock	H4	Output	TTL
RLINK_B_P	Receiver B, positive link input	J14	Input	Link
RLINK_B_N	Receiver B, negative link input	H14	Input	Link
XLINK_B_P	Transmitter B, positive link out	K11	Output	Link
XLINK_B_N	Transmitter B, negative link out	J11	Output	Link
XMIT_C_0	Transmitter C, data bit 0	A7	Input	TTL
XMIT_C_1	Transmitter C, data bit 1	B7	Input	TTL
XMIT_C_2	Transmitter C, data bit 2	D7	Input	TTL
XMIT_C_3	Transmitter C, data bit 3	C7	Input	TTL
XMIT_C_4	Transmitter C, data bit 4	A6	Input	TTL
XMIT_C_5	Transmitter C, data bit 5	B6	Input	TTL
XMIT_C_6	Transmitter C, data bit 6	A5	Input	TTL
XMIT_C_7	Transmitter C, data bit 7	D6	Input	TTL
XMIT_C_K	Transmitter C, special character (data bit 8 for TBI mode)	C6	Input	TTL
$\overline{\text{XMIT\_C\_IDLE}}$	Transmitter C, idle enable bar, (data bit 9 for TBI mode)	B5	Input	TTL
RECV_C_0	Receiver C, data bit 0	C1	Output	TTL
RECV_C_1	Receiver C, data bit 1	D2	Output	TTL
RECV_C_2	Receiver C, data bit 2	D4	Output	TTL
RECV_C_3	Receiver C, data bit 3	E2	Output	TTL
RECV_C_4	Receiver C, data bit 4	E3	Output	TTL
RECV_C_5	Receiver C, data bit 5	F4	Output	TTL
RECV_C_6	Receiver C, data bit 6	E1	Output	TTL
RECV_C_7	Receiver C, data bit 7	F2	Output	TTL

Table 8-2. 196 Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
RECV_C_K	Receiver C, special character (data bit 8 for TBI mode)	F1	Output	TTL
RECV_C_9	Receiver C, data bit 9 for TBI mode	F3	Output	TTL
RECV_C_IDLE	Receiver C, idle detect	G2	Output	TTL
RECV_C_ERR	Receiver C, error detect	H1	Output	TTL
RECV_C_RCLK	Receiver C, receive data clock	G1	Output	TTL
RLINK_C_P	Receiver C, positive link input	E14	Input	Link
RLINK_C_N	Receiver C, negative link input	F14	Input	Link
XLINK_C_P	Transmitter C, positive link out	E11	Output	Link
XLINK_C_N	Transmitter C, negative link out	F11	Output	Link
XMIT_D_0	Transmitter D, data bit 0	D8	Input	TTL
XMIT_D_1	Transmitter D, data bit 1	C8	Input	TTL
XMIT_D_2	Transmitter D, data bit 2	A8	Input	TTL
XMIT_D_3	Transmitter D, data bit 3	B8	Input	TTL
XMIT_D_4	Transmitter D, data bit 4	D9	Input	TTL
XMIT_D_5	Transmitter D, data bit 5	A9	Input	TTL
XMIT_D_6	Transmitter D, data bit 6	B9	Input	TTL
XMIT_D_7	Transmitter D, data bit 7	A10	Input	TTL
XMIT_D_K	Transmitter D, special character (data bit 8 for TBI mode)	B10	Input	TTL
$\overline{\text{XMIT\_D\_IDLE}}$	Transmitter D, idle enable bar, (data bit 9 for TBI mode)	E9	Input	TTL
RECV_D_0	Receiver D, data bit 0	D3	Output	TTL
RECV_D_1	Receiver D, data bit 1	E4	Output	TTL
RECV_D_2	Receiver D, data bit 2	B1	Output	TTL
RECV_D_3	Receiver D, data bit 3	C2	Output	TTL
RECV_D_4	Receiver D, data bit 4	A1	Output	TTL
RECV_D_5	Receiver D, data bit 5	C5	Output	TTL
RECV_D_6	Receiver D, data bit 6	C3	Output	TTL
RECV_D_7	Receiver D, data bit 7	C4	Output	TTL
RECV_D_K	Receiver D, special character (data bit 8 for TBI mode)	A2	Output	TTL
RECV_D_9	Receiver D, data bit 9 for TBI mode	B3	Output	TTL
RECV_D_IDLE	Receiver D, idle detect	D5	Output	TTL

Table 8-2. 196 Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
RECV_D_ERR	Receiver D, error detect	A4	Output	TTL
RECV_D_RCLK	Receiver D, receive data clock	A3	Output	TTL
RLINK_D_P	Receiver D, positive link input	C14	Input	Link
RLINK_D_N	Receiver D, negative link input	B14	Input	Link
XLINK_D_P	Transmitter D, positive link out	E12	Output	Link
XLINK_D_N	Transmitter D, negative link out	D12	Output	Link
TBIE	10-bit interface enable	N12	Input	TTL
HSE	Half speed enable	A12	Input	TTL
DDRE	Double data rate enable	D10	Input	TTL
BSYNC_0	Byte synchronization mode Select 0	P12	Input	TTL
BSYNC_1	Byte synchronization mode select 1	M12	Input	TTL
ADIE	Add/Drop idle enable	C11	Input	TTL
REPE	Repeater mode enable	A13	Input	TTL
RCCE	Recovered clock enable	C12	Input	TTL
REF_CLK	Reference clock	B11	Input	TTL
MEDIA	Media impedance select	N13	Input	TTL
WSE	Word synchronization enable	B12	Input	TTL
WSE_GEN	Generate word synchronization event	M10	Input	TTL
PLL_TPA	PLL analog test point	H12	Output	Analog
TST_0	Test mode select 0	N11	Input	TTL
TST_1	Test mode select 1	L10	Input	TTL
LBE	Loop back enable	P13	Input	TTL
LBOE	Loop back output enable	P14	Input	TTL
STNDBY	Standby mode enable	C10	Input	TTL
$\overline{\text{RESET}}$	System reset bar	A11	Input	TTL
COREVDD	Core logic supply	E5, E6, F5, G5, H5, J5, K5, K6, K7, K8, K9, K10, J10, H10, G10, F10, E10	Vdd	Supply

Table 8-2. 196 Signal to Ball Mapping (continued)

Signal Name	Description	Ball Number (196 MAPBGA)	Direction	I/O Type
COREGND/PADGND	Core logic ground / TTL I/O ground	E7, E8, F6, F7, F8, F9, H6, H7, H8, H9, G6, G7, G8, G9, J6, J7, J8, J9	GND	Ground
PLLAVDD	PLL analog supply	H13	AVdd	Supply
PLLAGND	PLL analog ground	G13	GND	Ground
PADVDD	TTL I/O supply	B2, D1, G4, J2, L2, L3, N4, M9, C9, B4	OVdd	Supply
XPADVDD	Link I/O supply	L13, K13, G12, E13, D11, D13, M11, M13, J13, F13, B13	XVdd	Supply
XPADGND	Link I/O Ground	K14, J12, G11, F12, D14, N14, L11, G14, A14, H11, C13	GND	Ground

Appendix A
Ordering Information

Figure A-1 provides the Motorola part numbering nomenclature for the MC92602 SERDES. For product availability, contact your local Motorola Semiconductor sales representative.

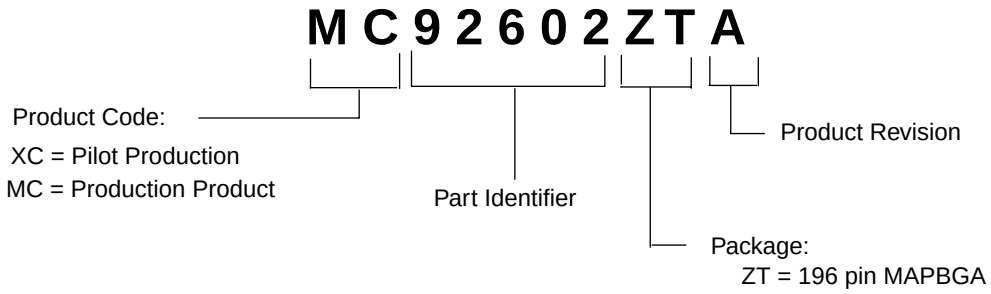


Figure A-1. Motorola Part Number Key

Appendix B
8B/10B Coding Scheme

The MC92602 provides fibre channel-specific 8B/10B encoding and decoding based on the FC-1 fibre channel standard. Given 8 bits entering a channel, the 8B/10B encoding converts them to 10 bits thereby increasing the transition density of the serially transmitted signal.

B.1 Overview

The FC-1 standard applies an algorithm that ensures that no more than five 1's or 0's are transmitted consecutively, giving a transition density equal to 2.5 for each 10 bit data block. Such a density ensures proper DC balance across the link and is sufficient for good clock recovery.

In the 8B/10B notation scheme, bytes are referred to as transmission characters, and each bit is represented by letters. Unencoded bits, the 8 bits that have not passed through a 8B/10B encoder, are represented by letters "A" through "H", which are bits 0 through7.

One unencoded transmission character (Byte)							
H	G	F	E	D	C	B	A
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							↑ lsb

Figure B-1. Unencoded Transmission Character Bit Ordering

Encoded bits, those that have passed through an encoder, are represented with the letters "a" through "j", representing bits 0–9 respectively. Character (bit) ordering in the fibre channel nomenclature is little-endian, with "a" being the least significant bit in a byte.

One coded transmission character (Byte)									
j	h	g	f	i	e	d	c	b	a
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
									↑ lsb

Figure B-2. Encoded Transmission Character Bit Ordering

B.1.1 Naming Transmission Characters

Transmission characters are given names based on the type of data in the byte and the bit values of the character. Two types of transmission characters are specified: data and special. Data characters are labeled “D” characters and special characters are labeled “K” characters. Each transmission character has a bit value and a corresponding decimal value. These elements are combined to provide each character with a name, see Table B-1.

Table B-1. Components of a Character Name

H G F	E D C B A	8B/10B notation
0 0 1	1 1 1 0 0	Data bit value
1	28	Decimal value of the bit value
D or K		Kind of transmission character
D28.1 = Data name assigned to this data byte if it is a data character. K28.1 = Data name assigned to this data byte if it is a special character.		

B.1.2 Encoding

Following is a simplified sequence of steps in 8B/10B coding:

1. An 8-bit block of unencoded data (a transmission character) is picked up by a transmitter.
2. The transmission character is broken into sub-blocks of three bits and five bits. The letters H G and F comprise the 3-bit block, and the letters E D C B and A comprise the 5-bit block.
3. The 3-bit and 5-bit sub-blocks pass through a 3B/4B encoder and a 5B/6B encoder, respectively. A bit is added to each sub-block, such that the transmission character is encoded and expanded to a total of 10-bits.
4. At the time the character is expanded into 10 bits, it is also encoded into the proper running disparity, either positive (RD+) or negative (RD-) depending on certain calculations (see Section B.1.3, “Calculating Running Disparity”). At start-up, the transmitter assumes negative running disparity.

5. The positive or negative disparity transmission character (see Figure B-3) is passed to the transmit driver, available for differentialization (See Section 2.3.3, “Transmit Driver Operation”).

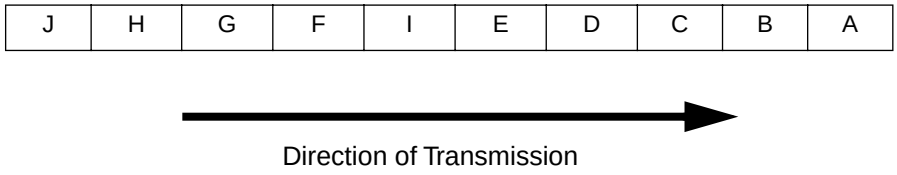


Figure B-3. Character Transmission

B.1.3 Calculating Running Disparity

Running disparity improves error detection and recovery. The rules for calculating the running disparity for sub-blocks are as follows (reference *Fibre Channel, Gigabit Communications and I/O for Computer Networks*):

- Running disparity at the end of any sub-block is positive if (1) the encoded sub-block contains more 1s than 0s, (2) if the 6-bit sub-block is 6’b00 0111, or (3) if the 4-bit sub-block is 4’b0011.
- Running disparity at the end of any sub-block is negative if (1) the encoded sub-block contains more 0 than 1 bits, (2) if the 6-bit sub-block is 6’b11 1000, or (3) if the 4-bit sub-block is 4’b1100.
- Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

B.2 Data Tables

Table B-2 displays the full valid data character 8B/10B codes. The values in the “Data Value HGFEDCBA” column are the possible bit values of the unencoded transmission characters. The current RD values are the possible positive and negative running disparity values.

Table B-2. Valid Data Characters

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	010101 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110

Table B-2. Valid Data Characters (continued)

Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Data Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table B-3 displays the full valid special character 8B/10B codes.

Table B-3. Valid Special Characters

Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdei fghj	Name	Data Value HGF EDCBA	Current RD- abcdei fghj	Current RD+ abcdie fghj
K28.0	000 11100	001111 0100	110000 1011	K28.6	110 11100	001111 0110	110000 1001
K28.1	001 11100	001111 1001	110000 0110	K28.7	111 11100	001111 1000	110000 0111
K28.2	010 11100	001111 0101	110000 1010	K23.7	111 10111	111010 1000	000101 0111
K28.3	011 11100	001111 0011	110000 1100	K27.7	111 11011	110110 1000	001001 0111
K28.4	100 11100	001111 0010	110000 1101	K29.7	111 11101	101110 1000	010001 0111
K28.5	101 11100	001111 1010	110000 0101	K30.7	111 11110	011110 1000	100001 0111

Glossary of Terms and Abbreviations

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this book. Some of the terms and definitions included in the glossary are reprinted from IEEE Std 754-1985, *IEEE Standard for Binary Floating-Point Arithmetic*, copyright ©1985 by the Institute of Electrical and Electronics Engineers, Inc., with the permission of the IEEE.

A

Asserted. Indicates active state of signal has been set. Refers to either inputs or outputs.

B

BERC. Bit Error Rate Checking.

BERT. Bit Error Rate Testing.

BIST. Built-In Self-Test.

Bit alignment. Refers to the transition tracking loop recovering data bits from the serial input stream.

Byte. Eight bits of uncoded data.

Byte alignment. Receiver identification of character boundaries through use of Idle character recognition.

C

Character. An 8B/10B encoded byte of data.

G

Gigabit. A unit of speed of data transfer. One gigabit indicates a data throughput of 1 billion bits per second requiring a transfer rate of 1.25 billion symbols per second of 8B/10B encoded data.

Gigabaud. A unit of speed of symbol transfer. One gigabaud indicates a data throughput of 800 million bits per second requiring a transfer rate of 1.0 billion symbols per second of 8B/10B encoded data.

I

ISI. Inter Symbol Interference, a distortion caused by the high-frequency loss characteristics of the transmission media.

N

Negated. Indicates inactive state of signal has been set. Refers to either inputs or outputs.

P

PLL. Phase Locked Loop.

PPM. parts per million.

R

Running disparity. The amount of DC imbalance over a history of symbols transmitted over a link. Equal to the difference between the number of one and zero symbols transmitted.

S

Symbol. One piece of information sent across the link; different from a bit in that bit implies data where symbol is encoded data.

W

Word synchronization. Alignment of four or more receivers' data by adjusting for differences in media and systemic delay between them such that data is presented by the receivers in the same grouping as they were transmit.

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