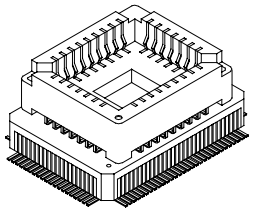
SONY

CXP87700

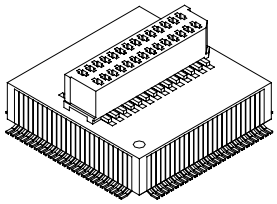
CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

100 pin PQFP (Ceramic)



QFP supported



LQFP supported

Description

The CXP87700 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87740/87748.

Features

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 333ns at 12MHz operation (3.0 to 5.5V)
  250ns at 16MHz operation (4.5 to 5.5V)
- Applicable EPROM — LCC type 27C256, LCC type 27C512
  (Maximum 48Kbytes are available)
- Incorporated RAM capacity — 1344bytes
- Peripheral functions
  - A/D converter — 8-bit, 12-channel, successive approximation method
    (Conversion time of 20µs/16MHz)
  - Serial interface — Incorporated 8-bit, 8-stage FIFO
    (auto transfer for 1 to 8bytes), 1-channel
    8-bit clock synchronous 1-channel
  - Timer — 8-bit timer
    8-bit timer/counter
    19-bit time base timer
    32kHz timer/counter
  - High precision timing pattern generator — PPG 19-pin, 32-stage programmable
    RTG 5-pin, 2-channel
  - PWM/DA gate output — PWM output 12-bit, 2-channel
    (repetitive frequency 62.5kHz/16MHz)
    DA gate pulse output 12-bit, 4-channel
  - Servo input control — Capstan FG, drum FG/PG, CTL input
  - VSYNC separator
  - FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - PWM output — 14-bit, 1-channel
  - VISS/VASS circuit — Pulse duty auto detection circuit
  - Remote control receiving circuit — 8-bit pulse measuring counter 6-stage FIFO
- Interruption — 21 factors, 15 vectors, multi-interruption possible
- Standby mode — Sleep/stop
- Package — 100-pin ceramic PQFP

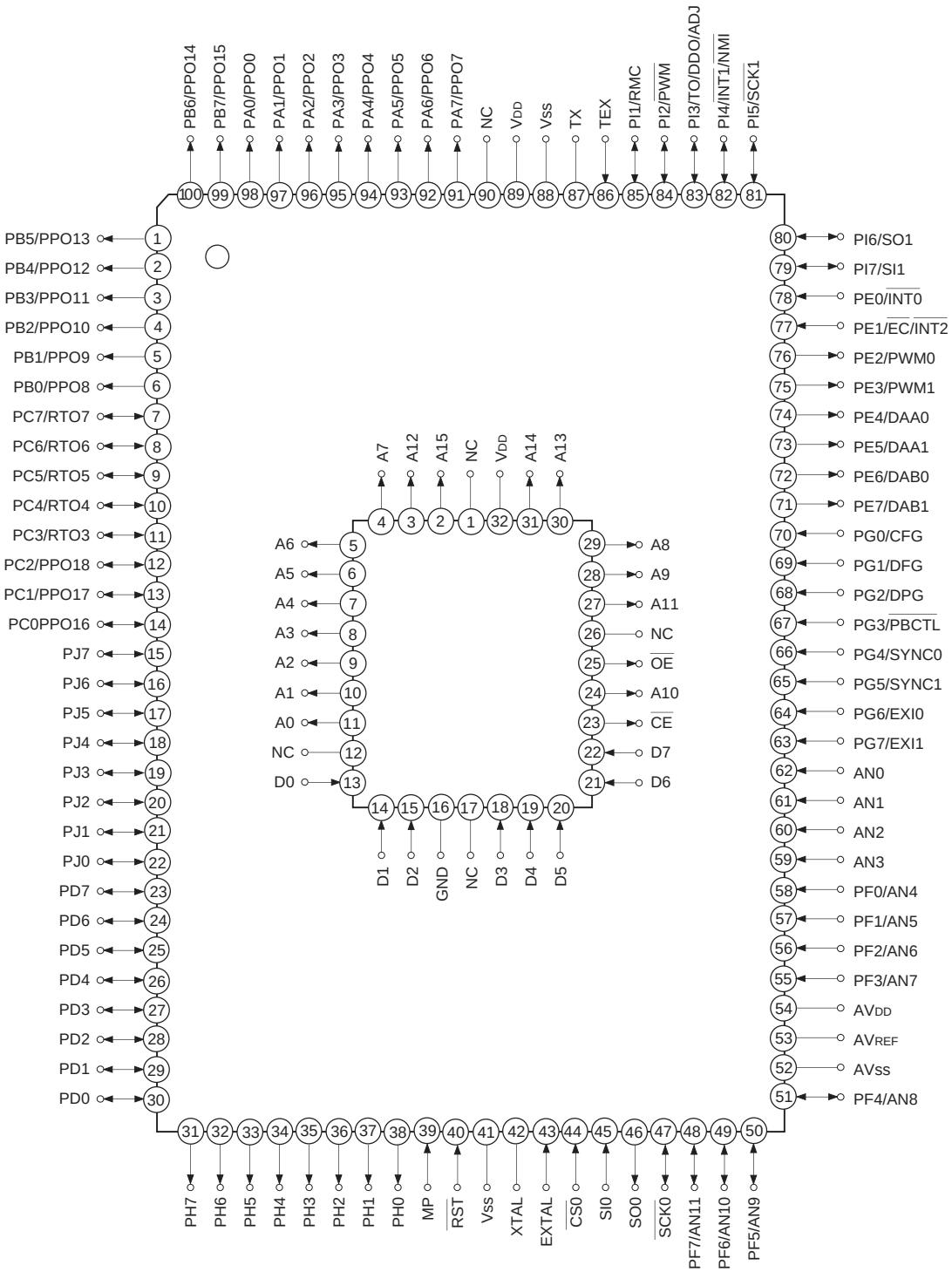
Note) Mask option depends on the type of the CXP87700. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

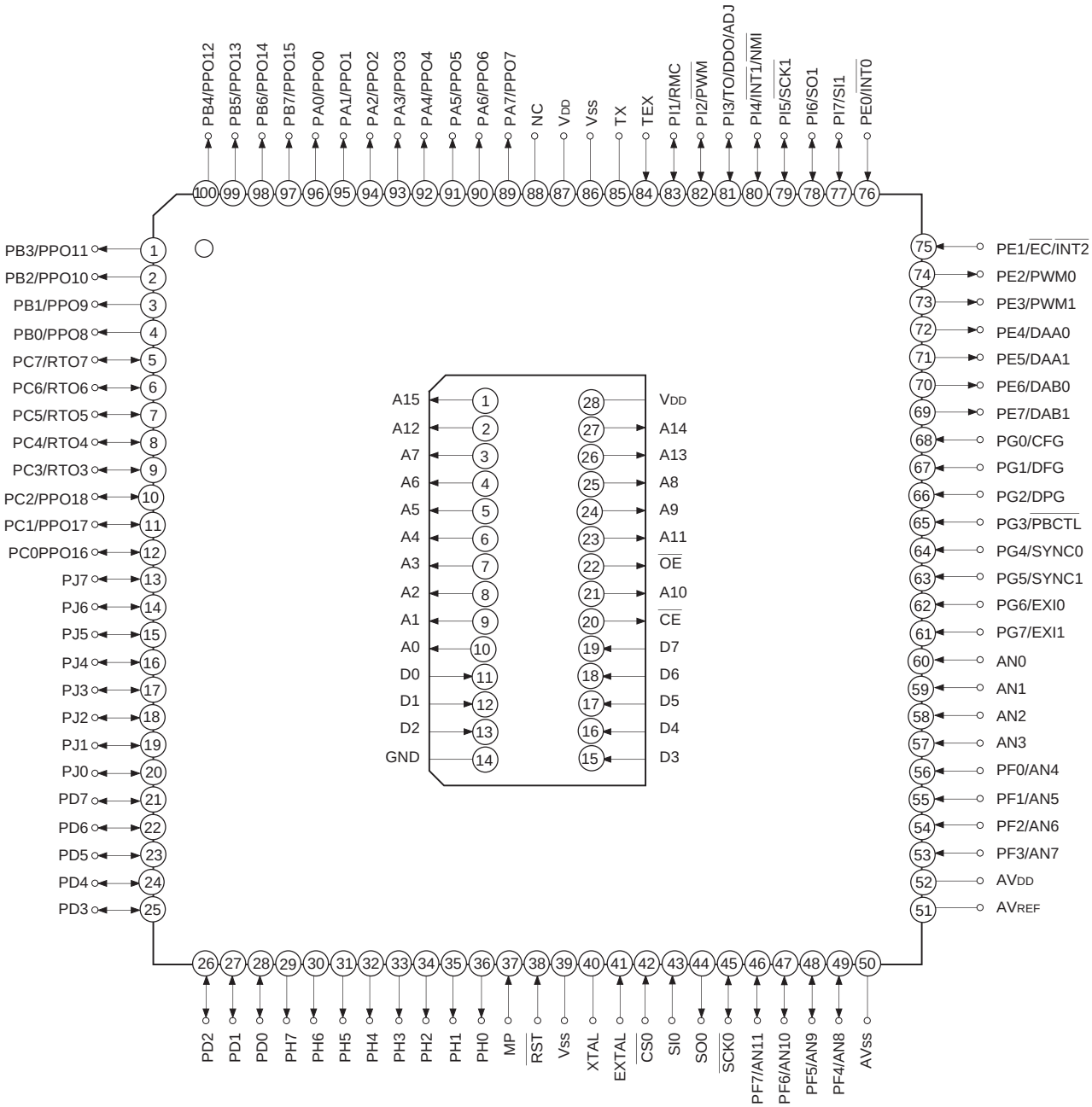
E93X14B81-PS

Pin Assignment in Piggyback Mode (QFP package)



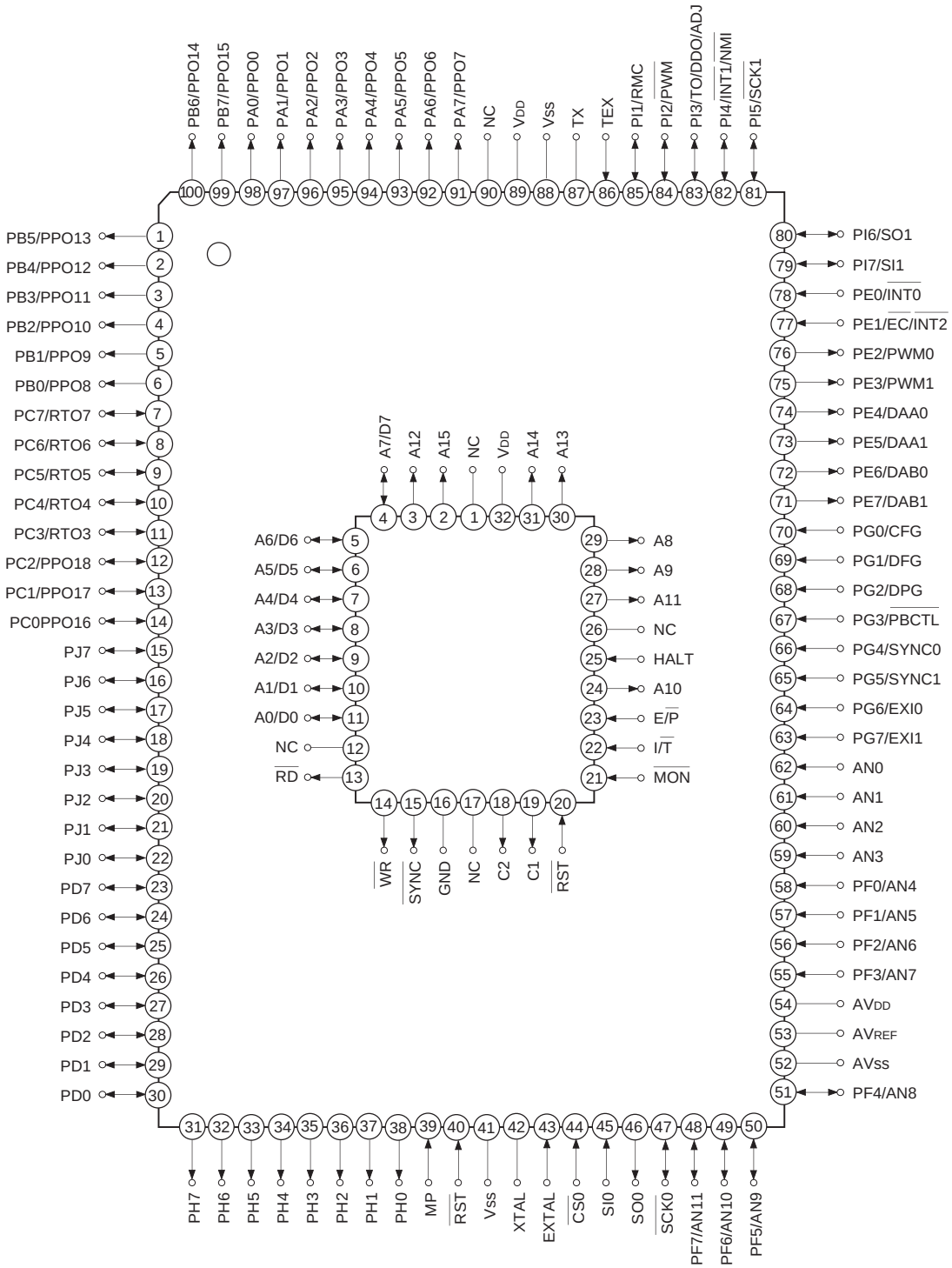
Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

Pin Assignment in Piggyback Mode (LQFP package)



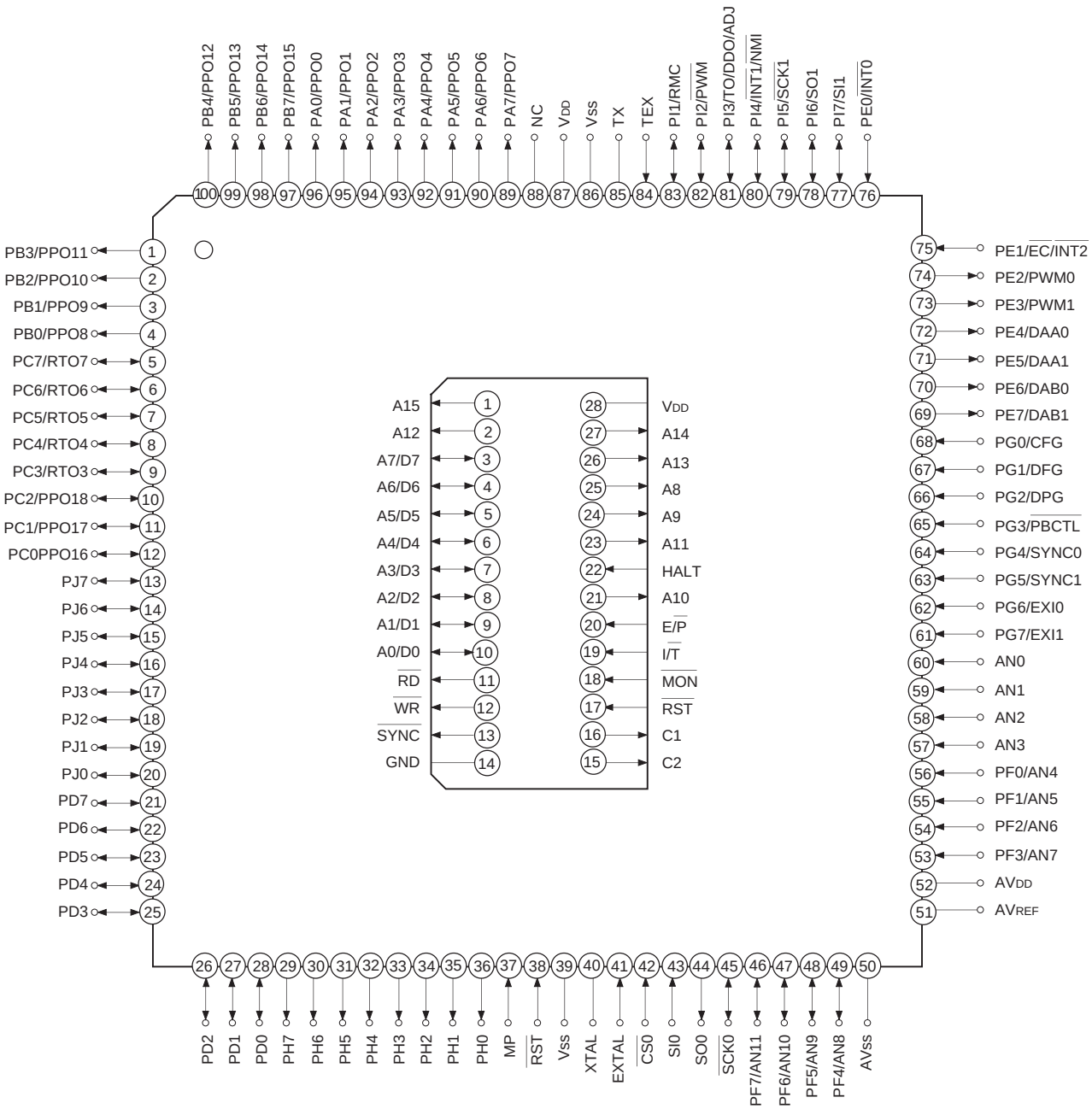
Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. V_{SS} (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

Pin Assignment in Evaluator Mode (LQFP package)



Note) 1. NC (Pin 88) is always connected to V_{DD}.
2. V_{SS} (Pins 39 and 86) are both connected to GND.
3. MP (Pin 37) is always connected to GND.

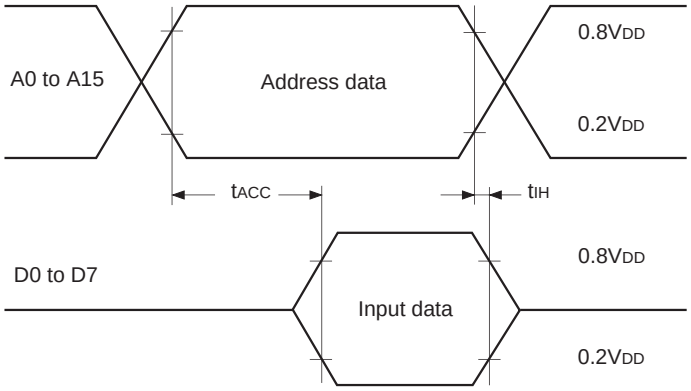
EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1 75*2	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation (V_{DD} = 4.5 to 5.5V)

*2 At 12MHz operation (V_{DD} = 3.0 to 5.5V), At 16MHz operation (V_{DD} = 4.5 to 5.5V)

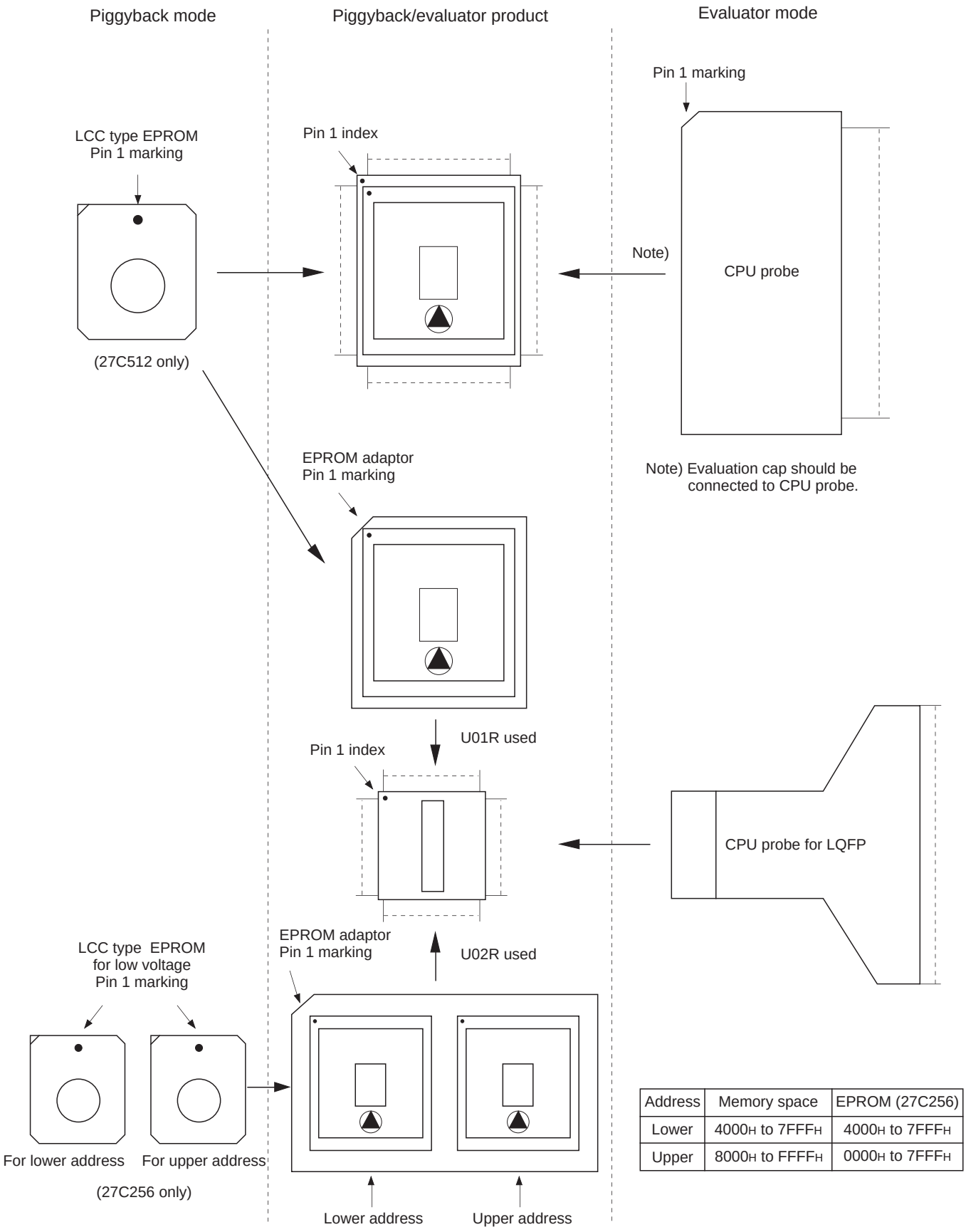


Products List

Optional item	Products			
	Mask		Piggyback/evaluator product	
	CXP87740	CXP87748	CXP87700-U01Q CXP87700-U01R	CXP87700-U02R
Package	100-pin plastic QFP/LQFP		100-pin ceramic PQFP	
ROM capacitance	40Kbytes	48Kbytes	EPROM 48Kbytes	
			27C512 × 1	27C256 × 2
Pull-up resistance for reset pin	Existent/Non-existent		Existent	
Power on reset circuit	Non-existent		Non-existent	
Input circuit format*1	CMOS schmitt/TTL schmitt		TTL schmitt	CMOS schmitt

*1 On PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

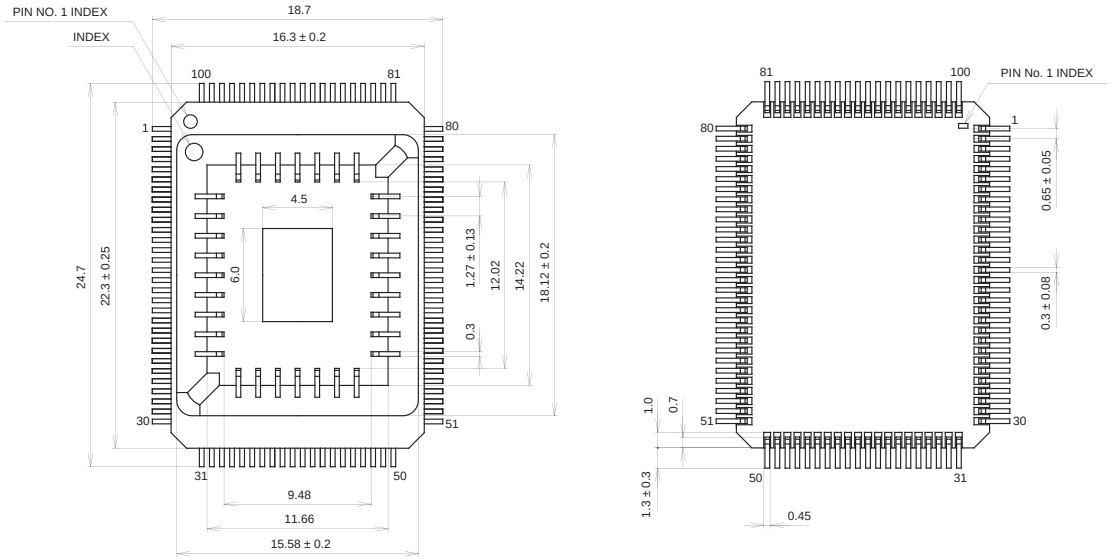
Piggyback mode/evaluator mode can be switched as shown below

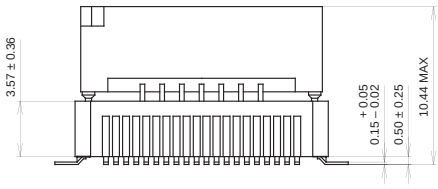


Address	Memory space	EPROM (27C256)
Lower	4000H to 7FFFH	4000H to 7FFFH
Upper	8000H to FFFFH	0000H to 7FFFH

Package Outline Unit: mm

100PIN PQFP (CERAMIC)



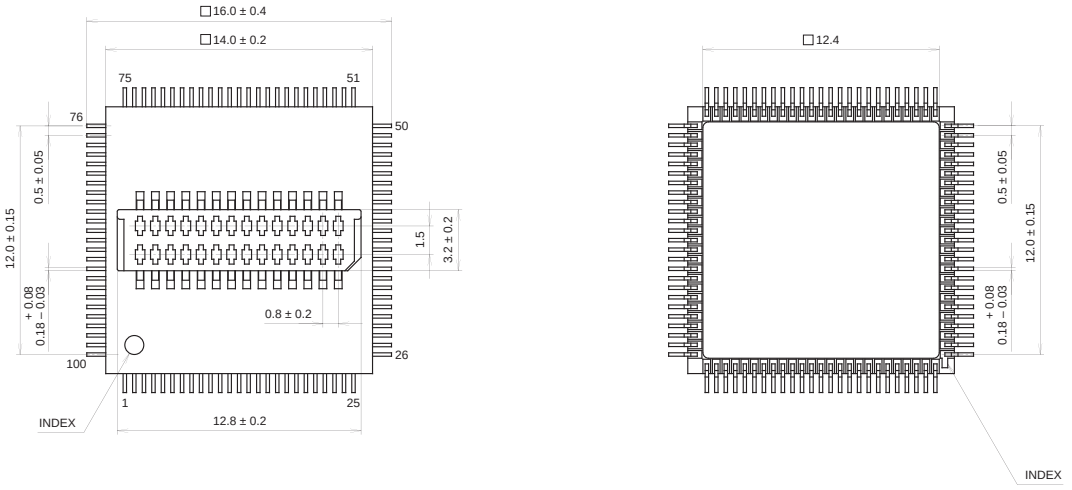


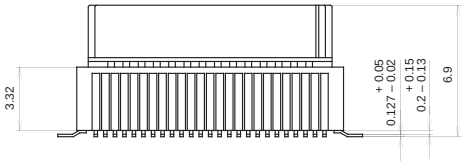
PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)





PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g