AMD Athlon™ VID/FID INTERFACE

Features

- 5-bit voltage identification (VID) interface logic for Athlon™ processor VDD_CORE circuitry
- Selectable 'Sleep' and 'On' VID code inputs
- 4-bit frequency identification (FID) interface logic with level shifter (2.5V to 3.3V)
- North Bridge-compatible open-drain FID outputs
- Built-in 2.5V/50mA voltage regulator with enable input
- Voltage regulator designed specifically for power-conscious battery-powered devices

Applications

- AMD Athlon™ processor-based products
- Motherboards
- Notebook computers

Product Description

The CMBUS100 VID/FID Interface is designed for use in microprocessor systems based on the AMD Athlon™ processors. The CMBUS100 provides the voltage identification (VID) interface logic required between an Athlon CPU and its associated VDD_CORE voltage regulator, as well as the frequency identification (FID) interface logic necessary between the CPU and the North Bridge controller.

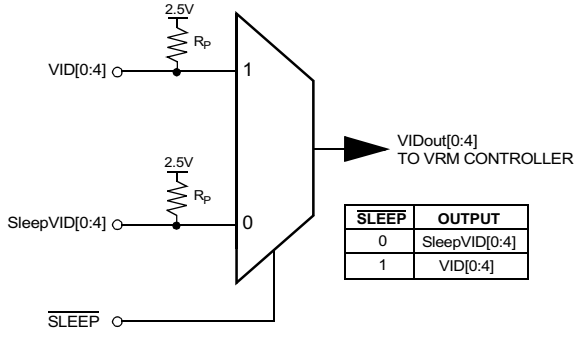
For the five VID code bit lines, the CMBUS100 provides a level-shifting function from the CPU's 2.5V output to the 3.3V that the VDD_CORE voltage regulator requires. Furthermore, there is an onboard multiplexer which enables selecting between the full-speed VID code of the CPU and a user-selectable 'Sleep' or 'Soft' VID code (the desktop system processor requires a 'Sleep' VID code whereas the mobile system processor requires a 'Soft' VID input).

For the 4 FID code bit lines, the CMBUS100 provides a level shifting function from the CPU's 2.5V output to the open-drain outputs that the North Bridge requires.

The CMBUS100 also features a 2.5V voltage regulator, which serves as the supply for the internal 2.5V pull-up resistors on the VID and FID inputs as well as providing a minimum of 50mA current for external loads. This is a series regulator which uses much less current than a shunt regulator, resulting in power savings and a longer battery life in notebook computers.

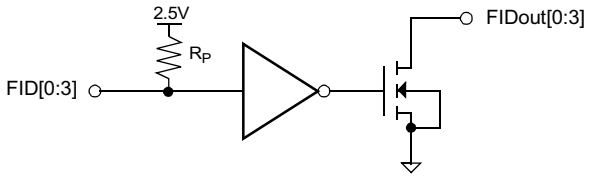
The CMBUS100 IC is available in a space-saving QSOP-28 package, and is fabricated with California Micro Devices' CMOS process.

Electrical Schematic

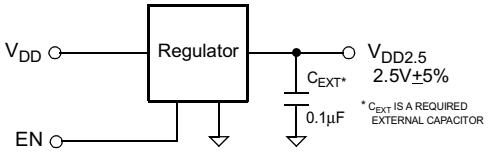


SLEEP	OUTPUT
0	SleepVID[0:4]
1	VID[0:4]

Voltage Identification (VID) Logic

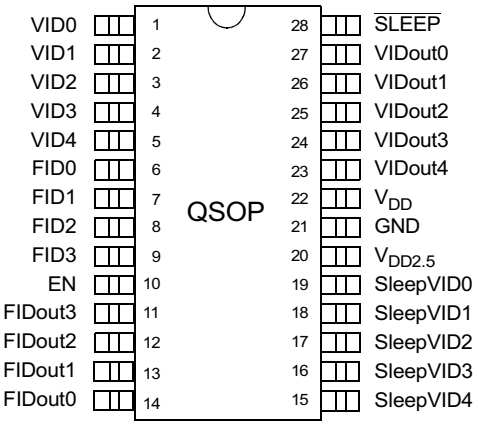


Frequency Identification (FID) Logic



Voltage Regulator Circuit

PACKAGE / PINOUT DIAGRAM



CMBUS100
QSOP-28 Package

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN(s)	NAME	DESCRIPTION
1-5	VID0–VID4	Bits 0 through 4 of the VCC_CORE ID input from processor, respectively. Each input has an internal 27KΩ pull-up resistor to 2.5V.
6-9	FID0–FID3	Bits 0 through 3 of the VID input from processor, respectively. Each input has an internal 27KΩ pull-up resistor to 2.5V.
10	EN	Regulator enable pin. This is an active high, 5.5V tolerant input which can be connected directly to V_{CC5} (5V), thus shutting down the regulator when V_{CC5} is turned off.
11-14	FIDout3–FIDout0	Bits 3 to 0 of the level-shifted FID output, respectively. These are open-drain outputs and are 5.5V tolerant.
15-19	SleepVID4–SleepVID0	Bits 4 through 0 of the SleepVID or SoftVID input, respectively. Each input has an internal 27KΩ pull-up resistor to 2.5V.
20	$V_{DD2.5}$	2.5V output from the voltage regulator. Can be used to power external pull-up resistors. This pin requires a 0.1µF decoupling capacitor to be connected as close as possible to it (see Note1).
21	GND	Device ground.
22	V_{DD}	3.3V supply input.
23-27	VIDout4–VIDout0	Bits 4 to 0 of the level-shifted VID output, respectively. These are 3.3V CMOS logic outputs.
28	$\overline{\text{SLEEP}}$	3.3V logic input to select between VID(0:4) inputs and SleepVID(0:4) inputs. When $\overline{\text{SLEEP}}$ is asserted low, the SleepVID(0:4) inputs are selected. When $\overline{\text{SLEEP}}$ is asserted high, the VID(0:4) inputs are selected. For systems based on the Athlon desktop processor, it is intended that this input be driven by the Power Management S1 state logic. For systems based on the mobile processor, it is intended that this input will be driven by the Power Good logic.

Note 1: It is essential that a 0.1µF decoupling capacitor be placed between $V_{DD2.5}$ and GND as close as possible to these pins. This capacitor is required to ensure the stability of the 2.5V regulator.

Ordering Information

PART NUMBERING INFORMATION			
Pins	**Package**	**Ordering Part Number[1]**	**Part Marking**
28	QSOP-28	CMBUS100Q	CMBUS100Q

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Supply Voltage, V_{DD}	5.5	V
Regulator Current	150	mA
Load current at open-drain FID outputs and CMOS VID outputs	6	mA
Storage Temperature Range	-65 to +150	°C
DC Package Power Rating	1000	mW

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Supply Voltage, V_{DD}	$3.15 \le V_{DD} \le 3.45$	V
Operating Temperature Range	0 to +70	°C

ELECTRICAL OPERATING CHARACTERISTICS[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" input voltage EN VID(0:4), SleepVID(0:4), FID(0:3) $\overline{SLEEP}$	V_{DD}=3.3V	 1.75 1.75 1.75		 5.5 2.9 3.7	 V V V
V_{IL}	Logic "0" input voltage EN VID(0:4), SleepVID(0:4), FID(0:3) $\overline{SLEEP}$	V_{DD}=3.3V	 -0.4 -0.4 -0.4		 0.75 0.75 0.75	 V V V
V_{FIDout}	Open-drain output voltage FIDout(0:3) outputs		0		5.5	V
I_{LOAD}	Load current FIDout(0:3) outputs VIDout(0:4) outputs				 6.0 6.0	 mA mA
I_{DD}	Supply Current	V_{DD}=3.3V; VID(0:4), SleepVID(0:4) and FID(0:3) inputs all at logic "1"		0.5	1.0	mA
$V_{VDD2.5}$	Regulator Output Voltage (at Pin 20)	$3.15 \leq V_{DD} \leq 3.45$; I_L=50mA	2.375	2.5	2.625	V
$I_{VDD2.5}$	Regulator Output Current (at Pin 20)	$3.15 \leq V_{DD} \leq 3.45$	50	100		mA
R_{ON}	"On" resistance of FID open-drain output (N-FET)		50	100	200	Ω
R_P	Pull-up resistance value	V_P = 2.5V	13.5	27.0	40.5	kΩ
V_{ESD}	ESD Withstand Voltage, Human Body Model, MIL-STD-883, Method 3015	Note 2,3	±2			kV

Note 1: T_A = 0 to +70°C.

Note 2: ESD applied to input and output pins with respect to GND, one at a time.

Note 3: These parameters are guaranteed by design and characterization.

Application Information

The CMBUS100 provides an easy way to interface the FID and VID signals from the AMD Athlon CPU to the North Bridge controller and the VRM controller/regulator. It also requires the least amount of board space.

Internal pull-up resistors (27kΩ nom.) are present at all inputs to the CMBUS100. External pull-up resistors may be added in parallel if lower resistances are required.

For the sleepVID(0:4) inputs, which set the VID code for the sleep and reset states, we suggest using either terminal pins or optional zero ohm resistors to short the individual sleepVID(0:4) inputs to ground.

The VIDout(0:4) outputs are 3.3V CMOS outputs. These outputs do not require pull-up resistors.

The FIDout(0:3) outputs are open-drain outputs. These require pull-up resistors. Consult your North Bridge design documentation for the possible range of values. Note that the current must not exceed 6mA, so for a 3.3V North Bridge the pull-up resistors cannot be less than 550Ω. We recommend using a much higher value, for example, 10kΩ, to minimize power consumption. The FIDout signals are tolerant of voltages up to 5.5V.

The 2.5V regulator is a series regulator, so the DC current consumption will be much less than a shunt type regulator, contributing to extended battery life in notebook computers. The regulated 2.5V output is used internally in the CMBUS100 for the R_P pull-up resistors, and is also available for external loads (50mA guaranteed, 100mA typical). A 0.1µF capacitor must be connected to the 2.5V output pin (pin 20) to ensure the stability of the regulator.

This regulator can be disabled by a logic LOW on the 'EN' pin (pin 10). Pin 10 is a 5.5V-tolerant input, so it can be connected to any signal which goes LOW during the system 'suspend to RAM' state. We suggest VCC5 because it is probably the easiest to route to.

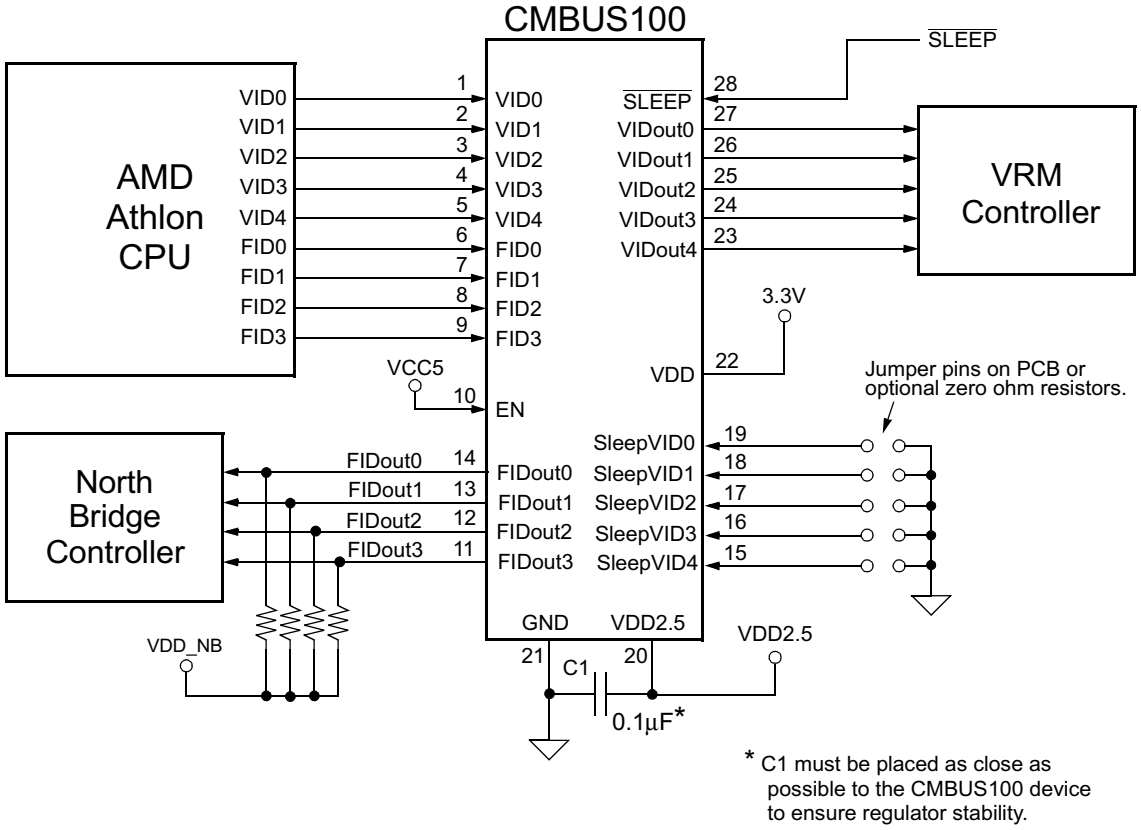


Figure 1. Athlon/North Bridge system application example for the CMBUS100.

Mechanical Details

QSOP Mechanical Specifications:

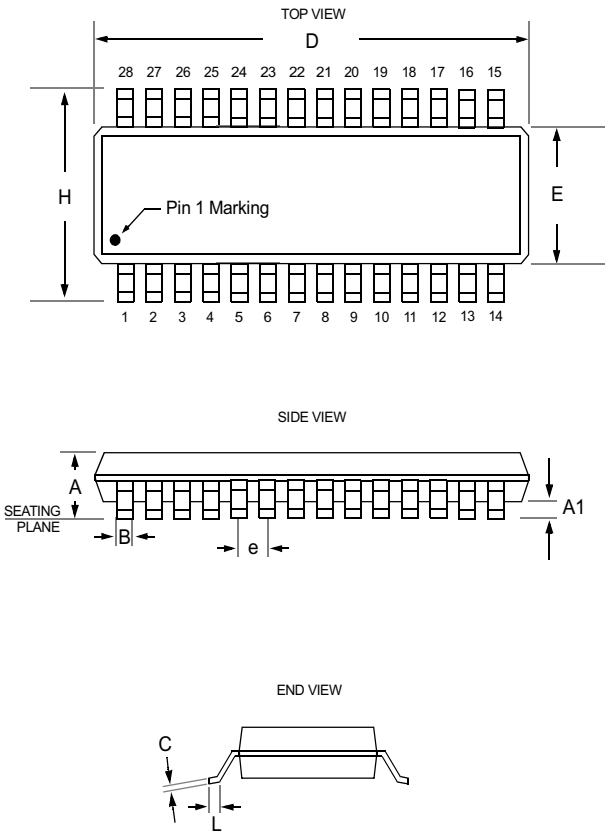
CMBUS100 devices are packaged in 28-pin QSOP packages. Dimensions are presented below.

For complete information on the QSOP-28 package, see the California Micro Devices QSOP Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP (JEDEC name is SSOP)			
Pins	28			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	9.80	9.98	0.386	0.393
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling Dimensions: inches				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for QSOP-28