

# 1

## PRODUCT OVERVIEW

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The S3C7565/P7565 single-chip CMOS microcontroller is designed for high performance in the application for Caller-ID, Telephone using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangable Microcontrollers).

Featuring a DTMF generator, up-to-960-dot LCD direct drive capability, one 8-bit timer/counter and flexible two 8-bit timer/counters, and serial I/O interface, the S3C7565/P7565 offer an excellent design solution for a wide variety of applications requiring DTMF, LCD support.

Up to 43 (including COM/SEG) pins in the 100-pin QFP package can be dedicated to I/O. Nine vectored interrupts provide a fast response to internal and external events. In addition the advanced CMOS technology of the S3C7565/P7565 ensures low power consumption with a wide operating voltage range.

### OTP

The S3C7565 microcontroller is also available in OTP (One Time Programmable) version, S3P7565. S3P7565 microcontroller has an on-chip 16 K-byte one-time-programmable EPROM instead of masked ROM. The S3P7565 is comparable to S3C7565, both in function and in pin configuration.

## FEATURES SUMMARY

### Memory

- 16K × 8-bit ROM
- 5,120 × 4-bit RAM (excluding LCD RAM)

### I/O Pins

- Input only: 4pins (Not including COM/SEG)  
6pins (Including COM/SEG)
- I/O: 15pins (Not including COM/SEG)  
43pins (Including COM/SEG)

### Memory-Mapped I/O Structure

- Data memory bank 15

### 8-bit Basic Timer

- Four interval timer functions
- Watchdog timer

### 8-bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider

### 16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Configurable as two 8-bit Timers
- Serial I/O interface clock generator

### Watch Timer

- Time interval generation: 0.5 s, 3.9 ms  
at 32.768 kHz
- 4 frequency outputs to BUZ pin (0.5, 1, 2, 4 kHz)  
at 32.768 kHz

### Comparator

- 4-channel mode: Internal reference (4-bit resolution); 16-step variable reference voltage
- 3-channel mode: External reference

### DTMF Generator

- 16 dual-tone for tone dialing

### 8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable

### LCD Controller/Driver

- 60 SEG x 16 COM terminals
- 8, 12 and 16 com selectable
- COM 8–15: shared with port
- SEG40–59: shared with port
- Two kinds of LCD bias resistor value

### Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

### Interrupts

- Four external interrupt vectors
- Five internal interrupt vectors
- Two quasi-interrupts

### Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Subsystem clock stop mode

### Oscillation Sources

- RC, Crystal or Ceramic for system clock
- Oscillation frequency: 0.4–6.0 MHz
- CPU clock divider circuit (by 4, 8, or 64)

### Instruction Execution Times

- 1.12, 2.23, 17.88  $\mu$ s at 3.58 MHz
- 0.67, 1.33, 10.7  $\mu$ s at 6.0 MHz
- 122  $\mu$ s at 32.768 kHz (subsystem)

### Operating Temperature

- –40 °C to 85 °C

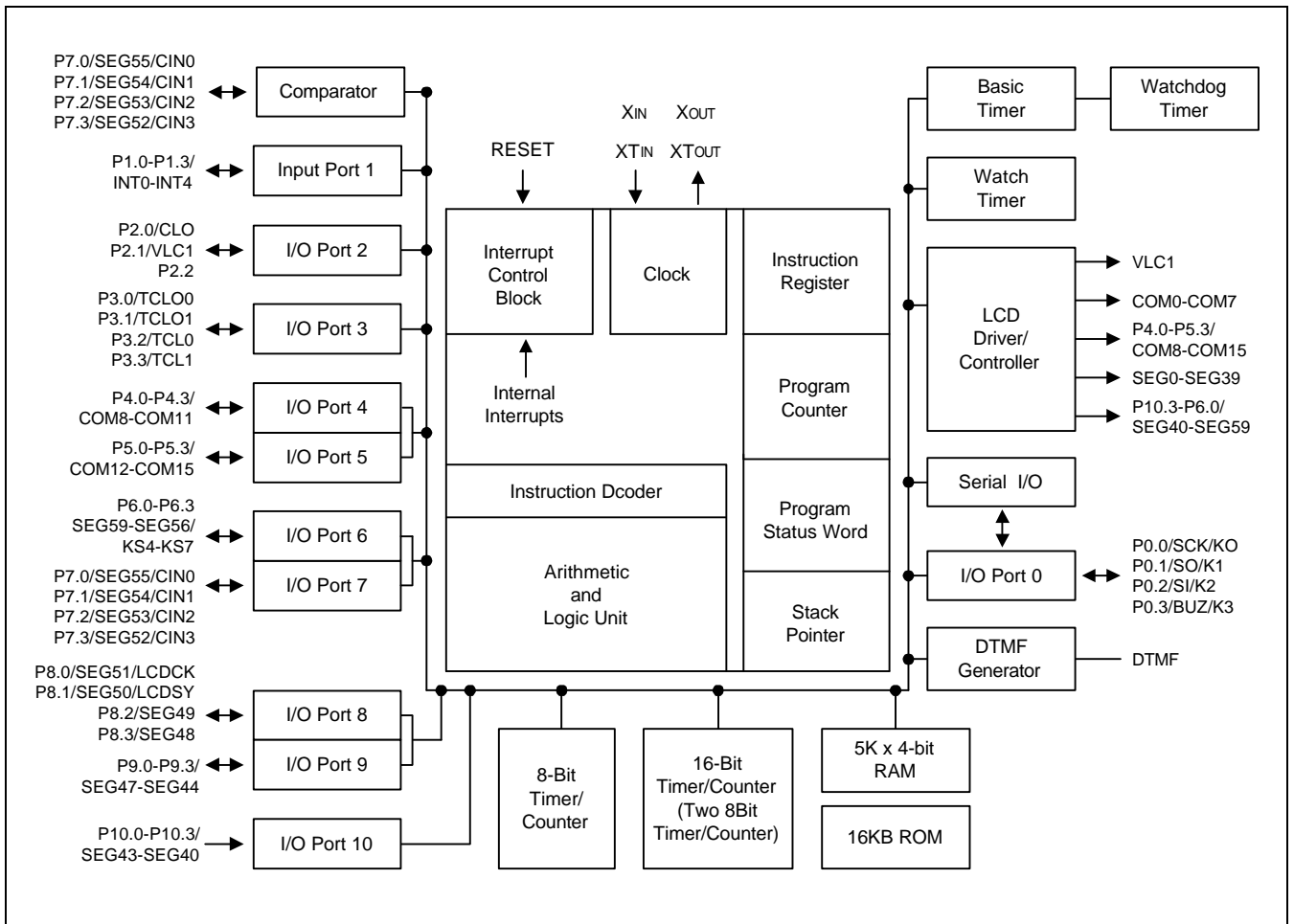
### Operating Voltage Range

- 1.8 V to 5.5 V (except DTMF and Comparator)
- 2 V to 5.5 V (include DTMF)
- 4.0 V to 5.5 V (include Comparator)

### Package Type

- 100-pin QFP (1420C)

**BLOCK DIAGRAM**



**Figure 1-1. S3C7565 Block Diagram**

PIN ASSIGNMENTS

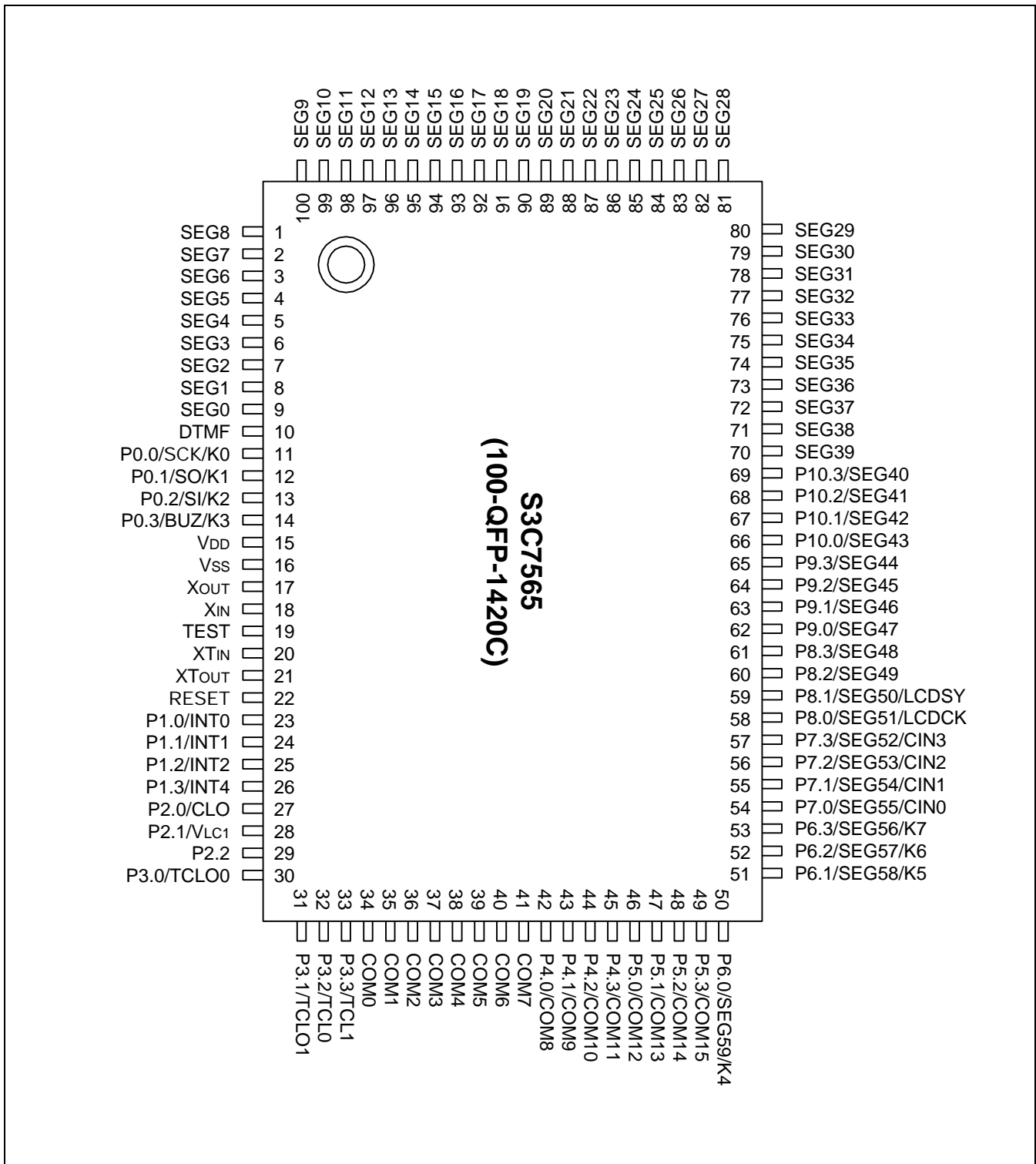


Figure 1-2. S3C7565 Pin Assignments (100-QFP Package)

## PIN DESCRIPTIONS

Table 1-1. S3C7565 Pin Descriptions

Pin Name	Pin Type	Description	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	SCK/K0 SO/K1 SI/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 4-bit pull-up resistors are software assignable.	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2	I/O	Same as port 0 except that port 2 is a 3-bit I/O port.	CLO V <sub>LC1</sub>
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	TCLO0 TCLO1 TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-bit or 8-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	COM8–COM11 COM12–COM15
P6.0–P6.3  P7.0–P7.3	I/O	Same as P4, P5.	SEG59– SEG56/K4–K7  SEG55/CIN0– SEG52/CIN3
P8.0–P8.1	I/O	Input ports. 1, 4-bit or 8-bit read and test is possible. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins. These pins can not be used as push-pull output. Refer to the NOTES of table 10-3. Port Mode Group Flags.	SEG51/LCDCK SEG50/LCDSY
P8.2–P8.3  P9.0–P9.3	I/O	Same as P4, P5.	SEG49 SEG48  SEG47–SEG44
P10.0–P10.3	I/O	Same as P4, P5.	SEG43–SEG40
SCK	I/O	Serial I/O interface clock signal.	P0.0/K0
SO	I/O	Serial data output.	P0.1/K1

Table 1-1. S3C7565 Pin Descriptions (Continued)

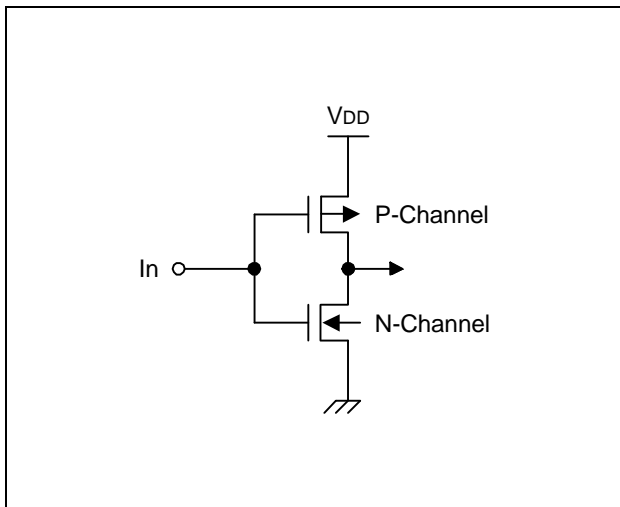
Pin Name	Pin Type	Description	Share Pin
SI	I/O	Serial data input.	P0.2/K2
BUZ	I/O	0.5, 1, 2, or 4 kHz frequency output for buzzer sound.	P0.3/K3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising or falling edges.	P1.2
INT4	I	External interrupt with a detection of rising and falling edge.	P1.3
CLO	I/O	Clock output .	P2.0
TCLO0	I/O	Timer/counter 0 clock output.	P3.0
TCLO1	I/O	Timer/counter 1 clock output.	P3.1
TCL0	I/O	External clock input for timer/counter 0.	P3.2
TCL1	I/O	External clock input for timer/counter 1.	P3.3
CIN0 CIN1 CIN2 CIN3	I/O	4-Channel comparator input CIN0–CIN2: comparator input only CIN3: comparator input or external reference input	P7.0/SEG55 P7.1/SEG54 P7.2/SEG53 P7.3/SEG52
DTMF	O	DTMF output	–
LCDCK	I/O	LCD clock output	P8.0/SEG51
LCDSY	I/O	LCD synchronization clock output.	P8.1/SEG50
COM0–COM7	O	LCD common signal output.	–
COM8–COM11	I/O		P4.0–P4.3
COM12–COM15			P5.0–P5.3
SEG0–SEG39	O	LCD segment signal output.	–
SEG40–SEG59	I/O		P10.3–P6.0
K0–K3	I/O	External interrupt (triggering edge is selectable)	P0.0–P0.3
K4–K7			P6.0–P6.3
V <sub>DD</sub>	–	Main power supply.	–
V <sub>SS</sub>	–	Ground.	–
RESET	I	Reset signal.	–
V <sub>LC1</sub>	–	LCD power supply.	P2.1
X <sub>IN</sub> , X <sub>OUT</sub>	–	Crystal, Ceramic or RC oscillator pins for system clock.	–
XT <sub>IN</sub> , XT <sub>OUT</sub>	–	Crystal oscillator pins for subsystem clock.	–
TEST	I	Chip test input pin. Hold GND when the device is operating.	–

**NOTE:** Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

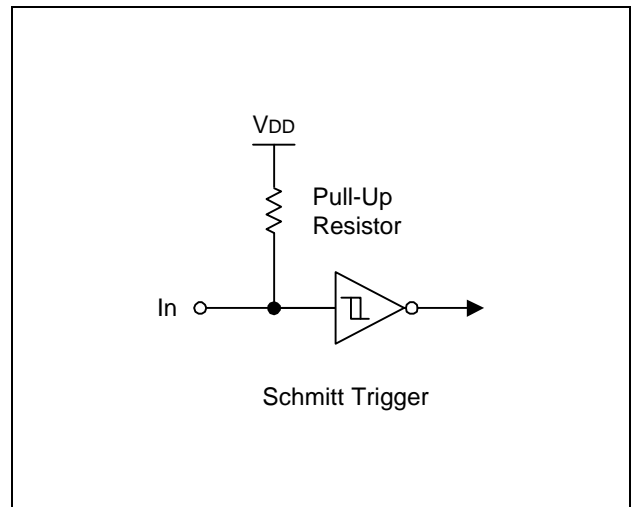
Table 1-2. Supplemental S3C7565 Pin Data

Pin Names	Share Pins	I/O Type	RESET Value	Circuit Type
P0.0–P0.3	SCK/K0, SO/K1, SI/K2, BUZ/K3	I/O	Input	E-4
P1.0–P1.3	INT0, INT1 and INT2, INT4	I	Input	A-4
P2.0	CLO	I/O	Input	E-4
P2.1	V <sub>LC1</sub>	I/O	Input	E-7
P2.2	–	I/O	Input	E-4
P3.0–P3.1	TCLO0, TCLO1	I/O	Input	E-2
P3.2–P3.3	TCL0, TCL1	I/O	Input	E-4
P4.0–P4.3 P5.0–P5.3	COM8–COM11 COM12–COM15	I/O	Input	H-24
P6.0–P6.3	SEG59/K4– SEG56/K7	I/O	Input	H-25
P7.0–P7.2	SEG55/CIN0– SEG53/CIN2	I/O	Input	H-26
P7.3	SEG52/CIN3	I/O	Input	H-27
P8.0–P8.1	SEG51–SEG50	I/O	Input	H-28
P8.2–P8.3	SEG49–SEG48	I/O	Input	H-24
P9.0–P9.3	SEG47–SEG44	I/O	Input	H-24
P10.0–P10.3	SEG43–SEG40	I/O	Input	H-24
COM0–COM7	–	O	High	H-3
SEG0–SEG39	–	O	High	H-3
DTMF	–	O	High impedance	G-7
V <sub>DD</sub>	–	–	–	–
V <sub>SS</sub>	–	–	–	–
RESET	–	I	–	B
V <sub>LC1</sub>	–	–	–	–
X <sub>IN</sub> , X <sub>OUT</sub>	–	–	–	–
XT <sub>IN</sub> , XT <sub>OUT</sub>	–	–	–	–
TEST	–	I	–	–

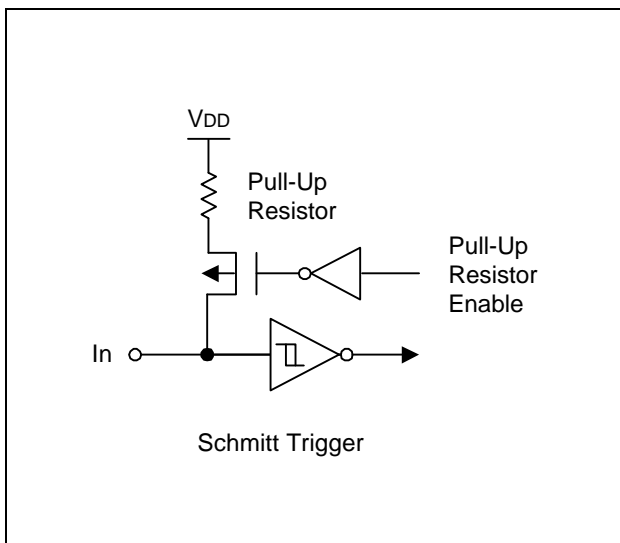
**PIN CIRCUIT DIAGRAMS**



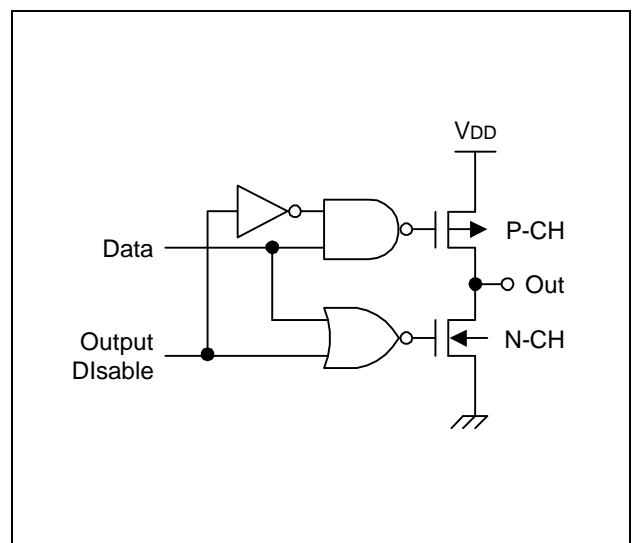
**Figure 1-3. Pin Circuit Type A**



**Figure 1-5. Pin Circuit Type B**



**Figure 1-4. Pin Circuit Type A-4**



**Figure 1-6. Pin Circuit Type C**



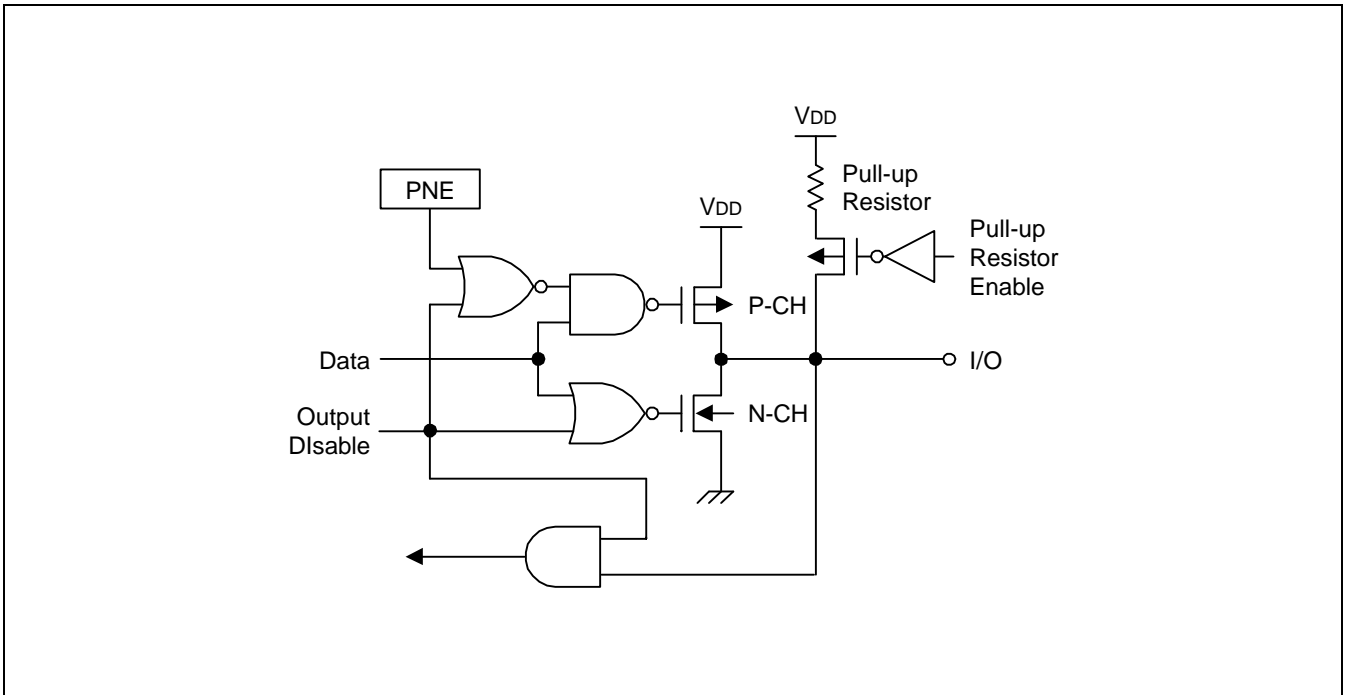


Figure 1-7. Pin Circuit Type E-2

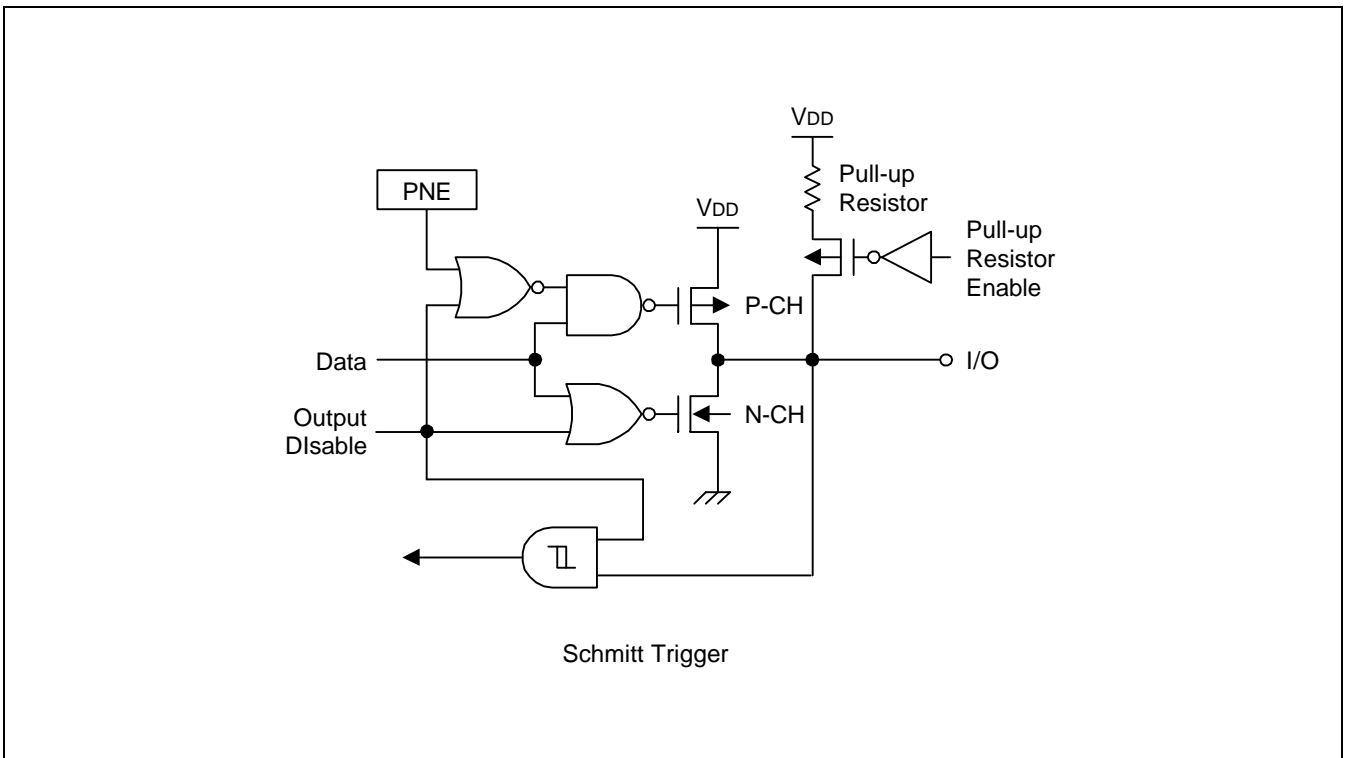


Figure 1-8. Pin Circuit Type E-4

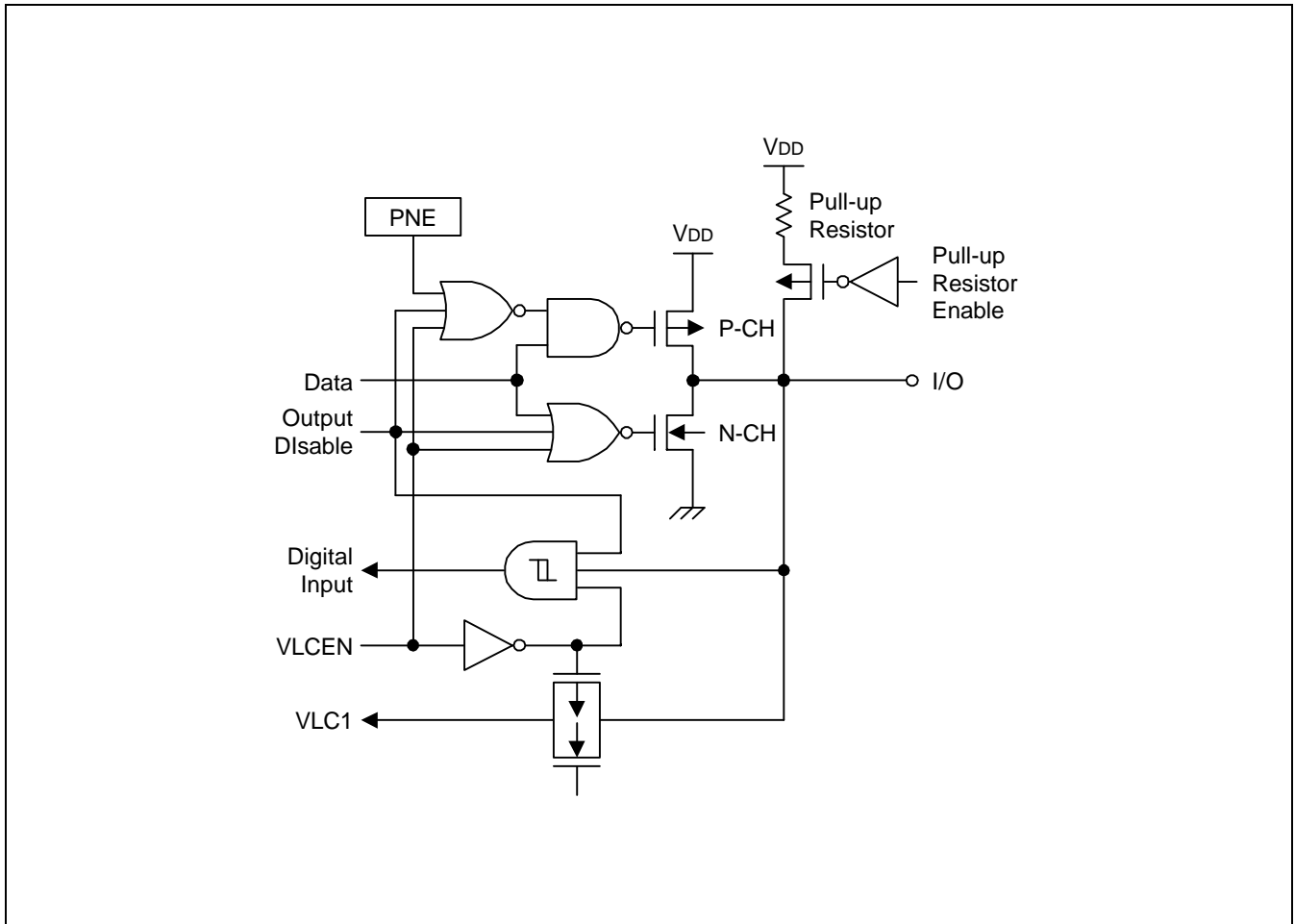


Figure 1-9. Pin Circuit Type E-7

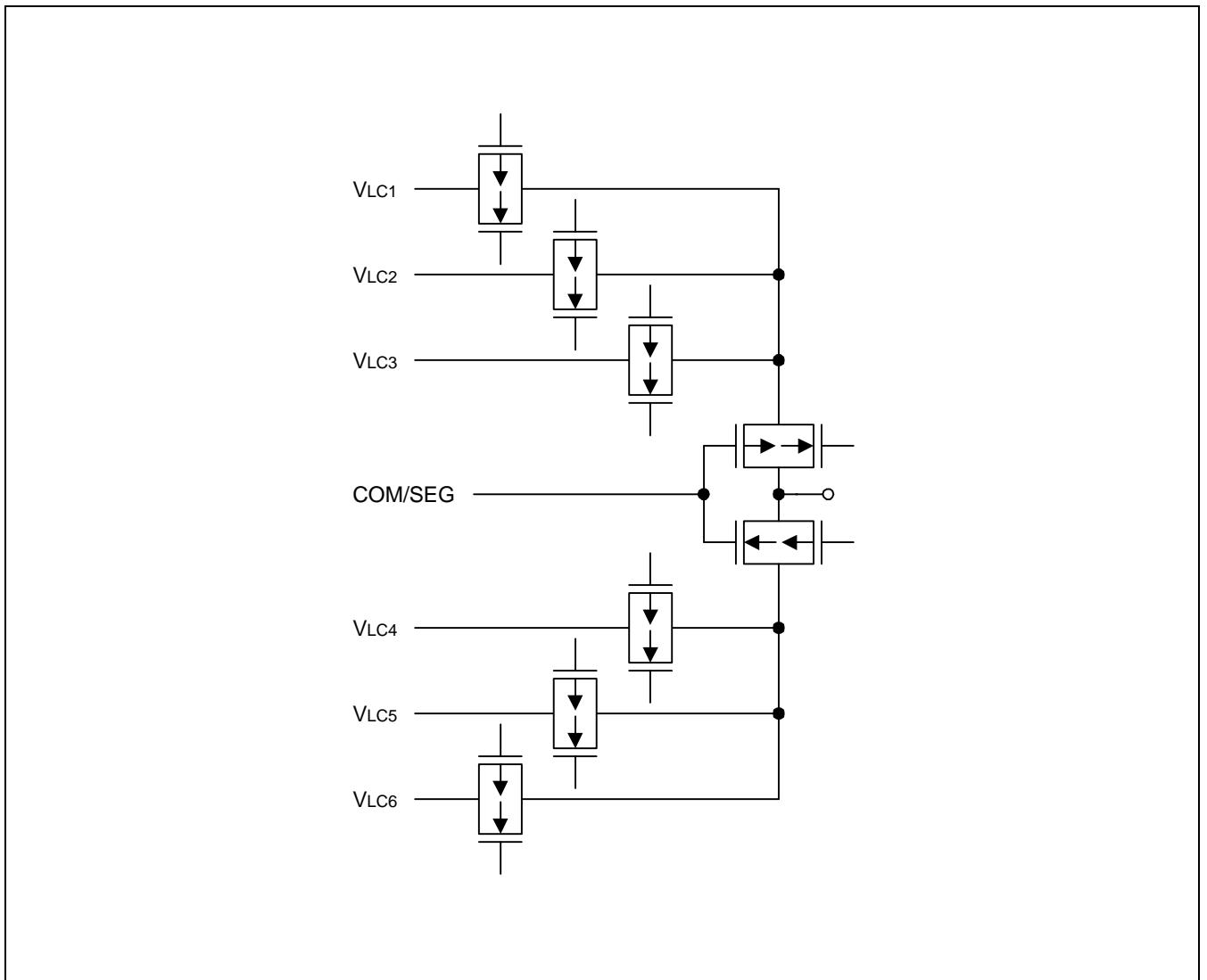


Figure 1-10. Pin Circuit Type H-3

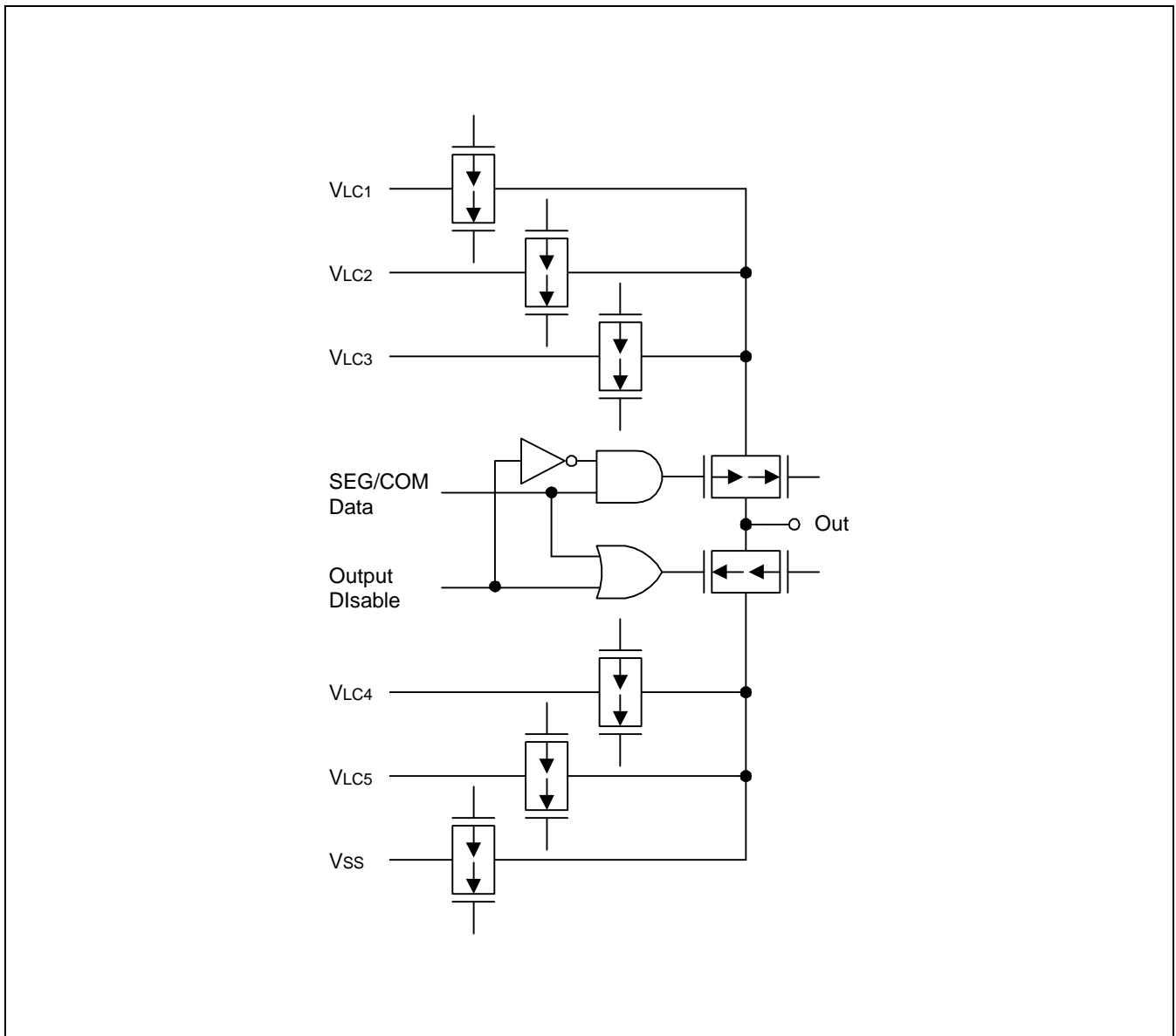


Figure 1-11. Pin Circuit Type H-23

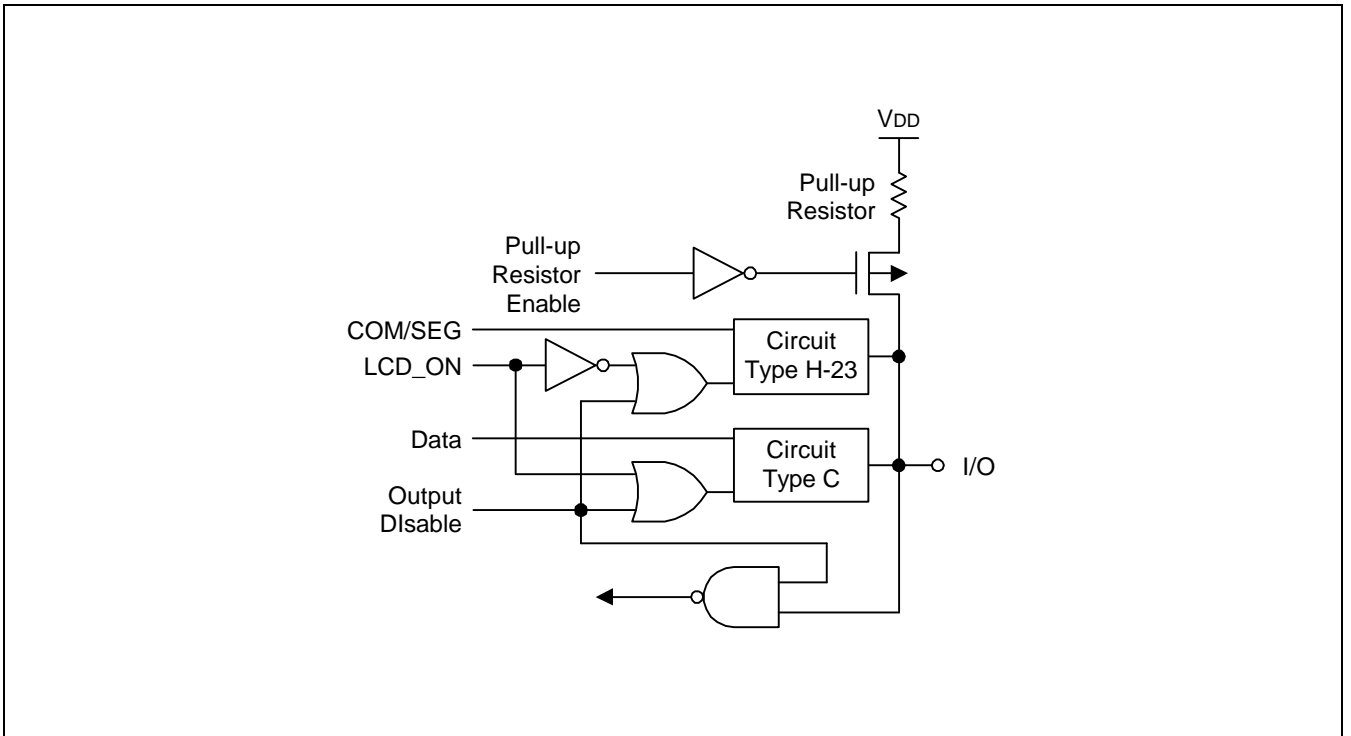


Figure 1-12. Pin Circuit Type H-24

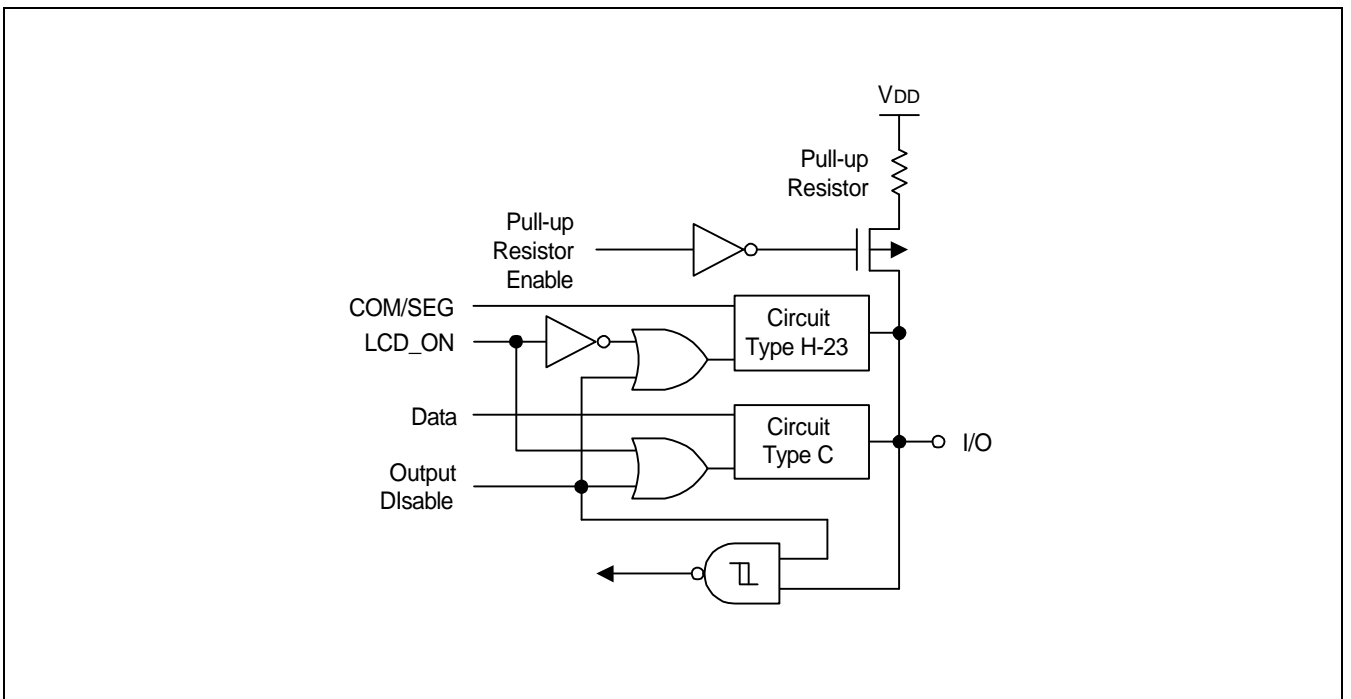


Figure 1-13. Pin Circuit Type H-25

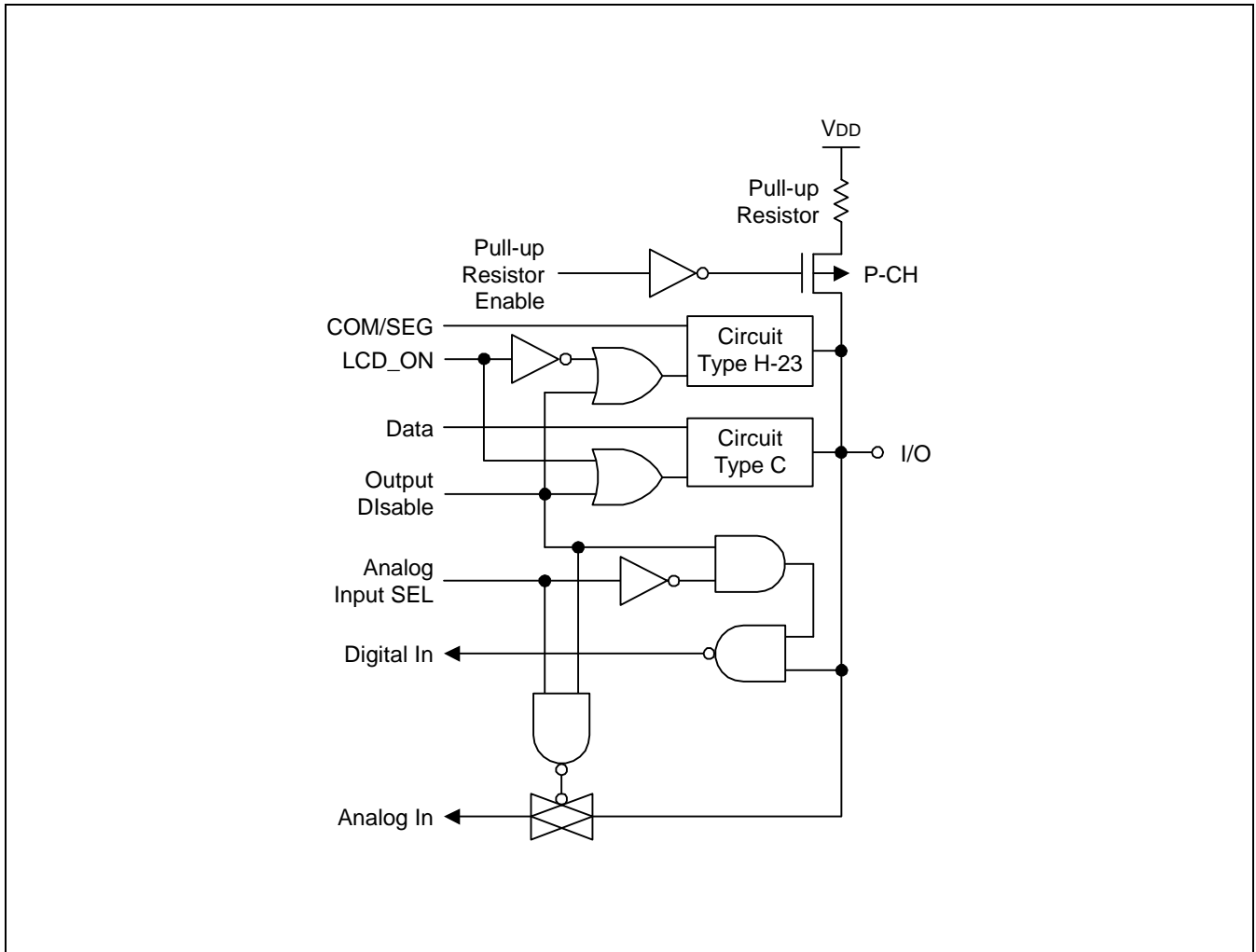


Figure 1-14. Pin Circuit Type H-26

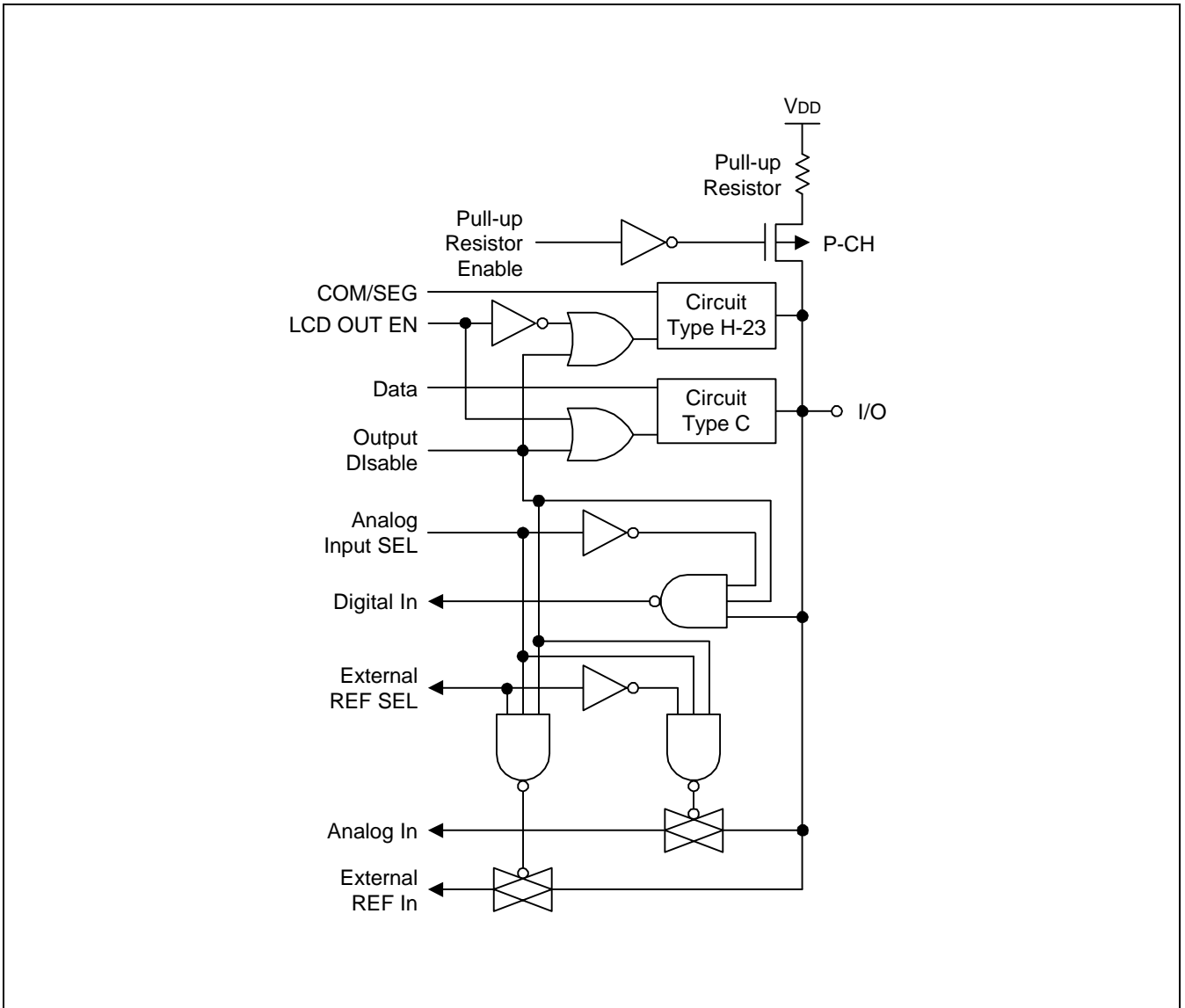


Figure 1-15. Pin Circuit Type H-27

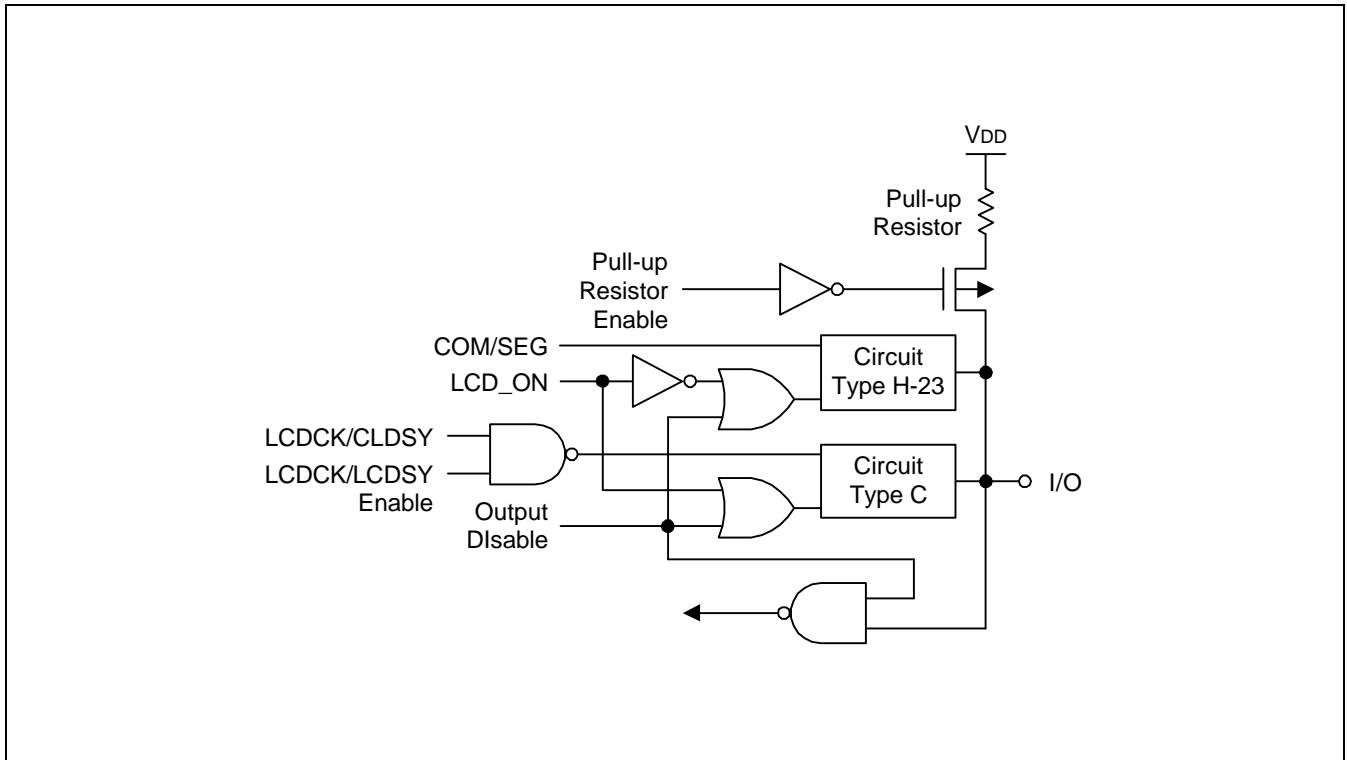


Figure 1-16. Pin Circuit Type H-28

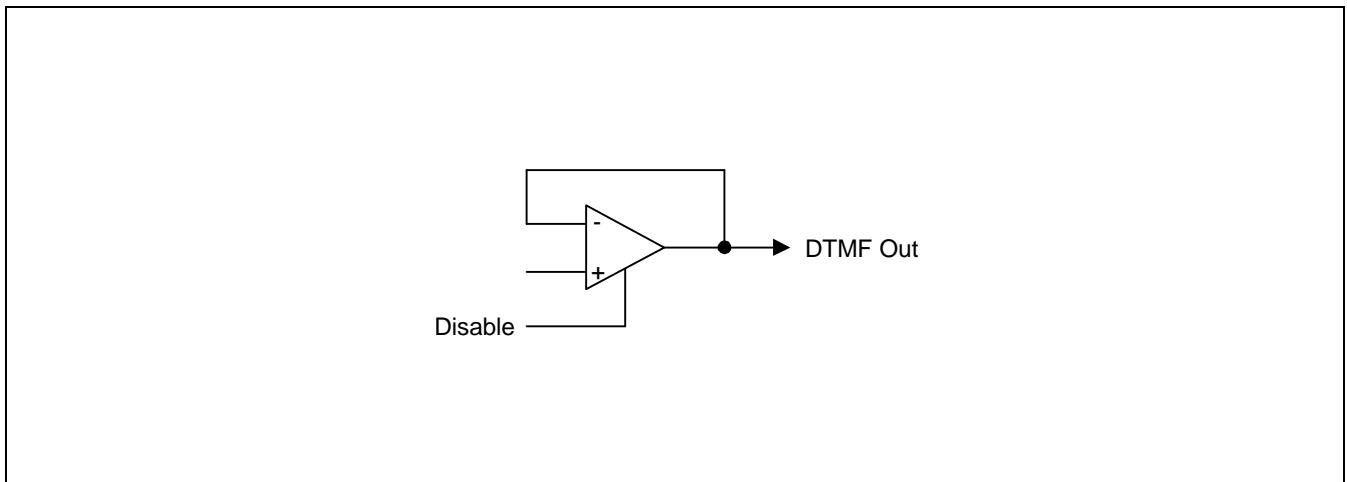


Figure 1-17. Pin Circuit Type G-7



# 16 ELECTRICAL DATA

## OVERVIEW

In this section, information on S3C7565 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

### Standard Electrical Characteristics

- Absolute maximum ratings
- D.C. electrical characteristics
- Main system clock oscillator characteristics
- Subsystem clock oscillator characteristics
- I/O capacitance
- A.C. electrical characteristics
- Operating voltage range

### Stop Mode Characteristics and Timing Waveforms

- RAM data retention supply voltage in stop mode
- Stop mode release timing when initiated by RESET
- Stop mode release timing when initiated by an interrupt request

### Miscellaneous Timing Waveforms

- A.C timing measurement point
- Clock timing measurement at  $X_{IN}$
- Clock timing measurement at  $XT_{IN}$
- TCL timing
- Input timing for RESET
- Input timing for external interrupts
- Serial data transfer timing

Table 16-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input Voltage	$V_I$	Ports 0–10	– 0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_O$	–	– 0.3 to $V_{DD} + 0.3$	V
Output Current High	$I_{OH}$	One I/O pin active	– 15	mA
		All I/O pins active	– 35	
Output Current Low	$I_{OL}$	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 (note)	
		Total for ports 0, 2–10	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	$T_A$	–	– 40 to + 85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	–	– 65 to + 150	$^\circ\text{C}$

**NOTE:** The values for Output Current Low ( $I_{OL}$ ) are calculated as Peak Value  $\times \sqrt{\text{Duty}}$  .

Table 16-2. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  to  $5.5\text{ V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	$V_{IH1}$	All input pins except those specified below for $V_{IH2}$ – $V_{IH3}$	$0.7 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	Ports 0, 1, 2, 6, P3.2, P3.3, and RESET	$0.8 V_{DD}$		$V_{DD}$	
	$V_{IH3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$	$V_{DD} - 0.1$		$V_{DD}$	
Input Low Voltage	$V_{IL1}$	All input pins except those specified below for $V_{IL2}$ – $V_{IL3}$	–	–	$0.3V_{DD}$	V
	$V_{IL2}$	Ports 0, 1, 2, 6, P3.2, P3.3, and RESET			$0.2V_{DD}$	
	$V_{IL3}$	$X_{IN}$ , $X_{OUT}$ , and $XT_{IN}$			0.1	
Output High Voltage	$V_{OH}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OH} = -1\text{ mA}$ Ports 0, 2–10	$V_{DD} - 1.0$	–	–	V
Output Low Voltage	$V_{OL}$	$V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ $I_{OL} = 15\text{ mA}$ Ports 0, 2–10	–	–	2.0	V

Table 16-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I <sub>LIH1</sub>	V <sub>I</sub> = V <sub>DD</sub> All input pins except those specified below for I <sub>LIH2</sub>	–	–	3	μA
	I <sub>LIH2</sub>	V <sub>I</sub> = V <sub>DD</sub> X <sub>IN</sub> , XT <sub>IN</sub>			20	
Input Low Leakage Current	I <sub>LIL1</sub>	V <sub>I</sub> = 0 V All input pins except RESET, X <sub>IN</sub> , XT <sub>IN</sub>	–	–	–3	μA
	I <sub>LIL2</sub>	V <sub>I</sub> = 0 V X <sub>IN</sub> , XT <sub>IN</sub>			–20	
Output High Leakage Current	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub> All output pins	–	–	3	μA
Output Low Leakage Current	I <sub>LOL</sub>	V <sub>O</sub> = 0 V All output pins	–	–	–3	μA
Pull-Up Resistor	R <sub>LI</sub>	V <sub>I</sub> = 0 V; V <sub>DD</sub> = 5 V, Port 0–10	25	47	100	kΩ
		V <sub>DD</sub> = 3 V	50	95	200	
	R <sub>L2</sub>	V <sub>I</sub> = 0 V; V <sub>DD</sub> = 5 V, RESET	100	220	400	
		V <sub>DD</sub> = 3 V	200	450	800	
LCD Voltage Dividing Resistor (Note)	R <sub>LCD1</sub>	–	40	55	70	kΩ
	R <sub>LCD2</sub>		20	28	35	
V <sub>DD-COMi</sub>   Voltage Drop (i = 0–15)	V <sub>DC</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V – 15 μA per common pin	–	–	120	mV
V <sub>DD-SEGx</sub>   Voltage Drop (x = 0–59)	V <sub>DS</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V – 15 μA per segment pin	–	–	120	
V <sub>LCX</sub> Output Voltage	V <sub>LC1</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V LCD clock = 0 Hz	V <sub>DD</sub> –0.2	V <sub>DD</sub>	V <sub>DD</sub> + 0.2	V
	V <sub>LC2</sub>		0.8V <sub>DD</sub> –0.2	0.8V <sub>DD</sub>	0.8V <sub>DD</sub> + 0.2	
	V <sub>LC3</sub>		0.6V <sub>DD</sub> –0.2	0.6V <sub>DD</sub>	0.6V <sub>DD</sub> + 0.2	
	V <sub>LC4</sub>		0.4V <sub>DD</sub> –0.2	0.4V <sub>DD</sub>	0.4V <sub>DD</sub> + 0.2	
	V <sub>LC5</sub>		0.2V <sub>DD</sub> –0.2	0.2V <sub>DD</sub>	0.2V <sub>DD</sub> + 0.2	

**NOTE:** R<sub>LCD1</sub> is the LCD Voltage dividing resistor when LCON.1 = "0", and R<sub>LCD2</sub> when LCON.1 = "1".

Table 16-2. D.C. Electrical Characteristics (Concluded)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

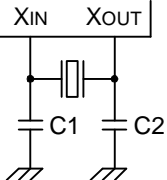
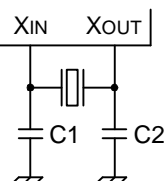
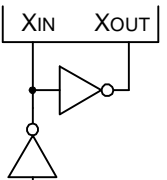
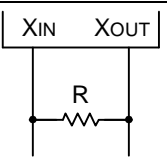
Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply Current (1)	I <sub>DD1</sub> (DTMF on)	Run mode; V <sub>DD</sub> = 5 V ± 10 % 3.58 MHz X-tal oscillator, C1 = C2 = 22 pF	–	3.9	7.0	mA	
		V <sub>DD</sub> = 3 V ± 10 %	–	2.0	4.0		
	I <sub>DD2</sub> (DTMF off)	Run mode; V <sub>DD</sub> = 5 V ± 10% Crystal oscillator C1 = C2 = 22pF	6.0 MHz 3.58 MHz	–	4.1 2.7	8.0 5.0	
		V <sub>DD</sub> = 3 V ± 10%	6.0 MHz 3.58 MHz		1.9 1.2	4.0 2.3	
	I <sub>DD3</sub>	Idle mode; V <sub>DD</sub> = 5 V ± 10 % Crystal oscillator C1 = C2 = 22pF	6.0 MHz 3.58 MHz	–	1.2 0.9	2.5 1.8	
		V <sub>DD</sub> = 3 V ± 10 %	6.0 MHz 3.58 MHz		0.5 0.4	1.5 1.0	
	I <sub>DD4</sub> (2)	Run mode; V <sub>DD</sub> = 3 V ± 10 % 32 kHz Crystal oscillator		–	17.5	45	μA
	I <sub>DD5</sub> (2)	Idle mode; V <sub>DD</sub> = 3 V ± 10 % 32 kHz Crystal oscillator		–	4.8	15	μA
I <sub>DD6</sub>	Stop mode; V <sub>DD</sub> = 5 V ± 10 % V <sub>DD</sub> = 3 V ± 10 %	SCMOD = 0000 XT <sub>IN</sub> = 0 V	–	2.0 0.6	5 3	μA	
	Stop mode; V <sub>DD</sub> = 5 V ± 10 % V <sub>DD</sub> = 3 V ± 10 %	SCMOD = 0100		0.2 0.1	3 2		
Row Tone level	V <sub>ROW</sub>	V <sub>DD</sub> = 2 to 5.5 V RL = 12 KΩ; Temp = -30 to 60 °C	-16.0	-14.0	-11.0	dBV	
Ratio of Column to Row tone	dBCR	V <sub>DD</sub> = 2 to 5.5 V RL = 12 KΩ; Temp = -30 to 60 °C	1	2	3		
Distortion (Dual tone)	THD	V <sub>DD</sub> = 2 to 5.5 V 1 MHz band RL = 12 KΩ; Temp = -30 to 60 °C	–	–	5	%	

**NOTES:**

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, the main system clock oscillation stops and the subsystem clock is used.
3. Currents in the following circuits are not included: on-chip pull-up resistors, internal LCD voltage dividing resistors, and output port drive currents.

Table 16-3. Main System Oscillator Characteristics

 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$ 

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3	
		Stabilization time <sup>(2)</sup>	Stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range; $V_{DD} = 3.0\text{ V}$	–	–	4	ms
Crystal Oscillator		Oscillation frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3	
		Stabilization time <sup>(2)</sup>	$V_{DD} = 3\text{ V}$	–	–	10	ms
$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	–		–	30			
External Clock		$X_{IN}$ input frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3	
		$X_{IN}$ input high and low level width ( $t_{XH}$ , $t_{XL}$ )	–	83.3	–	1,250	ns
RC Oscillator		Frequency	$R = 25\text{ k}\Omega, V_{DD} = 5\text{ V}$	–	2	–	MHz
			$R = 40\text{ k}\Omega, V_{DD} = 3\text{ V}$	–	1	–	

**NOTES:**

- Oscillation frequency and  $X_{IN}$  input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-4. Recommended Oscillator Constants

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C})$ 

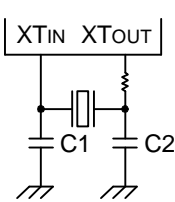
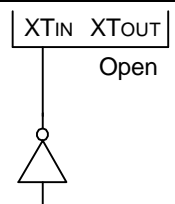
Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR 328M5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR 328MC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR 328MC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

**NOTES:**

1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 16-5. Subsystem Clock Oscillator Characteristics

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$ 

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	32	32.768	35	kHz
		Stabilization time (2)	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	–	1.0	2	s
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	–	–	10	
External Clock		$XT_{IN}$ input frequency (1)	$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	32	–	100	kHz
		$XT_{IN}$ input high and low level width ( $t_{XTL}$ , $t_{XTH}$ )	–	5	–	15	$\mu\text{s}$

**NOTES:**

1. Oscillation frequency and  $XT_{IN}$  input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 16-6. Input/output Capacitance

 $(T_A = 25\text{ }^\circ\text{C}, V_{DD} = 0\text{ V})$ 

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	$C_{IN}$	f = 1 MHz; Unmeasured pins are returned to $V_{SS}$	–	–	15	pF
Output Capacitance	$C_{OUT}$		–	–	15	pF
I/O Capacitance	$C_{IO}$		–	–	15	pF

Table 16-7. Comparator Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 4.0\text{ V to } 5.5\text{ V}, V_{SS} = 0\text{ V})$ 

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	–	–	0	–	$V_{DD}$	V
Reference Voltage Range	$V_{REF}$	–	0	–	$V_{DD}$	V
Input Voltage Accuracy	$V_{CIN}$	–	–	–	$\pm 150$	mV
Input Leakage Current	$I_{CIN}, I_{REF}$	–	–3	–	3	$\mu\text{A}$

Table 16-8. A.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t <sub>CY</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.67	–	64	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.33		64	
TCL0, TCL1 Input Frequency	f <sub>TI0</sub> , f <sub>TI1</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0	–	1.5	MHz
		V <sub>DD</sub> = 1.8 V to 5.5 V			1	
TCL0, TCL1 Input High, Low Width	t <sub>TIH0</sub> , t <sub>TIL0</sub> t <sub>TIH1</sub> , t <sub>TIL1</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V	0.48	–	–	μs
		V <sub>DD</sub> = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t <sub>KCY</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V <sub>DD</sub> = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source; Output	3800			



Table 16-8. A.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCK High, Low Width	t <sub>KH</sub> , t <sub>KL</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V External SCK source	325	–	–	ns
		Internal SCK source	T <sub>KCY</sub> / 2–50			
		V <sub>DD</sub> = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	t <sub>KCY</sub> / 2–150			
SI Setup Time to SCK High	t <sub>SIK</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V; Input	100	–	–	ns
		V <sub>DD</sub> = 2.7 V to 5.5 V; Output	150			
		V <sub>DD</sub> = 1.8 V to 5.5 V; Input	150			
		V <sub>DD</sub> = 1.8 V to 5.5 V; Output	500			
SI Hold Time to SCK High	t <sub>KSI</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V; Input	400	–	–	ns
		V <sub>DD</sub> = 2.7 V to 5.5 V; Output	400			
		V <sub>DD</sub> = 1.8 V to 5.5 V; Input	600			
		V <sub>DD</sub> = 1.8 V to 5.5 V; Output	500			
Output Delay for SCK to SO	t <sub>KSO</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V; Input	–	–	300	ns
		V <sub>DD</sub> = 2.7 V to 5.5 V; Output			250	
		V <sub>DD</sub> = 1.8 V to 5.5 V; Input			1000	
		V <sub>DD</sub> = 2.7 V to 5.5 V; Output			1000	
Interrupt Input High, Low Width	t <sub>INTH</sub> , t <sub>INTL</sub>	INT0–INT2, INT4, KS0–KS7	10	–	–	μs
RESET Input Low Width	t <sub>RSL</sub>	Input	10	–	–	μs

**NOTE:** Unless specified the otherwise, Instruction Cycle Time condition values assume a main system clock (fx) source.

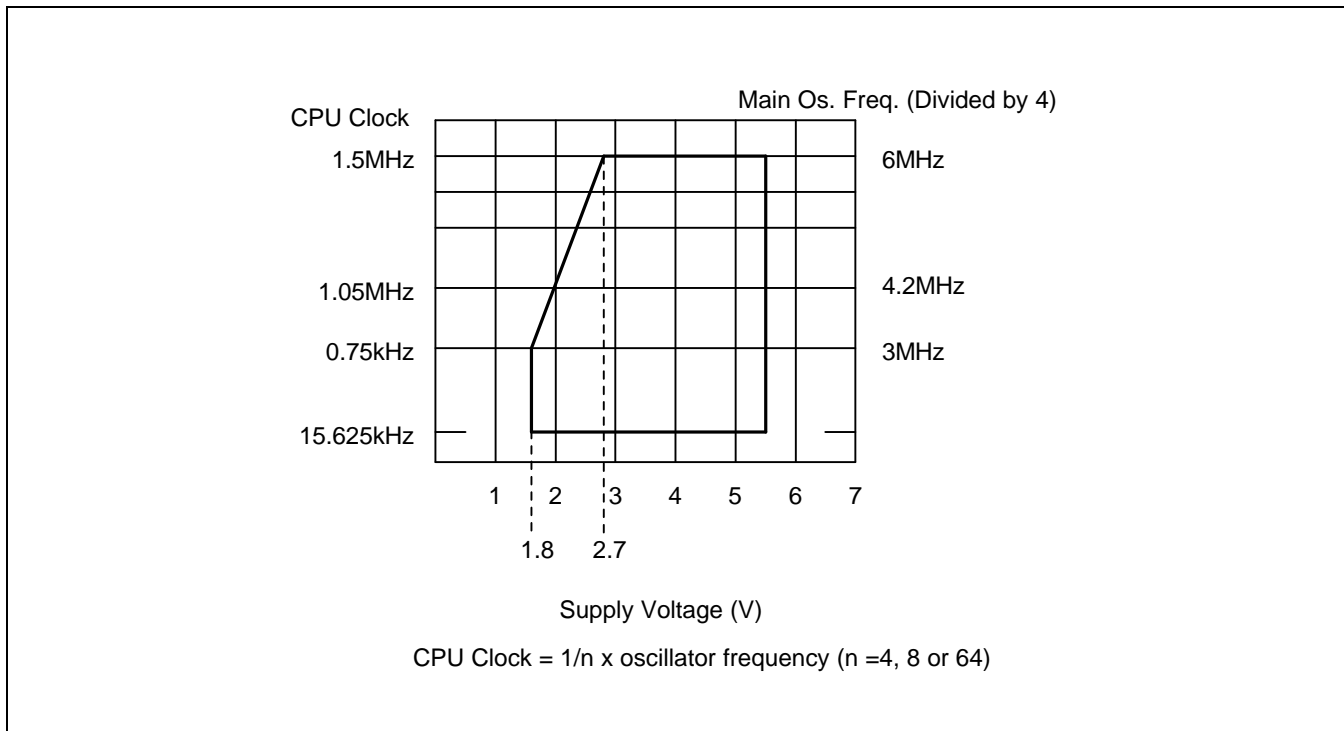


Figure 16-1. Standard Operating Voltage Range

Table 16-9. RAM Data Retention Supply Voltage in Stop Mode

(T<sub>A</sub> = -40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDDR</sub>	–	1.8	–	5.5	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.8 V	–	0.1	10	μA
Release signal set time	t <sub>SREL</sub>	–	0	–	–	μs
Oscillator stabilization wait time <sup>(1)</sup>	t <sub>WAIT</sub>	Released by RESET	–	2 <sup>17</sup> / fx	–	ms
		Released by interrupt	–	(2)	–	

**NOTES:**

- During the oscillator stabilization wait time, all the CPU operations must be stopped to avoid instability that can occur during the oscillator start-up.
- Use the basic timer mode register (BMOD) interval timer to delay an execution of CPU instructions during the wait time.

TIMING WAVEFORMS

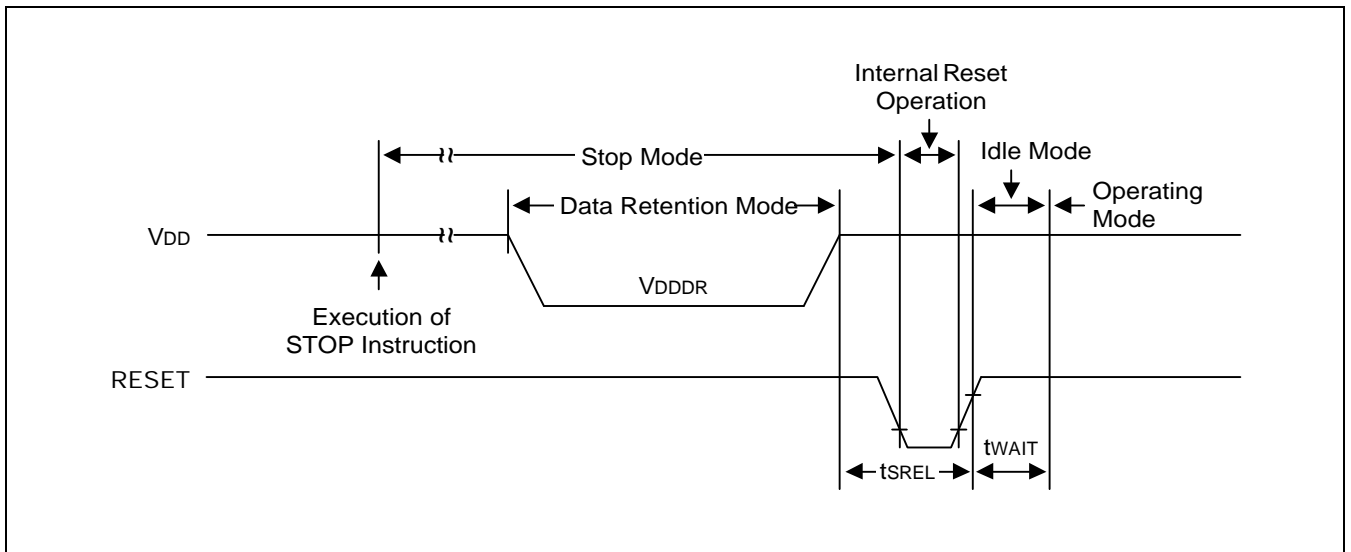


Figure 16-2. Stop Mode Release Timing When Initiated by RESET

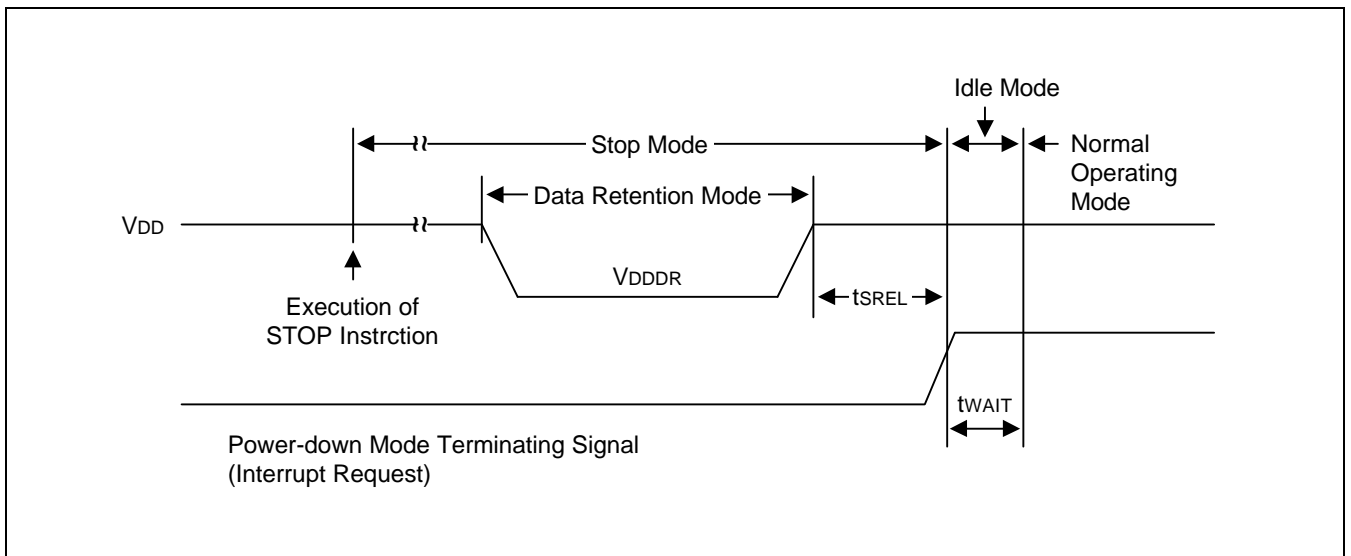


Figure 16-3. Stop Mode Release Timing When Initiated by Interrupt Request

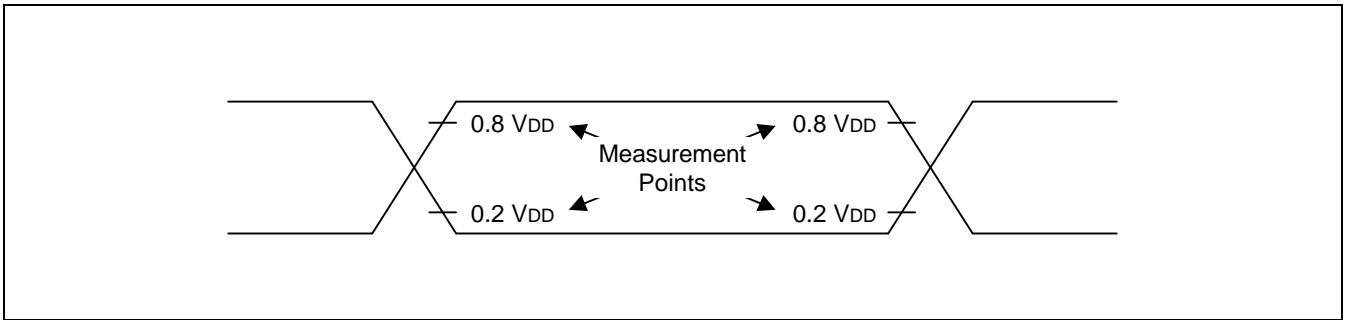


Figure 16-4. A.C. Timing Measurement Points (Except for  $X_{IN}$  and  $XT_{IN}$ )

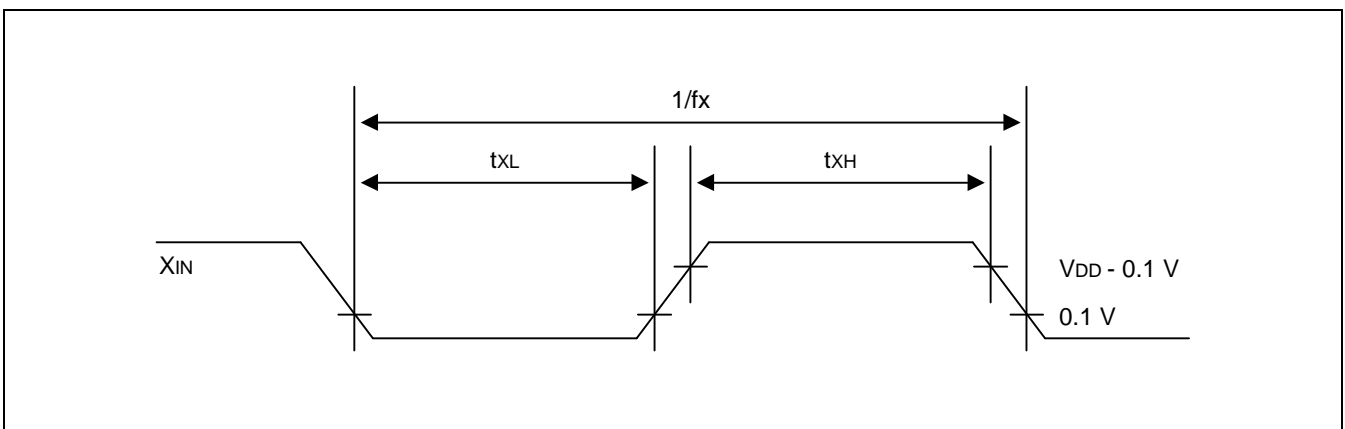


Figure 16-5. Clock Timing Measurement at  $X_{IN}$

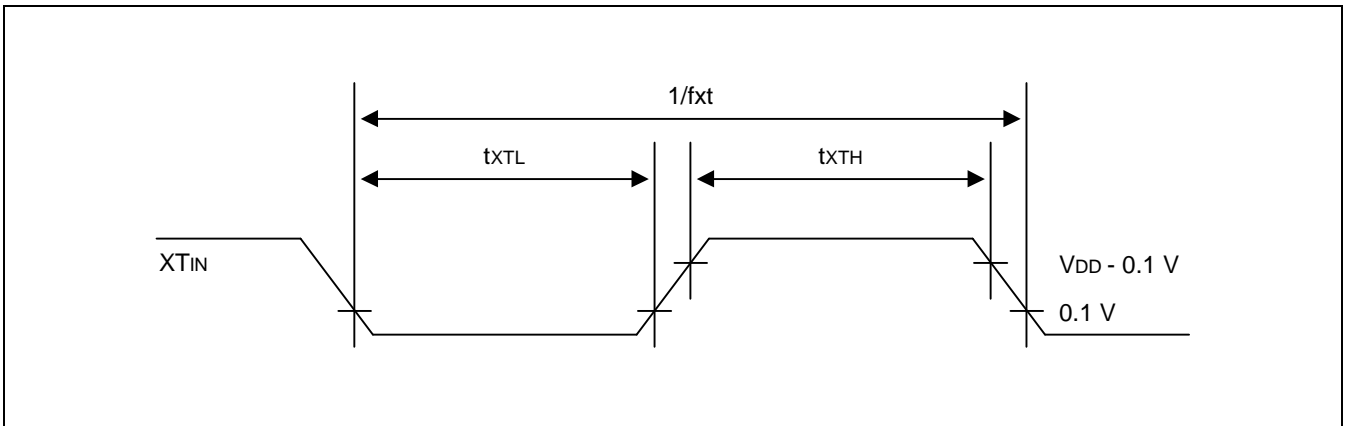


Figure 16-6. Clock Timing Measurement at  $XT_{IN}$

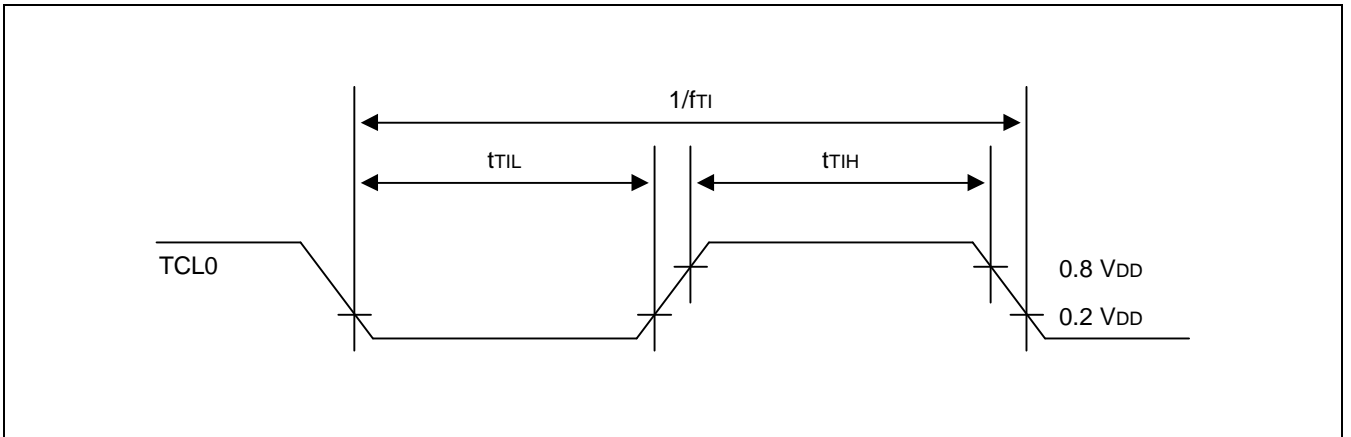


Figure 16-7. TCL Timing

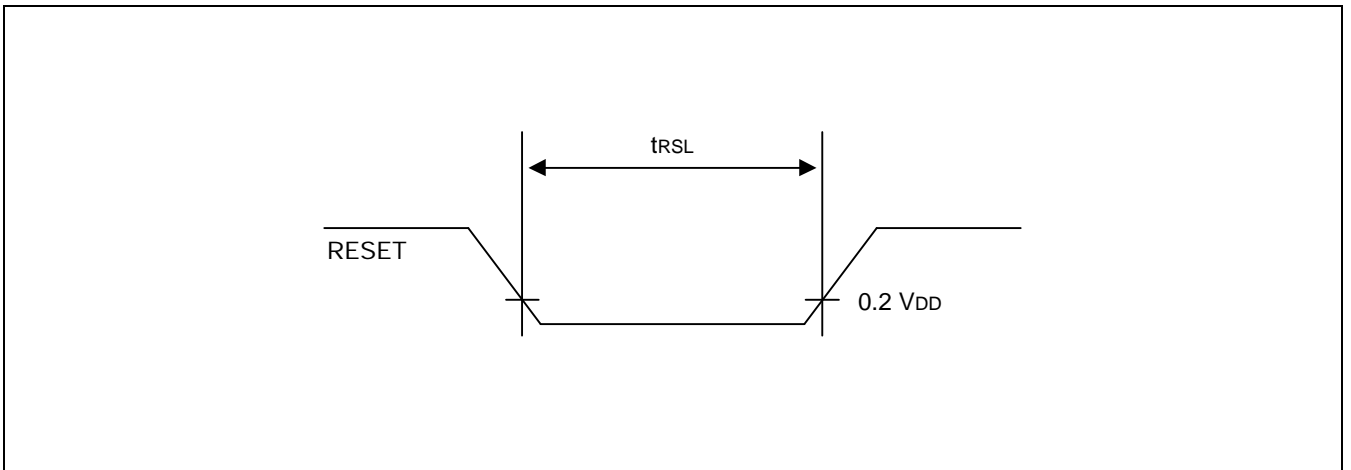


Figure 16-8. Input Timing for RESET Signal

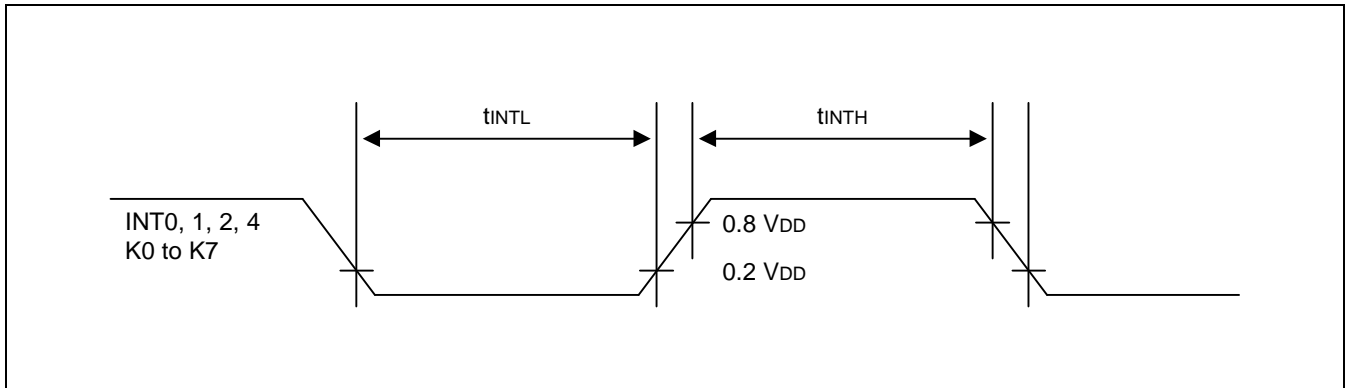


Figure 16-9. Input Timing for External Interrupts and Quasi-Interrupts

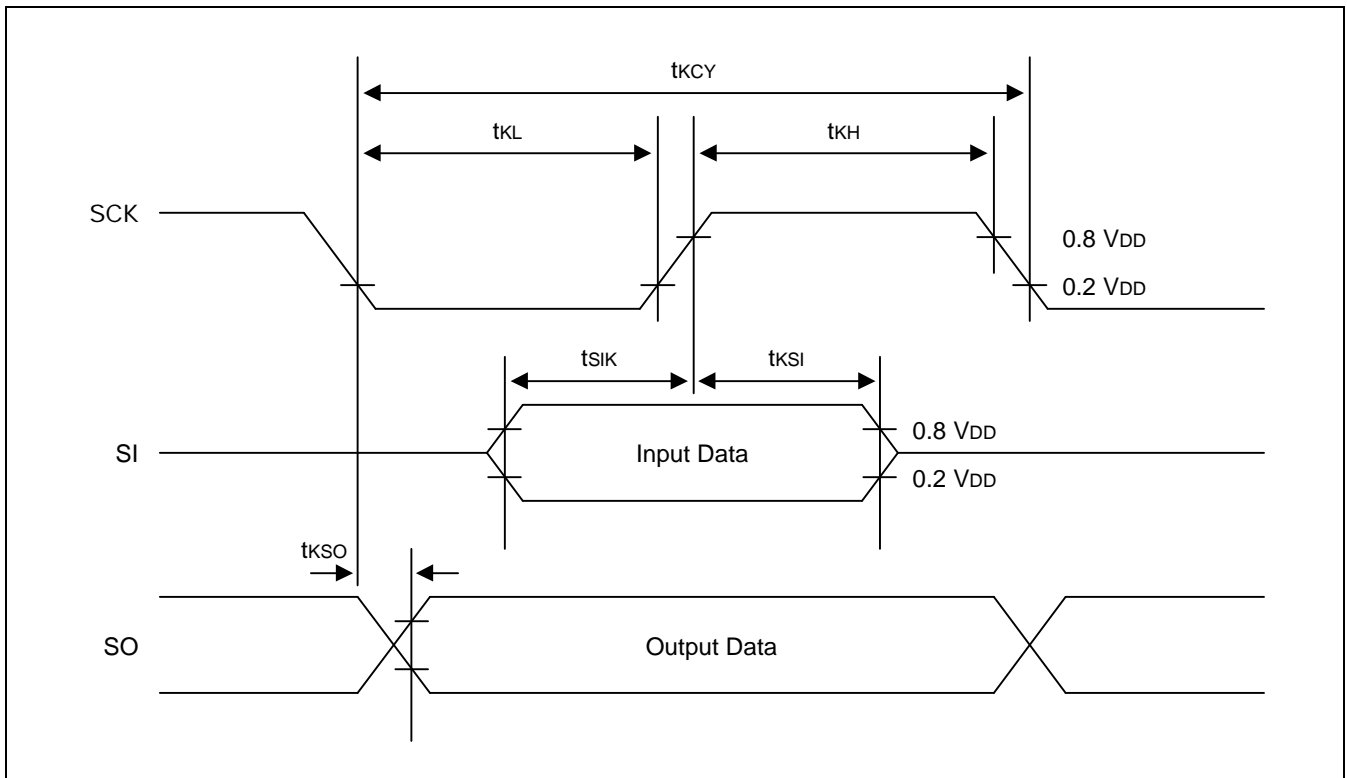


Figure 16-10. Serial Data Transfer Timing

# 17 MECHANICAL DATA

This section contains the following information about the device package:

- Package dimensions in millimeters
- Pad diagram
- Pad/pin coordinate data table

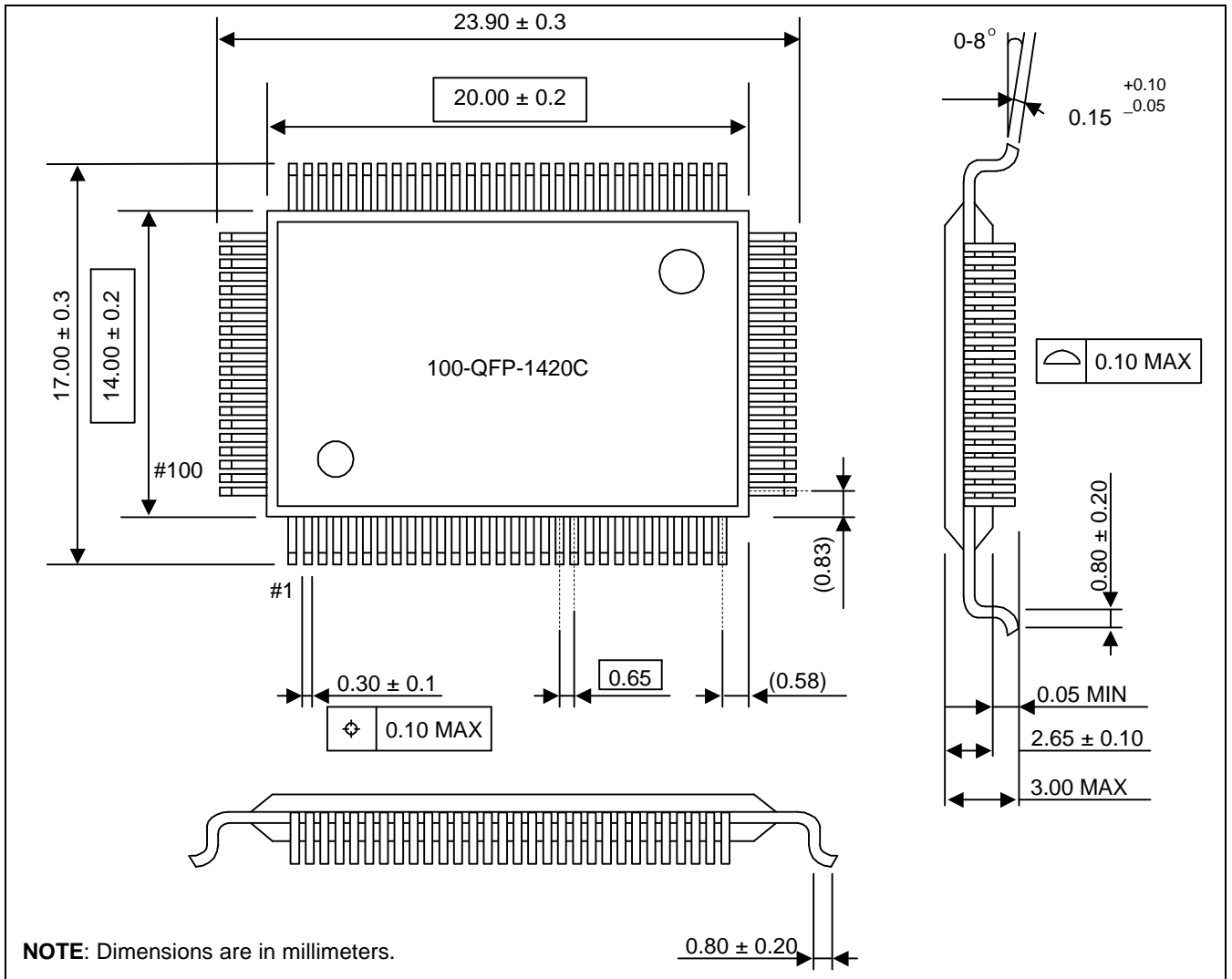


Figure 17-1. 100-QFP Package Dimensions



NOTES



# 18

## S3P7565 OTP

### OVERVIEW

The S3P7565 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C7565 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P7565 is fully compatible with the S3C7565, both in function and in pin configuration. Because of its simple programming requirements, the S3P7565 is ideal for use as an evaluation chip for the S3C7565.

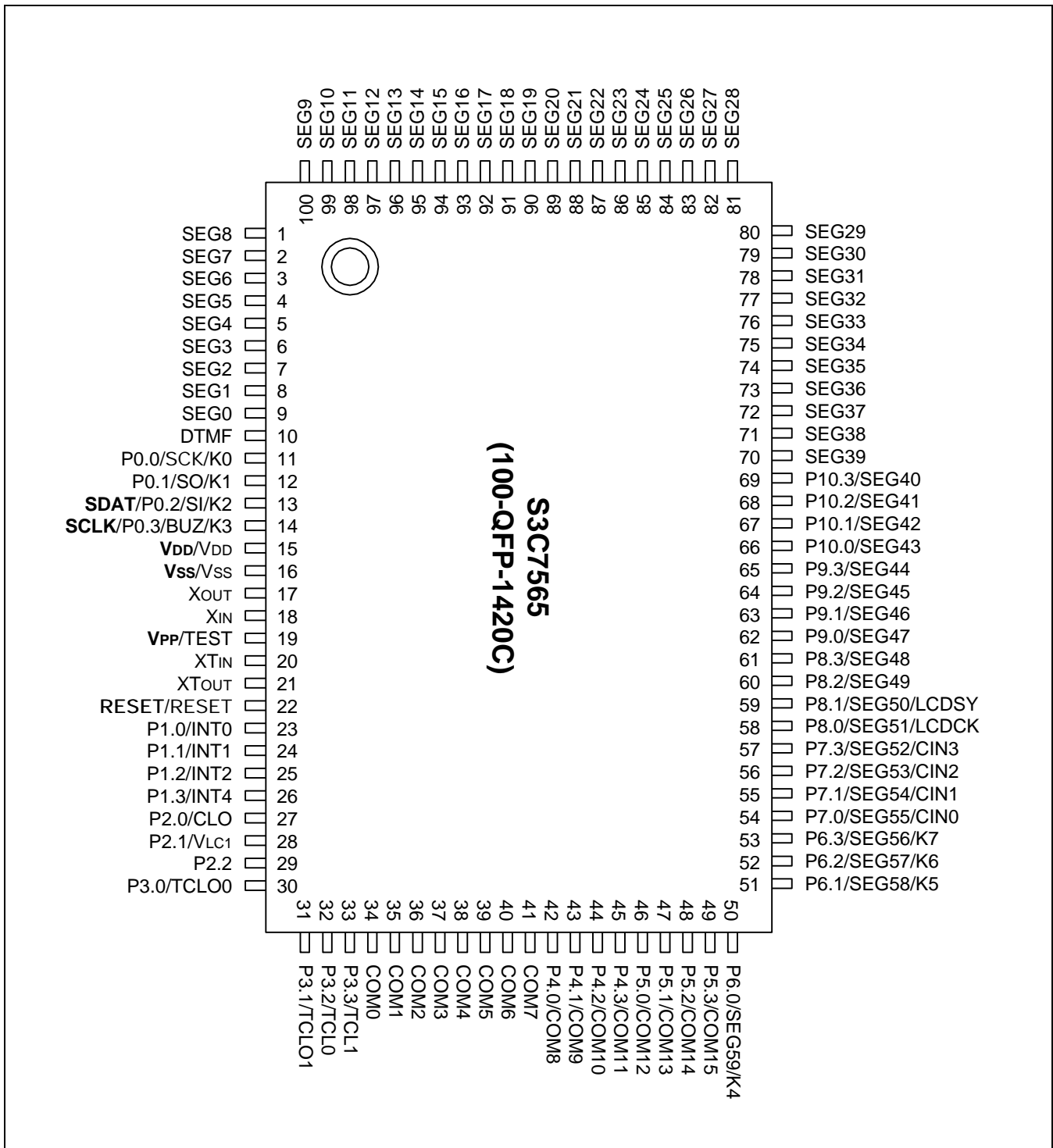


Figure 18-1. S3P7565 Pin Assignments (100-QFP Package)

Table 18-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P0.2	SDAT	13	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P0.3	SCLK	14	I/O	Serial clock pin. Input only pin.
TEST	V <sub>PP</sub> (TEST)	19	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. When OTP is operating, hold GND. (Option)
RESET	RESET	22	I	Chip initialization
V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> /V <sub>SS</sub>	15/16	I	Logic power supply pin. V <sub>DD</sub> should be tied to + 5 V during programming.

Table 18-2. Comparison of S3P7565 and S3C7565 Features

Characteristic	S3P7565	S3C7565
Program Memory	16-Kbyte EPROM	16-Kbyte mask ROM
Operating Voltage (V <sub>DD</sub> )	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5V	
Pin Configuration	100 QFP	100 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub> (TEST) pin of the S3P7565, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 18-3 below.

Table 18-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>PP</sub> (TEST)	REG/MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

**NOTE:** "0" means Low level; "1" means High level.

Table 18-4. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input Voltage	$V_I$	Ports 0–10	– 0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_O$	–	– 0.3 to $V_{DD} + 0.3$	V
Output Current High	$I_{OH}$	One I/O pin active	– 15	mA
		All I/O pins active	– 35	
Output Current Low	$I_{OL}$	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 (note)	
		Total for ports 0, 2–10	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	$T_A$	–	– 40 to + 85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	–	– 65 to + 150	$^\circ\text{C}$

**NOTE:** The values for Output Current Low ( $I_{OL}$ ) are calculated as Peak Value  $\times \sqrt{\text{Duty}}$  .

Table 18-5. D.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V <sub>IH1</sub>	All input pins except those specified below for V <sub>IH2</sub> -V <sub>IH3</sub>	0.7 V <sub>DD</sub>	-	V <sub>DD</sub>	V
	V <sub>IH2</sub>	Ports 0, 1, 2, 6, P3.2, P3.3, and RESET	0.8 V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH3</sub>	X <sub>IN</sub> , X <sub>OUT</sub> , and XT <sub>IN</sub>	V <sub>DD</sub> - 0.1		V <sub>DD</sub>	
Input Low Voltage	V <sub>IL1</sub>	All input pins except those specified below for V <sub>IL2</sub> -V <sub>IL3</sub>	-	-	0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	Ports 0, 1, 2, 6, P3.2, P3.3, and RESET			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	X <sub>IN</sub> , X <sub>OUT</sub> , and XT <sub>IN</sub>			0.1	
Output High Voltage	V <sub>OH</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OH</sub> = -1 mA Ports 0, 2-10	V <sub>DD</sub> - 1.0	-	-	V
Output Low Voltage	V <sub>OL</sub>	V <sub>DD</sub> = 4.5 V to 5.5 V I <sub>OL</sub> = 15 mA Ports 0, 2-10	-	-	2.0	V
Input High Leakage Current	I <sub>LIH1</sub>	V <sub>I</sub> = V <sub>DD</sub> All input pins except those specified below for I <sub>LIH2</sub>	-	-	3	μA
	I <sub>LIH2</sub>	V <sub>I</sub> = V <sub>DD</sub> X <sub>IN</sub> , XT <sub>IN</sub>			20	
Input Low Leakage Current	I <sub>LIL1</sub>	V <sub>I</sub> = 0 V All input pins except RESET, X <sub>IN</sub> , XT <sub>IN</sub>	-	-	-3	μA
	I <sub>LIL2</sub>	V <sub>I</sub> = 0 V X <sub>IN</sub> , XT <sub>IN</sub>			-20	
Output High Leakage Current	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub> All output pins	-	-	3	μA
Output Low Leakage Current	I <sub>LOL</sub>	V <sub>O</sub> = 0 V All output pins	-	-	-3	μA

Table 18-5. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pull-up Resistor	R <sub>LI</sub>	V <sub>I</sub> = 0 V; V <sub>DD</sub> = 5 V, Port 0-10	25	47	100	kΩ
		V <sub>DD</sub> = 3 V	50	95	200	
	R <sub>L2</sub>	V <sub>I</sub> = 0 V; V <sub>DD</sub> = 5 V, RESET	100	220	400	
		V <sub>DD</sub> = 3 V	200	450	800	
LCD Voltage Dividing Resistor (note)	R <sub>LCD1</sub>	–	40	55	70	kΩ
	R <sub>LCD2</sub>		20	28	35	
V <sub>DD</sub> -COM <sub>i</sub>   Voltage Drop (i = 0-15)	V <sub>DC</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V – 15 μA per common pin	–	–	120	mV
V <sub>DD</sub> -SEG <sub>x</sub>   Voltage Drop (x = 0-59)	V <sub>DS</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V – 15 μA per segment pin	–	–	120	
V <sub>LCX</sub> Output Voltage	V <sub>LC1</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V LCD clock = 0 Hz	V <sub>DD</sub> -0.2	V <sub>DD</sub>	V <sub>DD</sub> +0.2	V
	V <sub>LC2</sub>		0.8V <sub>DD</sub> -0.2	0.8V <sub>DD</sub>	0.8V <sub>DD</sub> +0.2	
	V <sub>LC3</sub>		0.6V <sub>DD</sub> -0.2	0.6V <sub>DD</sub>	0.6V <sub>DD</sub> +0.2	
	V <sub>LC4</sub>		0.4V <sub>DD</sub> -0.2	0.4V <sub>DD</sub>	0.4V <sub>DD</sub> +0.2	
	V <sub>LC5</sub>		0.2V <sub>DD</sub> -0.2	0.2V <sub>DD</sub>	0.2V <sub>DD</sub> +0.2	

**NOTE:** R<sub>LCD1</sub> is the LCD Voltage dividing resistor when LCON.1 = "0", and R<sub>LCD2</sub> is the one when LCON.1 = "1".

Table 18-5. D.C. Electrical Characteristics (Concluded)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

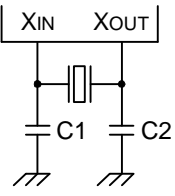
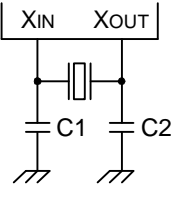
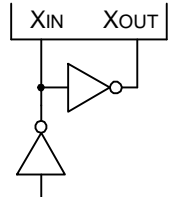
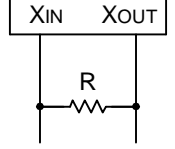
Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Supply Current <sup>(1)</sup>	I <sub>DD1</sub> (DTMF on)	Run mode; V <sub>DD</sub> = 5 V ± 10 % 3.58 MHz X-tal oscillator, C1 = C2 = 22 pF	–	3.9	7.0	mA	
		V <sub>DD</sub> = 3 V ± 10%	–	2.0	4.0		
	I <sub>DD2</sub> (DTMF off)	Run mode; V <sub>DD</sub> = 5 V ± 10 % Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 3.58 MHz		4.1 2.7	8.0 5.0	
		V <sub>DD</sub> = 3 V ± 10 %	6.0 MHz 3.58 MHz		1.9 1.2	4.0 2.3	
	I <sub>DD3</sub>	Idle mode; V <sub>DD</sub> = 5 V ± 10 % Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 3.58 MHz	–	1.2 0.9	2.5 1.8	
		V <sub>DD</sub> = 3 V ± 10 %	6.0 MHz 3.58 MHz		0.5 0.4	1.5 1.0	
	I <sub>DD4</sub> <sup>(2)</sup>	Run mode; V <sub>DD</sub> = 3 V ± 10 % 32 kHz Crystal oscillator		–	17.5	45	μA
	I <sub>DD5</sub> <sup>(2)</sup>	Idle mode; V <sub>DD</sub> = 3 V ± 10 % 32 kHz Crystal oscillator		–	y	15	μA
I <sub>DD6</sub>	Stop mode; V <sub>DD</sub> = 5 V ± 10 % V <sub>DD</sub> = 3 V ± 10 %	SCMOD = 0000 XT <sub>IN</sub> = 0 V	–	2.0 0.6	5 3	μA	
	Stop mode; V <sub>DD</sub> = 5 V ± 10 % V <sub>DD</sub> = 3 V ± 10 %	SCMOD = 0100		0.2 0.1	3 2		
Row Tone Level	V <sub>ROW</sub>	V <sub>DD</sub> = 2 to 5.5 V RL = 12 KΩ; Temp = -30 to 60 °C	-16.0	-14.0	-11.0	dBV	
Ratio of Column to Row tone	d <sub>BCR</sub>	V <sub>DD</sub> = 2 to 5.5 V RL = 12 KΩ; Temp = -30 to 60 °C	1	2	3		
Distortion (Dual tone)	THD	V <sub>DD</sub> = 2 to 5.5 V 1 MHz band RL = 12 KΩ; Temp = -30 to 60 °C	–	–	5	%	

**NOTES:**

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, the main system clock oscillation stops and the subsystem clock is used.
3. Currents in the following circuits are not included: on-chip pull-up resistors, internal LCD voltage dividing resistors, and output port drive currents.

Table 18-6. Main System Oscillator Characteristics

 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}, V_{DD} = 1.8\text{ V to } 5.5\text{ V})$ 

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Unit
Ceramic Oscillator		Oscillation frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3.0	
		Stabilization time <sup>(2)</sup>	Stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range; $V_{DD} = 3.0\text{ V}$	–	–	4	ms
Crystal Oscillator		Oscillation frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3.0	
		Stabilization time <sup>(2)</sup>	$V_{DD} = 3\text{ V}$	–	–	10	ms
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	–	–	30	
External Clock		$X_{IN}$ input frequency <sup>(1)</sup>	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$	0.4	–	6.0	MHz
			$V_{DD} = 1.8\text{ V to } 5.5\text{ V}$	0.4	–	3.0	
		$X_{IN}$ input high and low level width ( $t_{XH}$ , $t_{XL}$ )	–	83.3	–	1,250	ns
RC Oscillator		Frequency	$R = 25\text{ k}\Omega, V_{DD} = 5\text{ V}$	–	2	–	MHz
			$R = 40\text{ k}\Omega, V_{DD} = 3\text{ V}$	–	1	–	

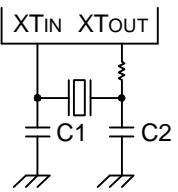
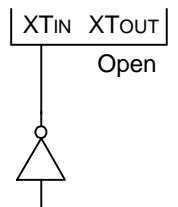
**NOTES:**

- Oscillation frequency and  $X_{IN}$  input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.



Table 18-7. Subsystem Clock Oscillator Characteristics

(T<sub>A</sub> = -40 °C + 85 °C, V<sub>DD</sub> = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	V <sub>DD</sub> = 1.8 V to 5.5 V	32	32.768	35	kHz
		Stabilization time (2)	V <sub>DD</sub> = 2.7 V to 5.5 V	–	1.0	2	s
			V <sub>DD</sub> = 1.8 V to 5.5 V	–	–	10	
External Clock		XT <sub>IN</sub> input frequency (1)	V <sub>DD</sub> = 1.8 V to 5.5 V	32	–	100	kHz
		XT <sub>IN</sub> input high and low level width (t <sub>XTL</sub> , t <sub>XTH</sub> )	–	5	–	15	μs

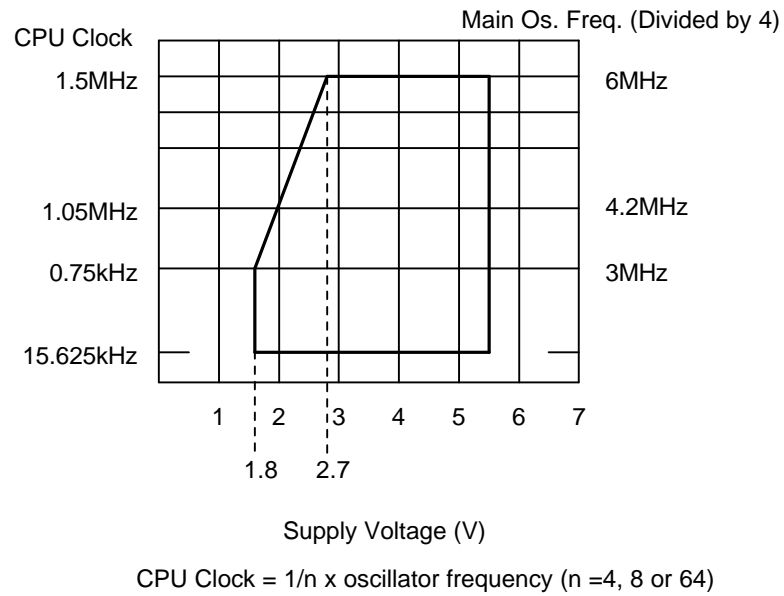
**NOTES:**

- Oscillation frequency and XT<sub>IN</sub> input frequency data are for oscillator characteristics only.
- Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 18-8. Input/Output Capacitance

(T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C <sub>IN</sub>	f = 1 MHz; Unmeasured pins are returned to V <sub>SS</sub>	–	–	15	pF
Output Capacitance	C <sub>OUT</sub>		–	–	15	pF
I/O Capacitance	C <sub>IO</sub>		–	–	15	pF



**Figure 18-2. Standard Operating Voltage Range**