



Product Preview

9-Bit Register With 3-State Outputs (Non-Inverting)

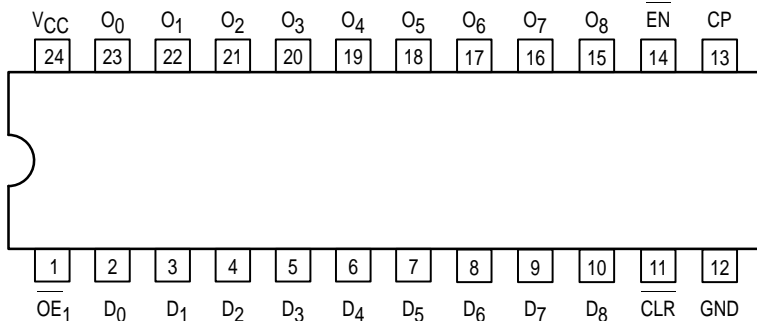
The MC74AC/ACT823 consists of nine D-type edge-triggered flip-flops. This device has 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enabled pins, the buffered clock (CP) and buffered Output Enable (OE) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With OE LOW, the contents of the flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance state.

Operation of the OE input does not affect the state of the flip-flops. The MC74AC/ACT823 has Clear (CLR) and Clock Enable (EN) pins. These devices are ideal for parity bus interfacing in high performance systems.

When CLR is LOW, and OE is LOW, the outputs are LOW. When CLR is HIGH, data can be entered into the flip-flops. When EN is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

- 3-State Outputs for Bus Interfacing
- Broad Side Pin Configuration
- ACT has TTL – Compatible Inputs
- High Speed Parallel Positive Edge-Triggered D-Type Flip-Flops
- High Performance Bus Interface Buffering for Busses Carrying Parity
- Outputs Source/Sink 24 mA

Pinout: 24-Lead Packages (Top View)



FUNCTION TABLE

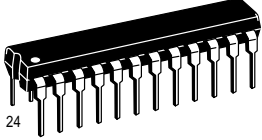
Inputs					Internal	Outputs	Operating Mode
OE	CLR	EN	CP	D _n	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level; L = LOW Voltage Level; X = Immaterial; Z = High Impedance State; ↑ = LOW-to-High Transition; NC = No Change

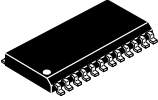
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MC74AC823
MC74ACT823

9-BIT REGISTER WITH 3-STATE OUTPUTS



N SUFFIX
CASE 724-03
PLASTIC PACKAGE



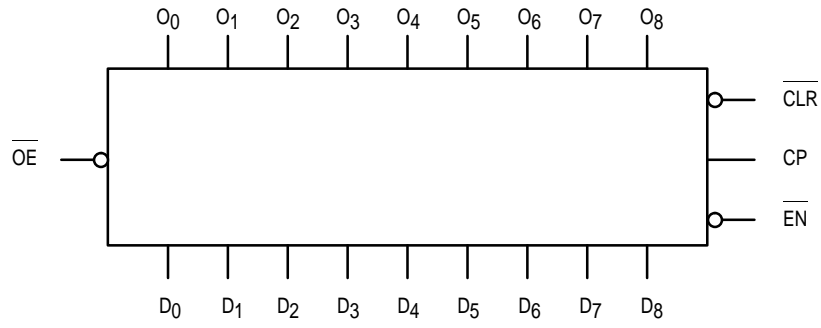
DW SUFFIX
CASE 751E-04
SOIC PACKAGE

PIN NAMES

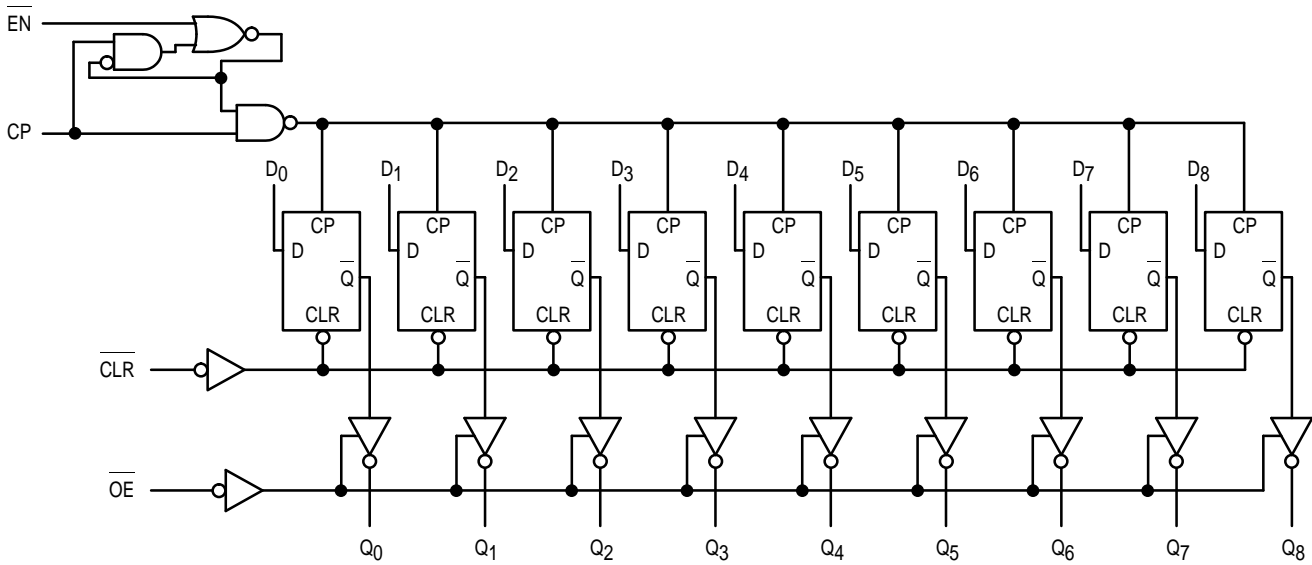
- D₀ – D₈ Data Inputs
- O₀ – O₈ Data Outputs
- OE Output Enable
- EN Clock Enable
- CLR Clear
- CP Clock Input

MC74AC823 MC74ACT823

LOGIC SYMBOL



LOGIC DIAGRAM



MC74AC823 MC74ACT823

MAXIMUM RATINGS*

Symbol	Parameter	Value	Units
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{in}	DC Input Voltage, Output Voltage (Ref. to GND)	0		V _{CC}	V	
Δt/Δv	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V		150		ns/V
		V _{CC} @ 4.5 V		40		
		V _{CC} @ 5.5 V		25		
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V		10		ns/V
		V _{CC} @ 5.5 V		8.0		
T _J	Junction Temperature (PDIP)			140	°C	
T _A	Operating Ambient Temperature Range	-40	25	85	°C	
I _{OH}	Output Current — HIGH			-24	mA	
I _{OL}	Output Current — LOW			24	mA	

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = - 50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} - 24 mA - 24 mA
		4.5		3.86	3.76			
		5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OH} 24 mA 24 mA
		4.5		0.36	0.44			
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5			-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80		μA	V _{IN} = V _{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.

† Maximum test duration 2.0 ms, one input loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0						MHz	
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0						ns	
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0						ns	
t _{PHL}	Propagation Delay CLR to O _n	3.3 5.0						ns	
t _{PZH}	Output Enable Time OE to O _n	3.3 5.0						ns	
t _{PZL}	Output Enable Time OE to O _n	3.3 5.0						ns	
t _{PHZ}	Output Disable Time OE to O _n	3.3 5.0						ns	
t _{PLZ}	Output Disable Time OE to O _n	3.3 5.0						ns	

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP	3.3 5.0					ns	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0					ns	
t _s	Set-up Time, HIGH or LOW EN to CP	3.3 5.0					ns	
t _h	Hold Time, HIGH or LOW EN to CP	3.3 5.0					ns	
t _w	CP Pulse Width HIGH or LOW	3.3 5.0					ns	
t _w	CLR Pulse Width, LOW	3.3 5.0					ns	
t _{rec}	CLR to CP Recovery Time	3.3 5.0					ns	

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} - 24 mA I _{OH} - 24 mA	
5.5		4.86	4.76					
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OH} 24 mA	
5.5		0.36	0.44					
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND	
ΔI _{CC} T	Additional Max. I _{CC} /Input	5.5	0.6		1.5			
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5			-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V _{IN} = V _{CC} or GND	

* All outputs loaded; thresholds on input associated with output under test.

† Maximum test duration 2.0 ms, one input loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0	120	158		109		MHz	
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5	5.5	9.5	1.5	10.5	ns	
t _{PHL}	Propagation Delay CP to Q _n	5.0	2.0	5.5	9.5	1.5	10.5	ns	
t _{PHL}	Propagation Delay CLR to O _n	5.0	2.5	8.0	13.5	2.0	15.5	ns	
t _{PZH}	Output Enable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns	
t _{PZL}	Output Enable Time OE to O _n	5.0	2.0	6.5	11.0	1.5	12.0	ns	
t _{PHZ}	Output Disable Time OE to O _n	5.0	1.5	6.5	11.0	1.5	12.0	ns	
t _{PLZ}	Output Disable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns	

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Set-up Time, HIGH or LOW D _n to CP	5.0	0.5	2.5	2.5	ns		
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0	2.5	2.5	ns		
t _s	Set-up Time, HIGH or LOW EN to CP	5.0	0	2.0	2.5	ns		
t _h	Hold Time, HIGH or LOW EN to CP	5.0	0	1.0	1.0	ns		
t _w	CP Pulse Width, HIGH or LOW	5.0	2.5	4.5	5.5	ns		
t _w	CLR Pulse Width, LOW	5.0	3.0	5.5	5.5	ns		
t _{rec}	CLR to CP Recovery Time	5.0	1.5	3.5	4.0	ns		

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

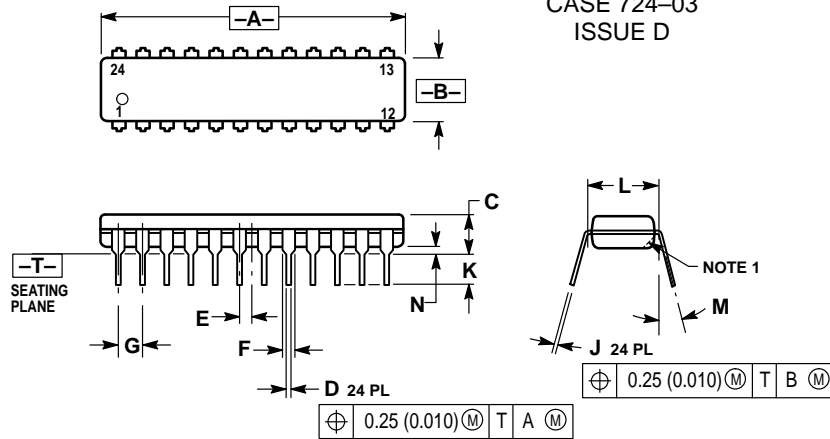
CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	44.0	pF	V _{CC} = 5.0 V

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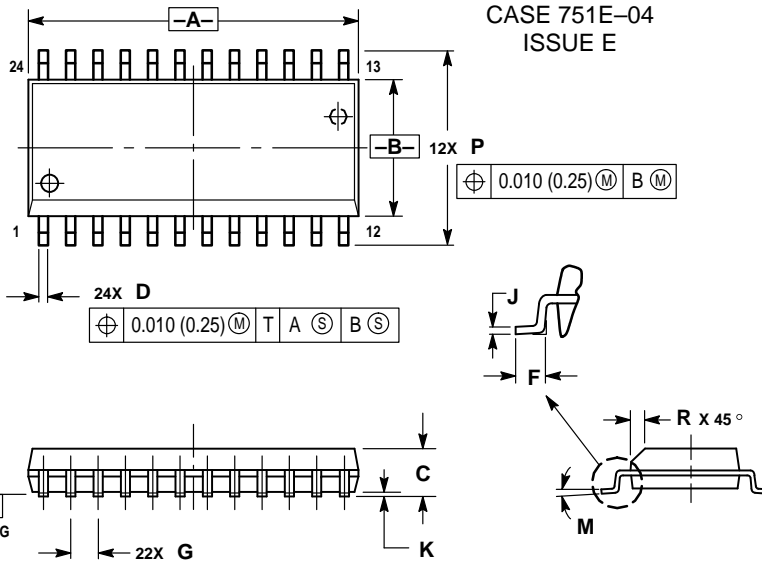
OUTLINE DIMENSIONS

N SUFFIX PLASTIC DIP PACKAGE CASE 724-03 ISSUE D




- NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH.

DW SUFFIX PLASTIC SOIC PACKAGE CASE 751E-04 ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

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MC74AC823/D

