PROCESS

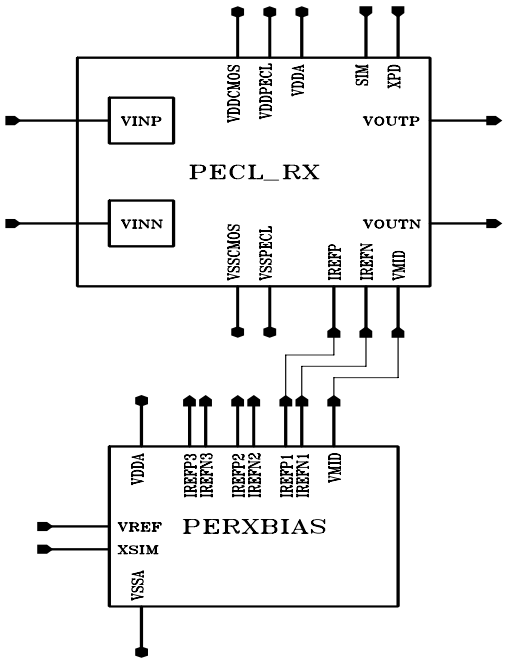
C35B3 (0.35um)

FEATURES

- PECL_RX area: 0.1 mm^2,
  size: x = 300 µm y = 340 µm
- PERXBIAS
  size: x = 382 µm y = 375 µm
- 3.3 V ±10% supply voltage
- 622 Mb/s transmission speed
- 1 ns max. propagation delay
- Power dissipation 23 mW at 3.3 V static without PERXBIAS
- Junction temperature –40 - 125°C
- Output levels fully compatible with F100K PECL Family
- Power down mode

DESCRIPTION

The PECL_RX is a 3.3 V PECL differential line receiver featuring an operating frequency up to 311 MHz (622 Mb/s) and accepting standard F100K levels (referred to the positive supply).
The PECL_RX accepts (750 mV) differential input signals and translates them to CMOS output levels.
With the companion line driver (PECL_TX) it can be used for high speed applications.
The cell PECL_RX requires the PERXBIAS cell for biasing. PERXBIAS can drive up to 3 PECL_RX cells. An external voltage reference must be used.
The PECL_RX can be set in power down mode.



TECHNICAL DATA FOR PECL_RX

($T_{junction}$ = –40 to 125 °C, VDDPECL = VDDCMOS = VDDA = +3.0 V to +3.6 V, XPD = High, SIM = Low, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Input $V_{ID} = \lvert VINP - VINN \rvert$		250	750	900	mV
V_{ICM}	Common Mode Input Voltage $V_{ICM} = (VINP + VINN) / 2$	Referred to VDDPECL	–1.5	–1.3	–1.1	V
V_{IH}	Input Voltage High	Referred to VDDPECL	–1.165		–0.870	V
V_{IL}	Input Voltage Low	Referred to VDDPECL	–1.830		–1.475	V
V_{HYS}	Hysteresis		25		100	mV
V_{OH}	Output Voltage High		CMOS levels			V
V_{OL}	Output Voltage Low					V

AC CHARACTERISTICS

C_L = 1 pF at each output, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	Propagation Delay [1]		600	800	1000	ps
t_{SKD1}	Differential Pulse Skew [1]				80	ps
t_{SKD2}	Differential Channel to Channel Skew [1]				100	ps
t_{TLH}	Rise Time [2]		150	300	600	ps
t_{THL}	Fall Time [2]		150	300	600	ps
C_{load}	Load Capacitance	@622 Mb/s			1	pF
C_{in}	Input Capacitance			700	900	fF
f_{MAX}	Operating Frequency			311	311	MHz
T_{XS}	Transmission Rate			622	622	Mb/s

POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCDC}	DC Current Consumption	Without PERXBIAS		7	10	mA
I_{CCAC}	AC Current Consumption	C_{load} = 1 pF @622 Mb/s, without PERXBIAS		11	15	mA
I_{CCPD}	Power Down Current Consumption	XPD = Low, without PERXBIAS			300	µA
P_{diss_DC}	DC Power Consumption	Without PERXBIAS		23	36	mW
P_{diss_AC}	AC Power Consumption	C_{load} = 1 pF @622 Mb/s, without PERXBIAS		36	54	mW
P_{diss_PD}	Power Consumption in Power Down Mode	XPD = Low, without PERXBIAS			1.08	mW

1) Including the package: SOIC28, pins 5–10 or 19–24 for VOUTP and VOUTN

2) Specified at 20% and 80% of the output voltage

TECHNICAL DATA FOR PERXBIAS

($T_{junction}$ = –40 to 125 °C, VDDA = +3.0 V to +3.6 V, XSIM = High, unless otherwise specified)

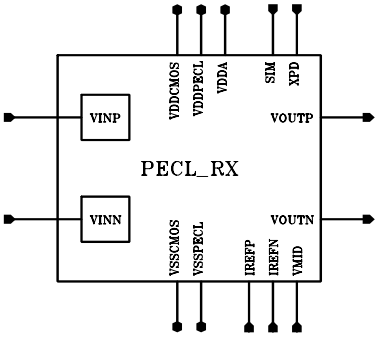
POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	DC Current Consumption			1.2	2	mA
P_{diss}	Power Consumption			4	7.2	mW

REFERENCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Reference Voltage		1.20	1.22	1.24	V

SYMBOL OF PECL_RX

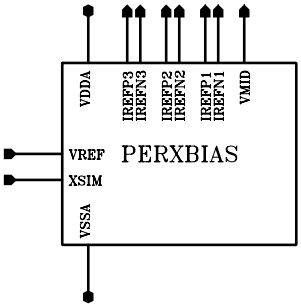


XPD	VINP	VINN	VOUTP	VOUTN
High	High	Low	High	Low
High	Low	High	Low	High
Low	X	X	High	Low

PIN LIST OF PECL_RX

Pin	Description	Type
VDDPECL	Positive Supply for PECL Receiver	Supply
VDDA	Positive Supply	Supply
VDDCMOS	Positive Supply for CMOS Output Buffer	Supply
VSSPECL	Negative Supply	Supply
VSSCMOS	Negative Supply	Supply
IREFP	Bias Current	Analog
IREFN	Bias Current	Analog
VMID	Voltage Reference	Analog
XPD	Power Down	Digital
SIM	Test Pin	Digital
VINP	Positive Input	Analog
VINN	Negative Input	Analog
VOUTP	Pos. PECL Output	Digital
VOUTN	Neg. PECL Output	Digital

SYMBOL OF PERXBIAS



PIN LIST OF PERXBIAS

Pin	Description	Type
VDDA	Positive Supply	Supply
VSSA	Negative Supply	Supply
IREFP1	Bias Current	Analog
IREFP2	Bias Current	Analog
IREFP3	Bias Current	Analog
IREFN1	Bias Current	Analog
IREFN2	Bias Current	Analog
IREFN3	Bias Current	Analog
VMID	Voltage Reference	Analog
XSIM	Test Pin	Digital
VREF	External Reference Voltage	Analog

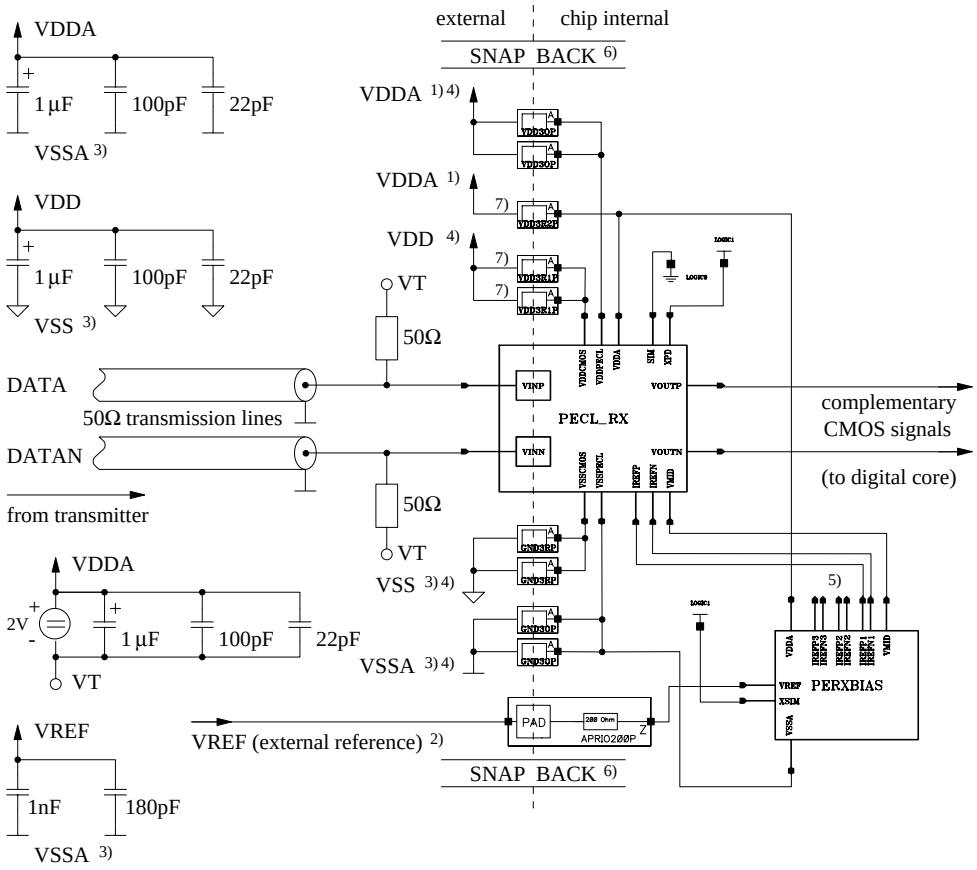
THEORY OF OPERATION

The PECL_RX is a differential line receiver which accepts low voltage input signals according to F100K standard.
The input signal lines must be 50 Ω transmission lines. At the receiver input each signal has to be terminated to the voltage level V_T (where V_T = VDDPECL – 2 V) with an external termination resistor of 50 Ω, but also other termination schemes are possible. The cell PECL_RX can be set in power down mode. It requires the PERXBIAS cell for biasing. PERXBIAS can drive up to 3 PECL_RX cells. An external voltage reference must be used.

APPLICATION

- High Speed Backplane Driver
- Complementary Clock Drivers
- Level Translator
- System Interconnects
- ATM Applications
- SDH Applications
- High-Resolution Imaging Applications
- Laser Printers
- Digital Copiers

TYPICAL APPLICATION



1) Each power pin must have its own set of blocking capacitors.
2) An external reference must be used.
3) VSSA and VSS must be connected on the PCB level.
4) The two power pads can be bonded to one package pin (double bonding).
5) Two more PECL_RX cells can be driven with IREFxx of the PERXBIAS cell. If an output IREFxx is not used it must be left unconnected.
6) The PECL part of the chip has to be separated from the rest of the chip by use of snap backs (cell PWRCUT_DIG_P_SNAP_SNAP).
7) The cells VDD3R1P and VDD3R2P are not in the standard library, they are part of the IP-block.

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