

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MH161FK, TC7MH163FK

Synchronous Presetable 4-Bit Binary Counter

TC7MH161FK Asynchronous Clear

TC7MH163FK Synchronous Clear

The TC7MH161FK and 163FK are advanced high speed CMOS synchronous presetable 4-bit binary counters fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both  $\overline{\text{LOAD}}$  and  $\overline{\text{CLR}}$  inputs are active on low logic level.

Presetting of each IC's is synchronous to the rising edge of CK.

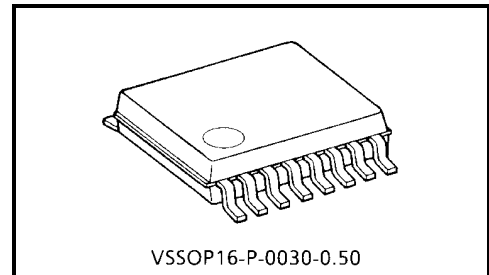
The clear function of the TC7MH163FK is synchronous to CK, while the TC7MH161FK are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

An input protection circuit ensures that 0 to 7 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## Features

- High speed:  $f_{\text{max}} = 185 \text{ MHz (typ.) (VCC = 5 V)}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A (max) (Ta = 25^\circ\text{C})}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC (min)}}$
- Power down protection is equipped with all inputs.
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC (opr)}} = 2\sim 5.5 \text{ V}$
- Low noise:  $V_{\text{OLP}} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS161/163



Weight: 0.02 g (typ.)

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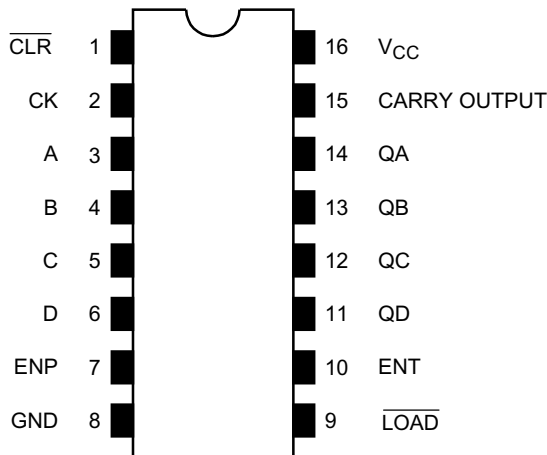
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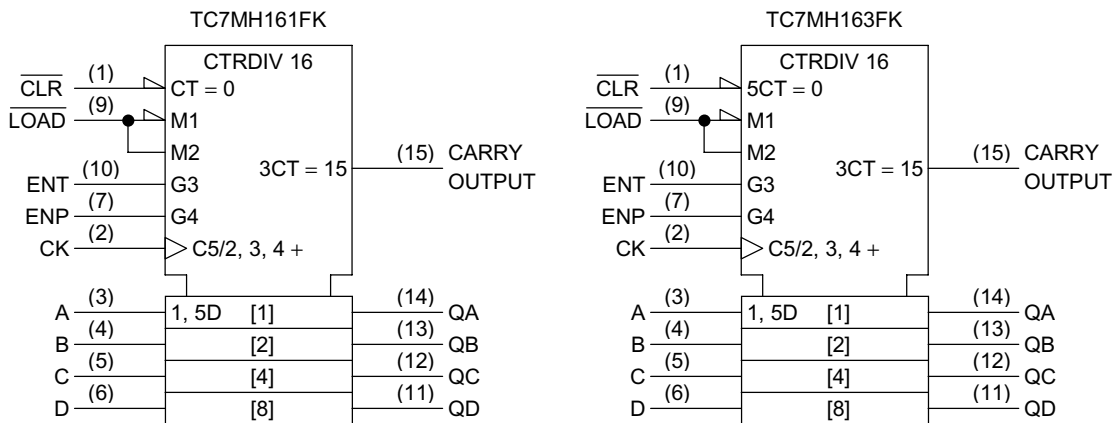
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## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

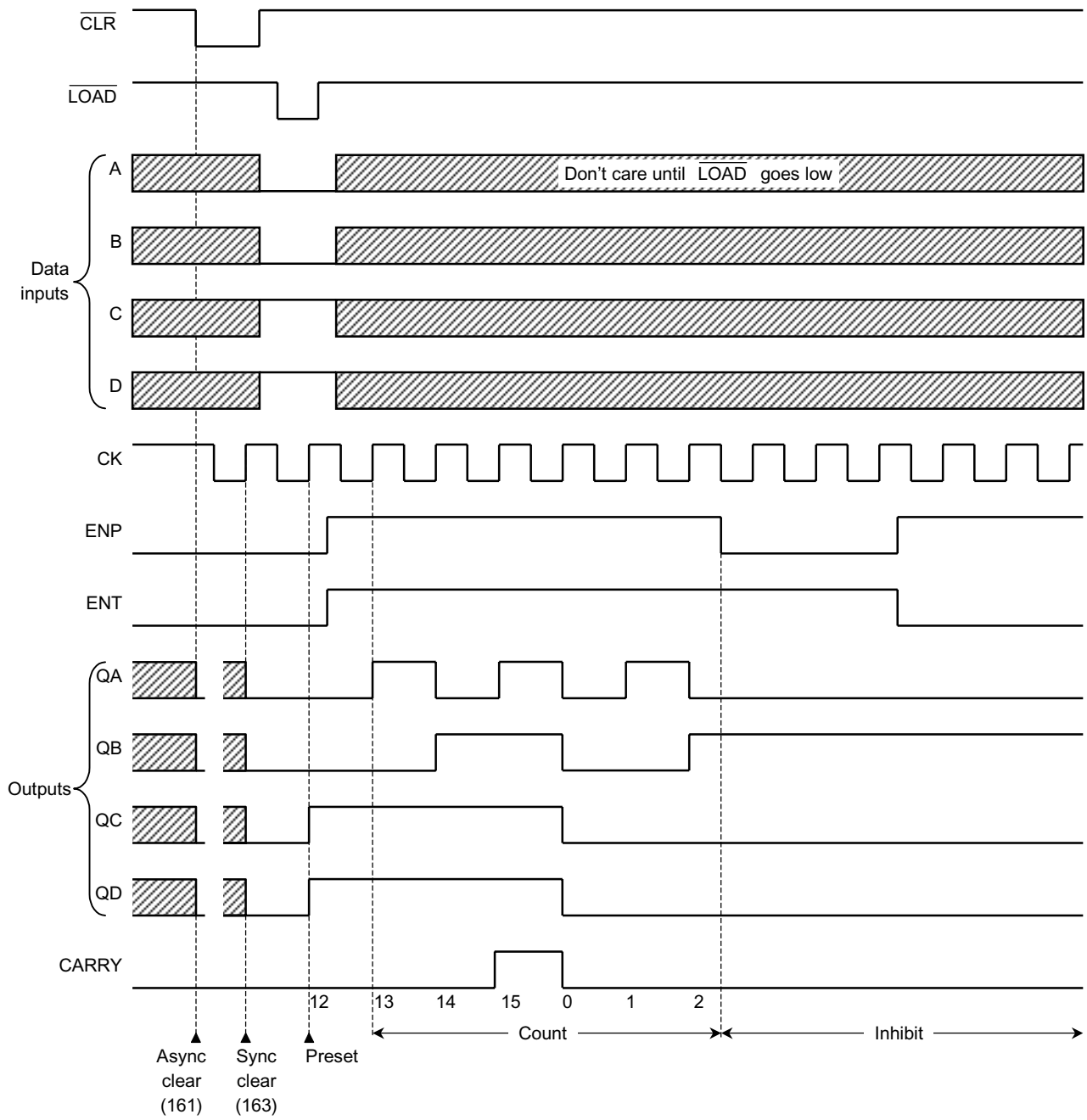
TC7MH161FK					TC7MH163FK					Outputs				Function
Inputs					Inputs					QA	QB	QC	QD	
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK					
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	Reset to "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	Reset data.
H	H	X	L	↑	H	H	X	L	↑	No change				No count
H	H	L	X	↑	H	H	L	X	↑	No change				No count
H	H	H	H	↑	H	H	H	H	↑	Count up				Count
H	X	X	X	↓	X	X	X	X	↓	No change				No count

X: Don't care

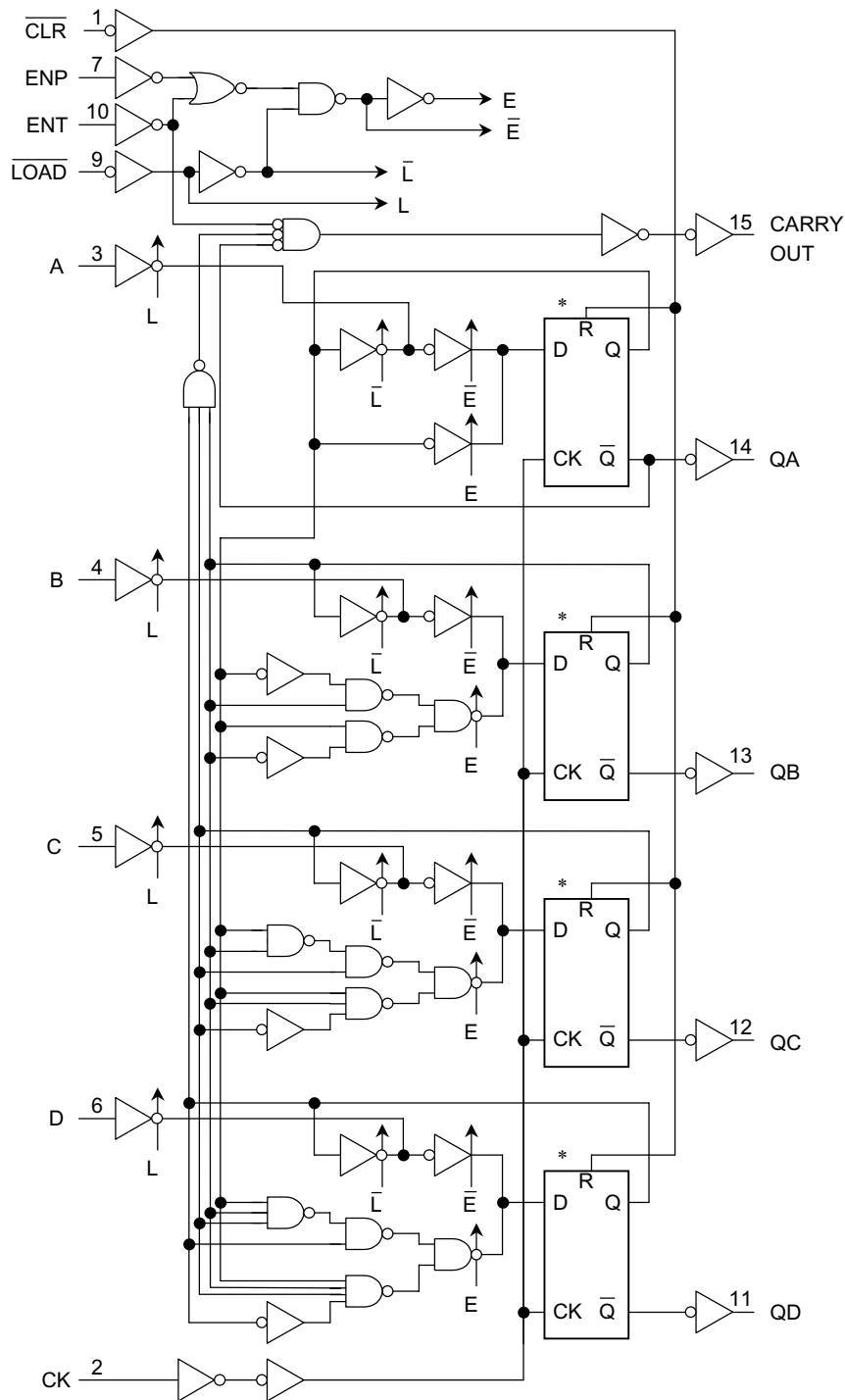
A, B, C, D: Logic level of data inputs

Carry: CARRY = ENT · QA · QB · QC · QD

**Timing Chart**



**System Diagram**



\*: Truth table of internal F/F

TC7MH161FK					TC7MH163FK				
D	CK	R	Q	$\bar{Q}$	D	CK	R	Q	$\bar{Q}$
X	X	H	L	H	X	$\uparrow$	H	L	H
L	$\uparrow$	L	L	H	L	$\uparrow$	L	L	H
H	$\uparrow$	L	H	L	H	$\uparrow$	L	H	L
X	$\downarrow$	L	No change		X	$\downarrow$	X	No change	

X: Don't care

## Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5~7.0	V
DC input voltage	V <sub>IN</sub>	-0.5~7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

## Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0~5.5	V
Input voltage	V <sub>IN</sub>	0~5.5	V
Output voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time	dt/dv	0~100 (V <sub>CC</sub> = 3.3 ± 0.3 V) 0~20 (V <sub>CC</sub> = 5 ± 0.5 V)	ns/V

## Electrical Characteristics

### DC Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
Input voltage	High level	V <sub>IH</sub>	—	2.0 3.0~5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V	
	Low level	V <sub>IL</sub>	—	2.0 3.0~5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3		
Output voltage	High level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
				I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
	Low level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0 0 0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	
				I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
				I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0~5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA	

## Timing Requirements (Input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C	Ta = -40~85°C	Unit
				Limit	Limit	
Minimum pulse width (CK)	$t_w(H)$ $t_w(L)$	Figure 1	3.3 ± 0.3	5.0	5.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum pulse width ( $\overline{CLR}$ )	$t_w(L)$	Figure 4 (Note1)	3.3 ± 0.3	5.0	5.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum set-up time (A, B, C, D)	$t_s$	Figure 2	3.3 ± 0.3	5.5	6.5	ns
			5.0 ± 0.5	4.5	4.5	
Minimum set-up time ( $\overline{LOAD}$ )	$t_s$	Figure 2	3.3 ± 0.3	8.0	9.5	ns
			5.0 ± 0.5	5.0	6.0	
Minimum set-up time (ENT, ENP)	$t_s$	Figure 3	3.3 ± 0.3	7.5	9.0	ns
			5.0 ± 0.5	5.0	6.0	
Minimum set-up time ( $\overline{CLR}$ )	$t_s$	Figure 5 (Note2)	3.3 ± 0.3	4.0	4.0	ns
			5.0 ± 0.5	3.5	3.5	
Minimum hold time	$t_h$	Figure 2, Figure 3	3.3 ± 0.3	1.0	1.0	ns
			5.0 ± 0.5	1.0	1.0	
Minimum hold time ( $\overline{CLR}$ )	$t_h$	Figure 5 (Note2)	3.3 ± 0.3	1.0	1.0	ns
			5.0 ± 0.5	1.5	1.5	
Minimum removal time ( $\overline{CLR}$ )	$t_{rem}$	Figure 4 (Note1)	3.3 ± 0.3	2.5	2.5	ns
			5.0 ± 0.5	1.5	1.5	

Note1: for TC7MH161FK only

Note2: for TC7MH163FK only

**AC Characteristics (Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	Figure 1, Figure 2	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time (CK-CARRY) [Count mode]	$t_{pLH}$ $t_{pHL}$	Figure 1	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	ns
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time (CK-CARRY) [Preset mode]	$t_{pLH}$ $t_{pHL}$	Figure 2	3.3 ± 0.3	15	—	11.0	17.2	1.0	20.0	ns
				50	—	13.5	20.7	1.0	23.5	
			5.0 ± 0.5	15	—	6.2	10.3	1.0	12.0	
				50	—	7.7	12.3	1.0	14.0	
Propagation delay time (ENT-CARRY)	$t_{pLH}$ $t_{pHL}$	Figure 6	3.3 ± 0.3	15	—	7.5	12.3	1.0	14.5	ns
				50	—	10.5	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	$t_{pHL}$	Figure 4 (Note4)	3.3 ± 0.3	15	—	8.9	13.6	1.0	16.0	ns
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	5.5	9.0	1.0	10.5	
				50	—	7.0	11.0	1.0	12.5	
Propagation delay time ( $\overline{\text{CLR}}$ -CARRY)	$t_{pHL}$	Figure 4 (Note4)	3.3 ± 0.3	15	—	8.4	13.2	1.0	15.5	ns
				50	—	10.9	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.0	8.6	1.0	10.0	
				50	—	6.5	10.6	1.0	12.0	
Maximum clock frequency	$f_{max}$	—	3.3 ± 0.3	15	80	130	—	70	—	MHz
				50	55	85	—	50	—	
			5.0 ± 0.5	15	135	185	—	115	—	
				50	95	125	—	85	—	
Input capacitance	C <sub>IN</sub>	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	—	(Note3)	—	23	—	—	—	pF	

Note3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C<sub>PD</sub>, and  $\Delta I_{CC}$  which is obtained from the following formula:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left( \frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

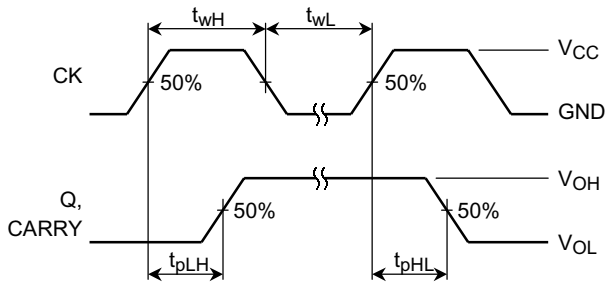
C<sub>QA</sub>~C<sub>QD</sub> and C<sub>CO</sub> are the capacitance QA~QD and CARRY OUT, respectively.

f<sub>CK</sub> is the input frequency of the CK.

Note4: for TC7MH161FK only

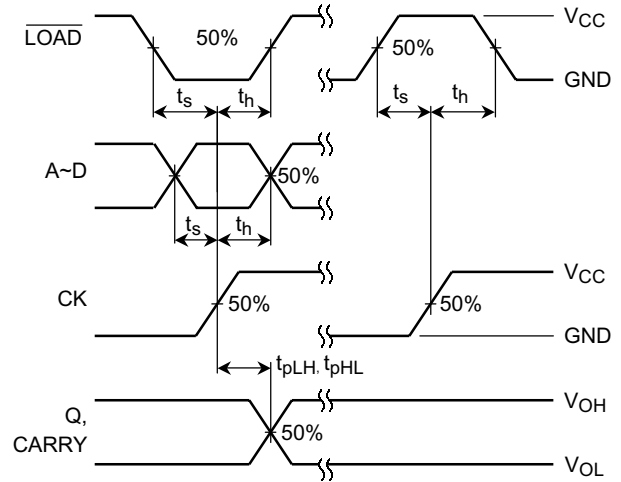
**AC Test Waveform**

**Count Mode**



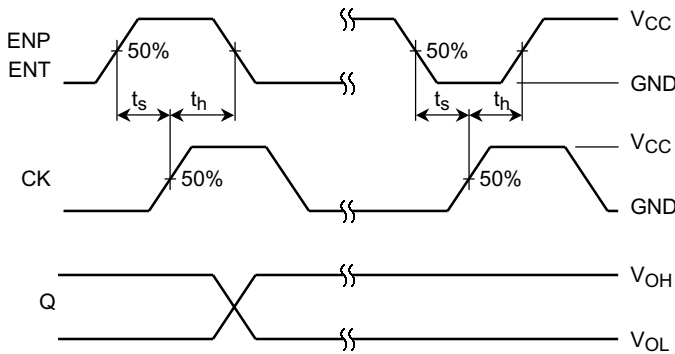
**Figure 1**

**Preset Mode**



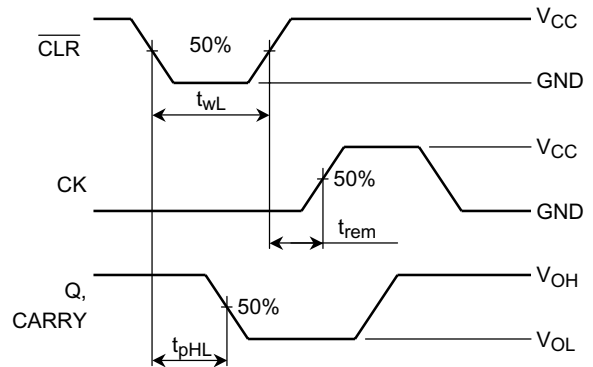
**Figure 2**

**Count Enable Mode**



**Figure 3**

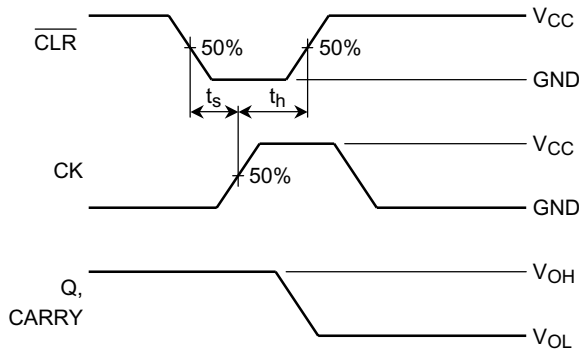
**Clear Mode (TC7MH161FK)**



**Figure 4**

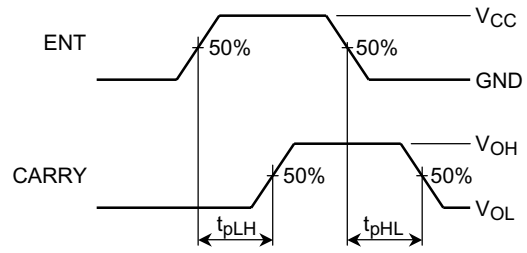


**Clear Mode (TC7MH163FK)**



**Figure 5**

**Cascade Mode (fix maximum count)**

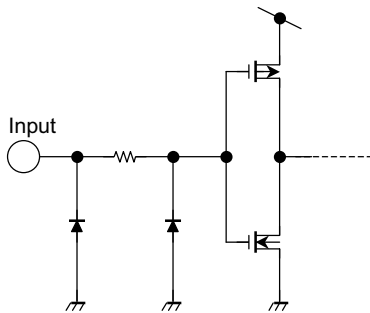


**Figure 6**

**Noise Characteristics (Input:  $t_r = t_f = 3$  ns)**

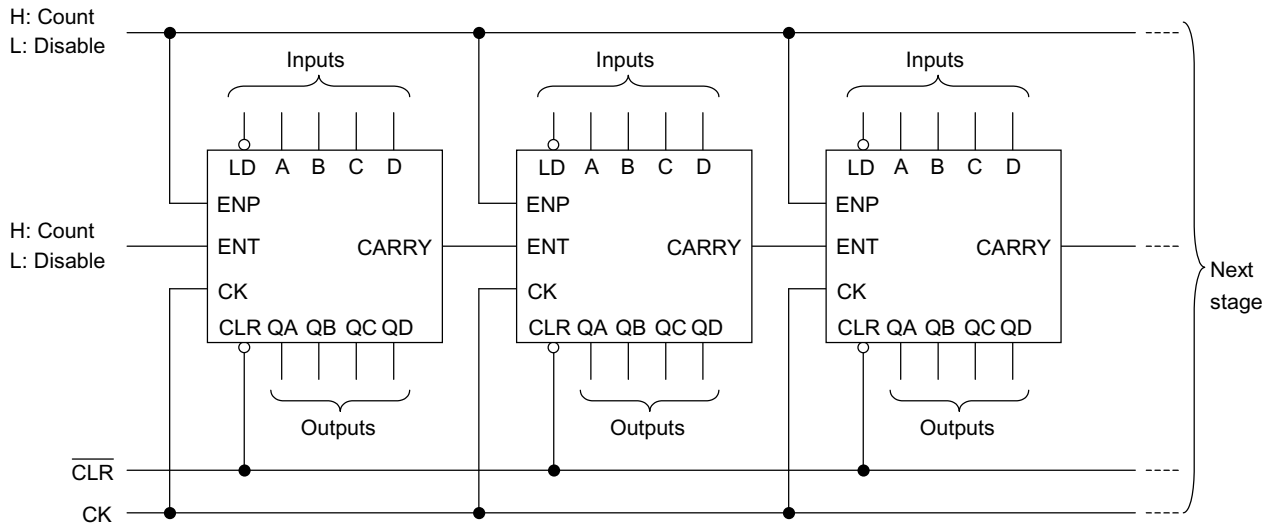
Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.4	-0.8	V
Minimum high level dynamic input voltage V <sub>IH</sub>	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V <sub>IL</sub>	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Input Equivalent Circuit**



**Typical Application**

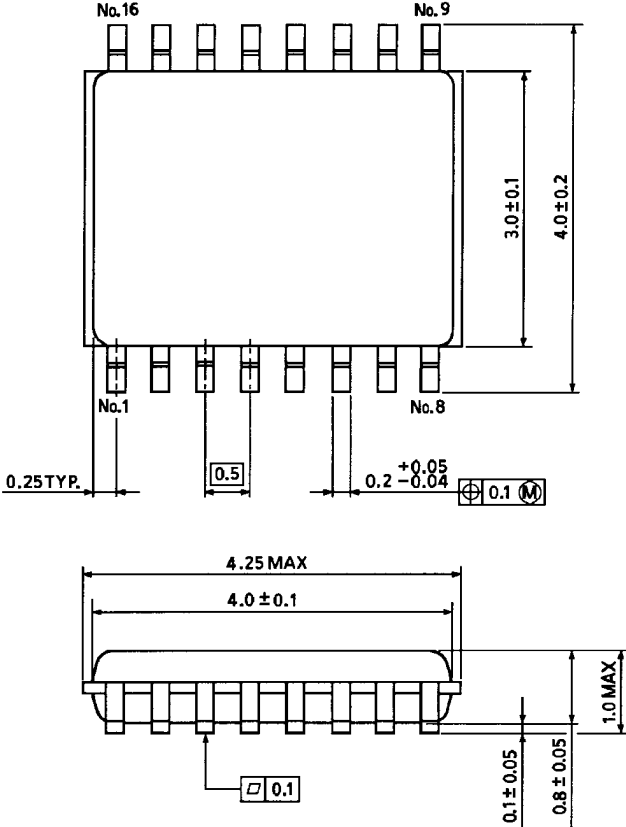
**Parallel Carry N-Bit Counter**



Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)