Telecommunication LSI

TC35143BF

Analog Front End LSI

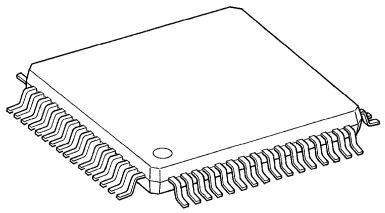
Version 1.00

980910EBA1-981021TS

Contents

1. Description

TC35143BF is a suitable analog front end LSI for handy communicator such as an HPC(Handheld PC). This LSI includes a line interface for V.34,V.90 a voice interface which is suitable for hands free/hand set system and a touch screen interface. TC35143BF communicates with a host processor through a serial interface called SIB. A host processor supplies the synchronization clock and shift clock to TC35143BF. Since all clocks of TC35143BF are generated from the shift clock, crystal for TC35143BF is not necessary. ADC/DAC sampling data of each interface, the control data to TC35143BF and the status data from TC35143BF are all transferred through this SIB interface.



LQFP64-P-1010-0.50A

2. Feature

2.1 Line Interface

- ☐ 16bit ADC/DAC
- ☐ Programmable input gain amplifier(2 levels/6dB step)
- ☐ ADC clip detector
- ☐ Differential line driver and receiver
- ☐ Analog echo canceler
- ☐ Programmable sampling frequency (three frequencies : 7.2 kHz, 8 kHz, and 9.6 kHz)

2.2 Voice Interface

- ☐ 14bit ADC/DAC
- ☐ 2 channel differential microphone inputs and 2 channel differential speaker outputs (useful for hands-free / handset system)
- ☐ Enabling/disabling for each block
- ☐ Mute switches in microphone input pass and speaker output pass
- ☐ Programmable microphone gain amplifier (15 levels/1.5dB step and 4 levels/6 dB step)
- ☐ Programmable speaker output attenuator (8 levels/3 dB step)
- ☐ Programmable sampling frequency (four frequencies : 8 kHz / approximately 11.08 kHz / 16 kHz / approximately 22.15 kHz)

2.3 Touch Screen Interface

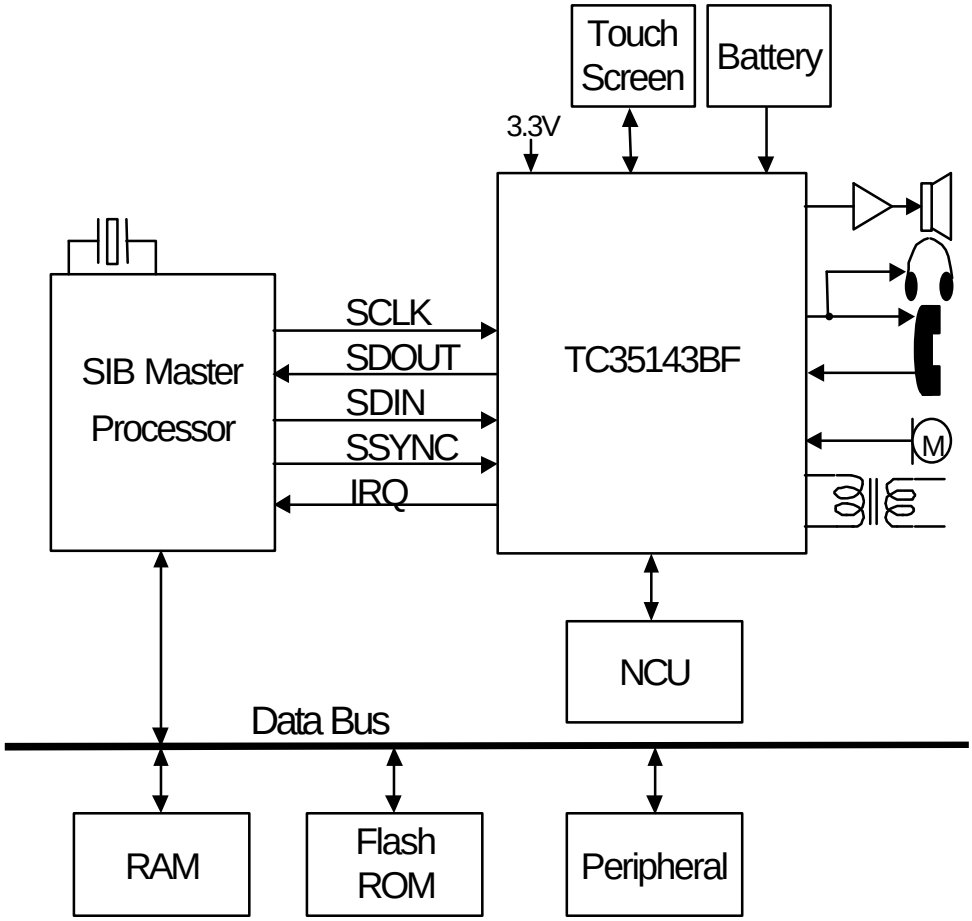
- ☐ 10bit ADC for voltage measurement
- ☐ Pen touch detection(Available during stand-by mode)
- ☐ Plate bias voltage generator
- ☐ Auxiliary analog input ports(4 ports)

2.4 Others

- ☐ 10 channels I/O ports
- ☐ Multi-chip connectivity via SIB(SIB input frequency is 9.216MHz)
- ☐ Interrupt output port
- ☐ +3.3V single power supply
- ☐ 64 pin plastic package

3. System Block Diagram

Below figure shows system block diagram using TC35143BF.



3.1 Internal System

The internal system block diagram is shown in the following figure.

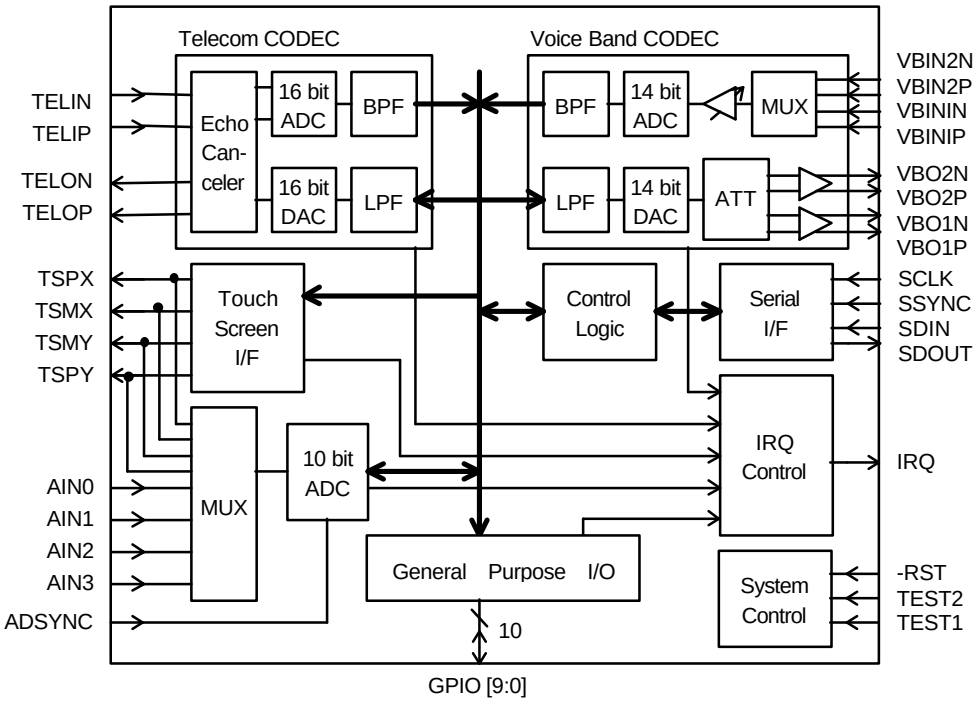


Figure 3.1.A TC35143BF block diagram

The line interface consists of a 16 bit ADC, a 16 bit DAC, an analog echo canceler for suppression of the telecom output signal and a voice band filter, which consist of an digital band pass filter. The ADC and the DAC have a performance for V.34,V.90 modem communications. Enabling and disabling of high pass filtering of the received band pass filter is useful for detecting several call progress tones. The differential interface extends dynamic range of reception signal. Individual enabling and disabling for the input and the output block save power consumption.

The voice interface is composed of a 14-bit ADC, 14-bit DAC, a digital filter for limiting the bandwidth, and an attenuator for adjusting the input/output levels. The 14-bit ADC and DAC allow you to configure a system featuring superior sound quality. Two channels of input and output pins each are provided for hands-free and handset use. An internal analog switch allows you to choose two channels of microphone input. Two channels of speaker outputs each are provided with an attenuator, so that sound volume on each speaker output can be adjusted independently. The input and output blocks can be powered off individually, making it possible to save power consumption.

The touch-screen interface controls the bias voltage applied to the touch-screen resistor network and switches over the circuits to measure the voltage of the resistor network. Four pins, TSPX, TSMX, TSMY, and TSPY, are used to apply a bias voltage to the resistor network and read out its measured voltage. The voltage is measured using a 10-bit ADC. An internal switch allows selection of either the touch-screen voltage input or general-purpose voltage input. The four channels of general-purpose voltage inputs can be used to monitor the battery voltage or for other purposes.

Ten general-purpose I/O ports are included as an additional function. These I/O ports can be used to control the NCU, etc.

Control of each block and transfer of sample data all are performed via a serial interface. in description.

4. Pin Function

4.1 Pin Layout

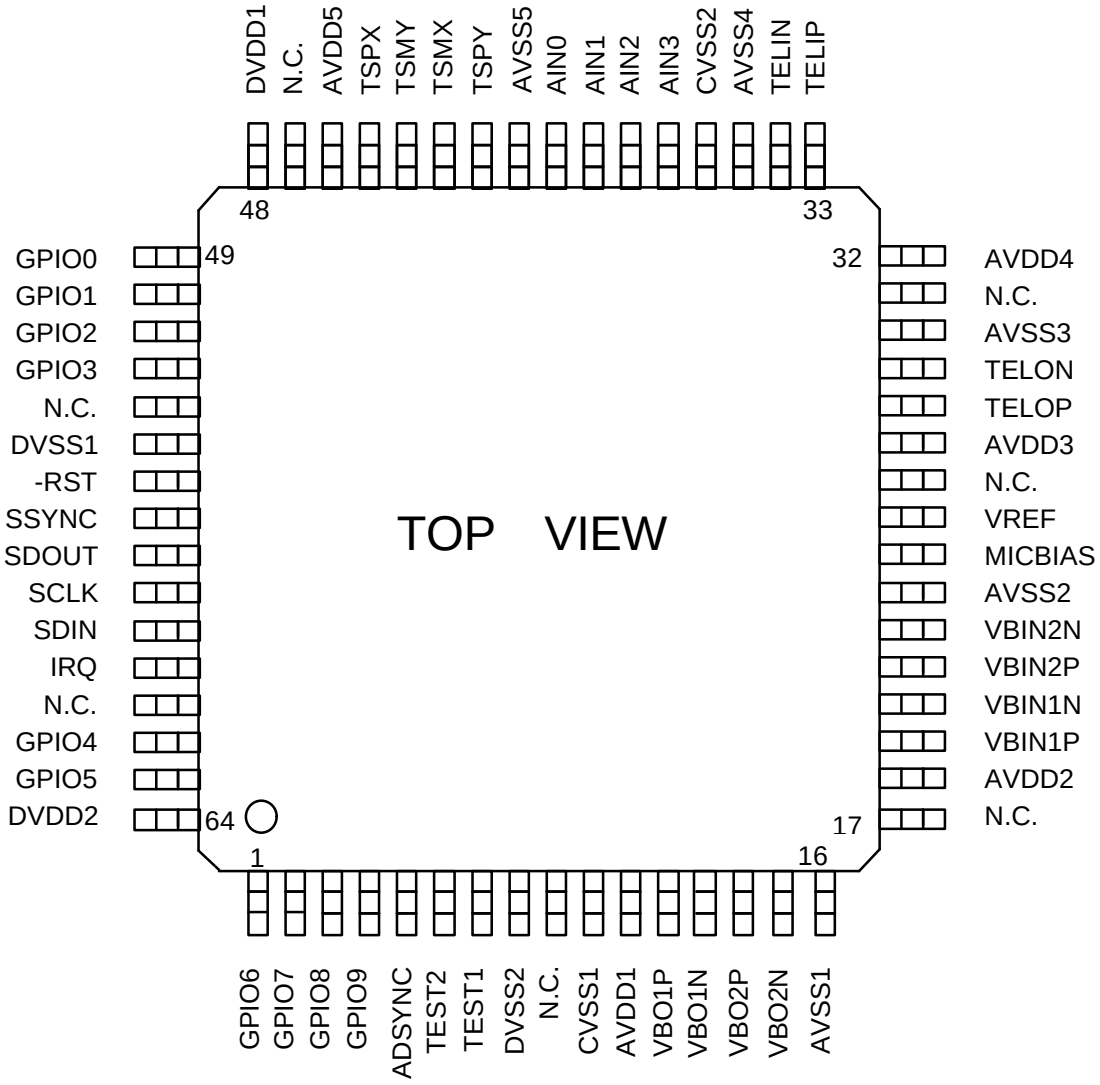


Figure 4.1.A TC35143BF pin layout

4.2 Pin Function

Table 4.2.A The pin function of TC35143BF(1/3)

Pin name	Pin No.	A/D/P	I/O	DEF	Group	Function
SCLK	58	D	I	-	HOST	The bit clock of the host interface. This clock is user as the internal master clock. It should be 9.216MHz clock with duty 50%. Connect this pin to the clock output of the SIB master chip.
SSYNC	56	D	I	-	HOST	The synchronization clock of host interface. This clock should be 72kHz. 128 bits of serial data constitutes one frame. Connect this pin to the sync signal output of the SIB master chip.
SDIN	59	D	I	-	HOST	The host data input. The data is latched at the falling edge of SCLK. Connect this pin to the data output of the SIB master chip.
SDOUT	57	D	O	HZ	HOST	The host data output. The data is output at the rising edge of SCLK. Connect this pin to the data input of the SIB master chip.
IRQ	60	D	O	L	HOST	The interrupt request output. High active. Use the control register to set the interrupt sources.
-RST	55	D	I	-	HOST	The system reset input. Low active.
TSPX	45	A	I/O	HZ (IN)	TSC	The touch screen interface terminal for X plate. When not using this pin, leave it open.
TSMX	43	A	I/O	HZ (IN)	TSC	The touch screen interface terminal for X plate. When not using this pin, leave it open.
TSPY	42	A	I/O	HZ (IN)	TSC	The touch screen interface terminal for Y plate. When not using this pin, leave it open.
TSMY	44	A	I/O	HZ (IN)	TSC	The touch screen interface terminal for Y plate. When not using this pin, leave it open.
AIN0	40	A	I	-	ADC	The ADC input terminal. When not using this pin, leave it open.
AIN1	39	A	I	-	ADC	The ADC input terminal. When not using this pin, leave it open.
AIN2	38	A	I	-	ADC	The ADC input terminal. When not using this pin, leave it open.
AIN3	37	A	I	-	ADC	The ADC input terminal. When not using this pin, leave it open.
ADSYNC	5	A	I	-	ADC	The external synchronization clock input for ADC According to edge, the ADC starts conversion in ADC sync mode. When not using this pin, pull it to GND.

A/D/P : A - Analog part, D - Digital part, P - Power supply
I/O : I - Input, O - Output, I/O - BI-direction
DEF : This means default status of the pin.
H - Hi level, L - Low level, Hz - high impedance, IN - input mode
Group : This means the functional group of the pin.
HOST - Host interface, TSC - Touch screen interface,
TEL - Telecom CODEC, VB - Voice band CODEC, ETC - The other,
POW - power supply

Table 4.2.B The pin function of TC35143BF(2/3)

Pin name	Pin No.	A/D/P	I/O	DEF	Group	Function
TELOP	28	A	O	HZ	TEL	The telecom positive output. When not using this pin, leave it open.
TELON	29	A	O	HZ	TEL	The telecom negative output. When not using this pin, leave it open.
TELIP	33	A	I	-	TEL	The telecom positive input. When not using this pin, leave it open.
TELIN	34	A	I	-	TEL	The telecom negative input. When not using this pin, leave it open.
VBO1P	12	A	O	HZ	VB	The voice band CODEC positive output 1. This pin is used for a handset receiver.
VBO1N	13	A	O	HZ	VB	The voice band CODEC negative output 1. This pin is used for a handset receiver.
VBO2P	14	A	O	HZ	VB	The voice band CODEC positive output 2. This pin is used for an external speaker.
VBO2N	15	A	O	HZ	VB	The voice band CODEC negative output 2. This pin is used for an external speaker.
VBIN1P	19	A	I	-	VB	The voice band CODEC positive input 1. This pin is used for a handset microphone. When not using this pin, leave it open.
VBIN1N	20	A	I	-	VB	The voice band CODEC negative input 1. This pin is used for a handset microphone. When not using this pin, leave it open.
VBIN2P	21	A	I	-	VB	The voice band CODEC positive input 2. This pin is used for an external microphone. When not using this pin, leave it open.
VBIN2N	22	A	I	-	VB	The voice band CODEC negative input 2. This pin is used for an external microphone. When not using this pin, leave it open.
MICBIAS	24	A	O	HZ	VB	The voltage source for electret microphone. Insert an electrolytic capacitor of 10 μF or more cascadely between this pin and analog GND and a 2kΩ resistor.
GPIO0	49	D	I/O	HZ (IN)	GPIO	These pins are general purpose I/O. Use the control register to set each port for input/output and the output level. These ports are set for input by default after a reset. When not using these pins, pull them to GND.
GPIO1	50	D	I/O	HZ (IN)	GPIO	
GPIO2	51	D	I/O	HZ (IN)	GPIO	
GPIO3	52	D	I/O	HZ (IN)	GPIO	
GPIO4	62	D	I/O	HZ (IN)	GPIO	
GPIO5	63	D	I/O	HZ (IN)	GPIO	
GPIO6	1	D	I/O	HZ (IN)	GPIO	
GPIO7	2	D	I/O	HZ (IN)	GPIO	
GPIO8	3	D	I/O	HZ (IN)	GPIO	
GPIO9	4	D	I/O	HZ (IN)	GPIO	

Table 4.2.C The pin function of TC35143BF(3/3)

Pin name	Pin No.	A/D/P	I/O	DEF	Group	Function
TEST1	7	D	I	-	ETC	The test terminal 1. This pin should be grounded.
TEST2	6					The test terminal 2. This pin should be grounded.
VREF	25	A	I/O	HZ (OUT)	ETC	The internal analog reference voltage. Insert a 10 μF electrolytic capacitor between the analog GND and this pin and also a 33 kΩ resistor between the analog Vdd and this pin. The pin direction is determined by register settings.
DVDD1	48	P	-	-	POW	The digital power supply input. Fix these pins to +3.3V. Insert a 0.1 μF laminated ceramic capacitor between each of these pins and the digital VSS of the same number. Make sure the capacitor is inserted as close to the pin as possible.
DVDD2	64	P	-	-	POW	
AVDD1	11	P	-	-	POW	The analog power supply input. Fix these pins to +3.3V. Insert a 0.1 μF laminated ceramic capacitor between each of these pins and the analog VSS of the same number. Make sure the capacitor is inserted as close to the pin as possible.
AVDD2	18	P	-	-	POW	
AVDD3	27	P	-	-	POW	
AVDD4	32	P	-	-	POW	
AVDD5	46	P	-	-	POW	
DVSS1	54	P	-	-	POW	The digital ground. Use a pattern design so that this pin is separated from the analog GND.
DVSS2	8	P	-	-	POW	
AVSS1	16	P	-	-	POW	The analog ground. Use a pattern design so that this pin is separated from the digital GND.
AVSS2	23	P	-	-	POW	
AVSS3	30	P	-	-	POW	
AVSS4	35	P	-	-	POW	
AVSS5	41	P	-	-	POW	
CVSS1	10	P	-	-	POW	The common ground. Connect this pin to the analog GND.
CVSS2	36	P	-	-	POW	
NC	9, 17, 26, 31, 47, 53, 61	-	-	-	-	Non connection pins. Leave it open.

5. Function

5.1 Hardware Interface

The system example using TC35143BF is shown in the following figure.

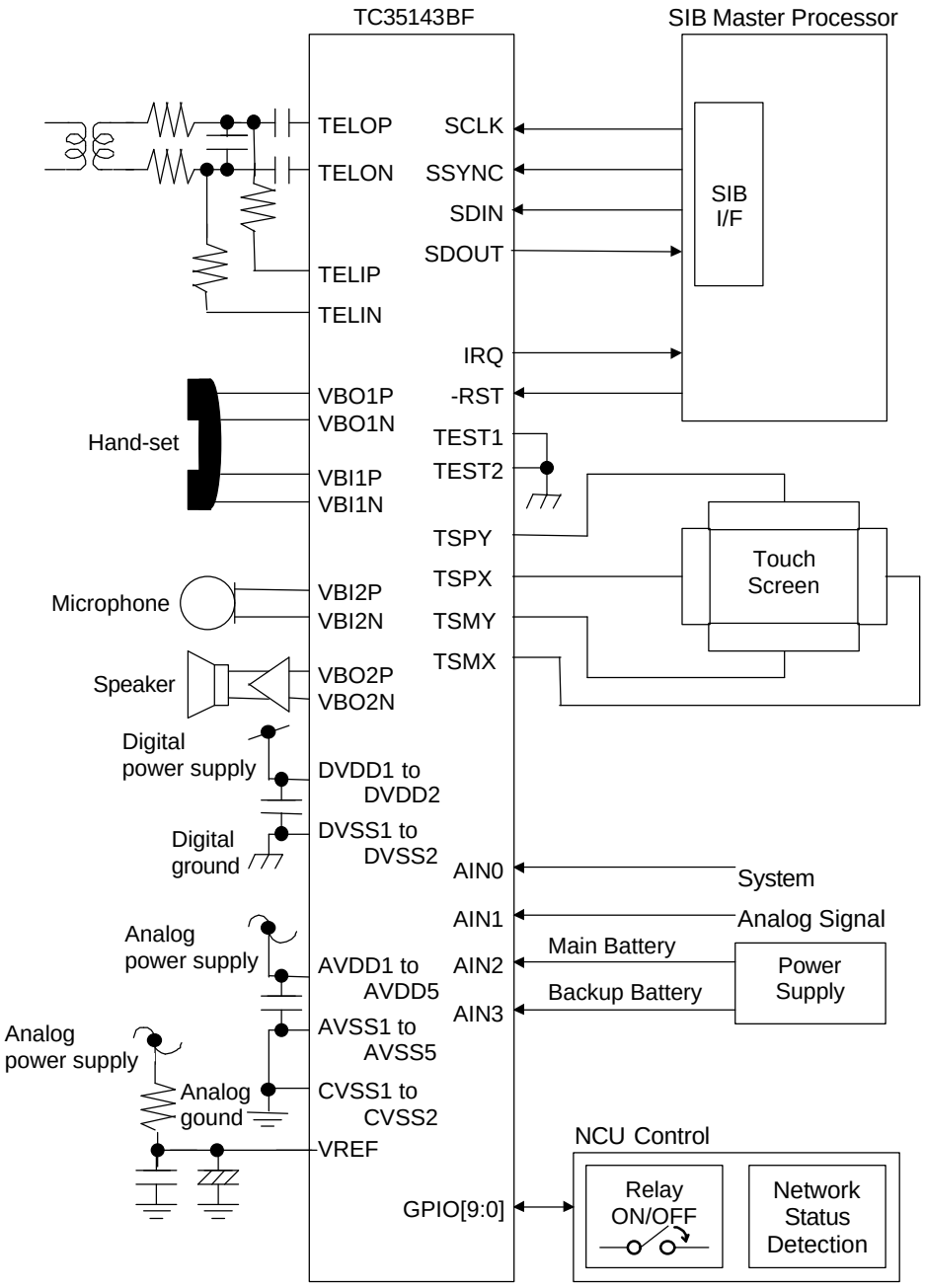


Figure 5.1.A System construction

5.2 Hardware Reset

TC35143BF should be reset, after power on. To reset TC35143BF, -RST terminal should be kept low level for at least 20 ns. The reset execution is performed asynchronously. After 6 periods of SCLK from -RST release, the internal reset is released. Figure 5.2.A shows the timing at which the hardware reset is released.

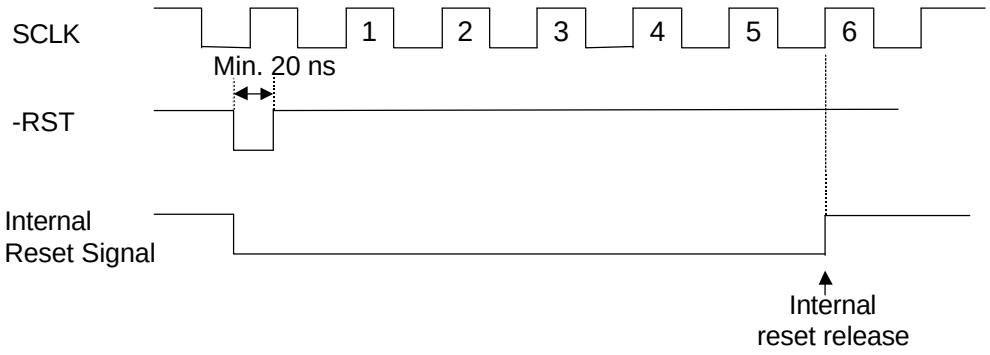


Figure 5.2.A Hardware reset timing

After reset, all the internal registers are set default value and all the terminal are set the default status.. The default value of registers is show in the resister map. The default status of the terminals are shown in the pin description table.

Set TC35143BF register after at least one frame has passed since the release of the reset. See 5.4.2 Interface Timing for frame timing.

5.3 Power-down Control

Figure 5.3.A shows the power-down system of the TC35143BF. Since the analog circuits in the Telecom, Voice, and Touch Screen blocks can be enabled or disabled for each input/output path, sophisticated power-down control is possible. All these settings are made by controlling the internal registers. For details, refer to the explanation of registers in each block. If all analog blocks are disabled, the reference voltage circuit also stops supplying the reference voltage to those blocks.

The reference voltage can be selected between the internal and external sources. The EXREFENA [W:A:5] bit is used for this selection. If you want to use the internal reference voltage, set EXREFENA to 0. In this case, insert a 10 μF capacitor between the analog GND and the VREF pin and also a 33 kΩ resistor between the analog Vdd and the VREF pin. Furthermore, when using the internal reference voltage, allow a period of at least 0.5 seconds before the analog block can be enabled immediately after power-on, as shown in Figure 5.3.A. As long as the power is supplied after this time on, there is no need to insert such a wait state. This wait state only needs to be inserted immediately after power-on. When using an external reference voltage, set EXREFENA to 1. In this case, the wait state of 0.5 seconds or more that is required when using the internal reference voltage is unnecessary. Note also that when an external reference power supply is connected directly to the VREF pin, an input leakage current of about 75 μA (max) flows in it. For applications such as HPC and portable information terminals which require the current consumption to be suppressed to a minimum, make sure the external reference voltage is not applied to the device during power-down state (all functions stopped) by, for example, inserting a switch external to the chip.

Power-down control of the digital unit is accomplished by turning SCLK , SSYNC and SDIN off. These clocks can be turned off only when all function blocks of the TC35143BF are disabled. Do not turn off those clocks if one block is enabled at least.

In addition, TC35143BF has feedback-type analog circuits. These circuits require at least 1 ms of idling from startup to when their operations stabilize. TC35143BF invalidates request flags to receive data until internal operations stabilize. Data can therefore not be received for a minimum of 1 ms from enable setting by the enable bit. For this 1 ms interval connect SCLK before carrying out input.

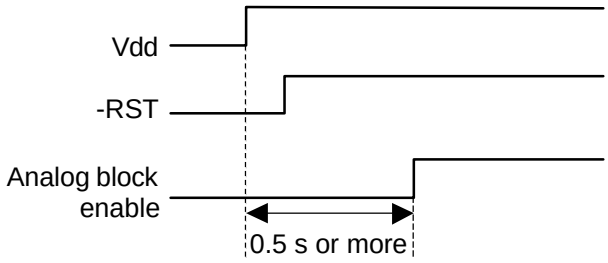


Figure 5.3.A Timing at Which the Analog Block is Enabled Immediately After Power-on

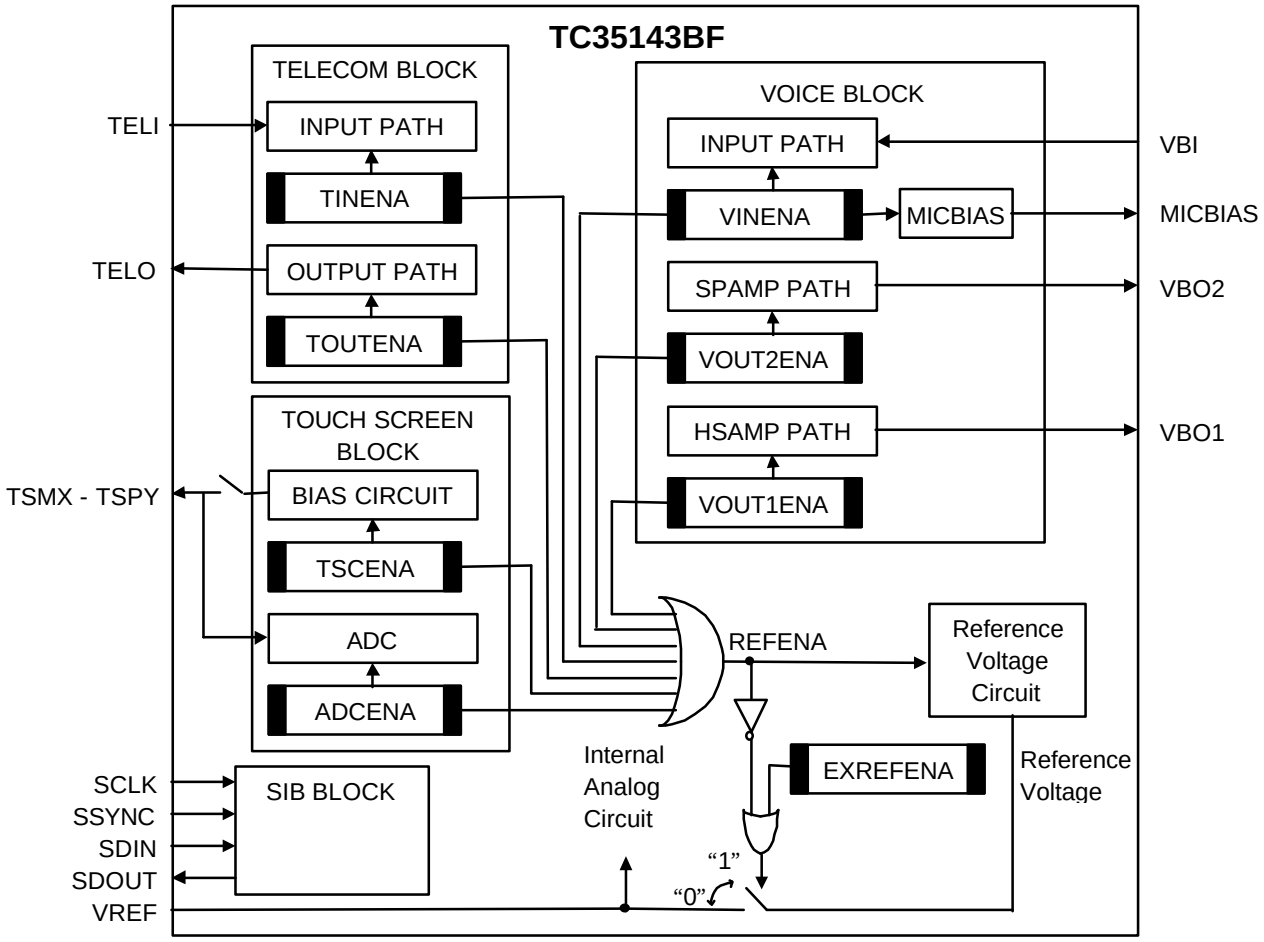


Figure 5.3.B Power-down system

5.4 Serial Interface

The TC35143BF's serial interface is mostly based on SIB interface standards, so it can be connected directly to the SIB master chip. Use of the SIB allows the master chip to communicate with multiple slave devices. Figure 5.4.A shows an example of a device connection.

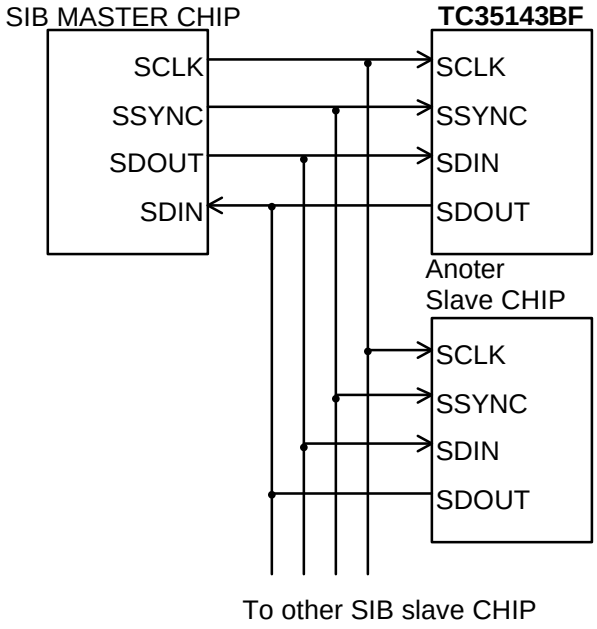


Figure 5.4.A Example of connection for some SIB devices

5.4.1 Pin Function

The following explains the TC35143BF's pin functions related to the SIB interface.

SDIN : This pin is used to receive the serial data sent from the SIB master chip.

SDOUT : This pin outputs the serial data that is sent to the SIB master chip.

SCLK : This pin is used to receive the serial clock supplied from the SIB master chip. Input a 9.216 MHz clock to this pin. The permissible deviation of the clock frequency is 100 ppm and of the duty rate is 45 % to 55 %.

SSYNC : This is a 72 kHz frame synchronizing signal supplied from the SIB master chip. This signal is driven high (= 1) for one SCLK cycle prior to each frame.

IRQ : This pin outputs the interrupt request signal that is sent to the SIB master chip.

5.4.2 Interface Timing

The SIB transfer method is synchronous, with data transferred in units of frames. Operations between the SIB master chip and SIB slave chips are synchronized using a frame sync signal. Figure 5.4.B shows a timing chart.

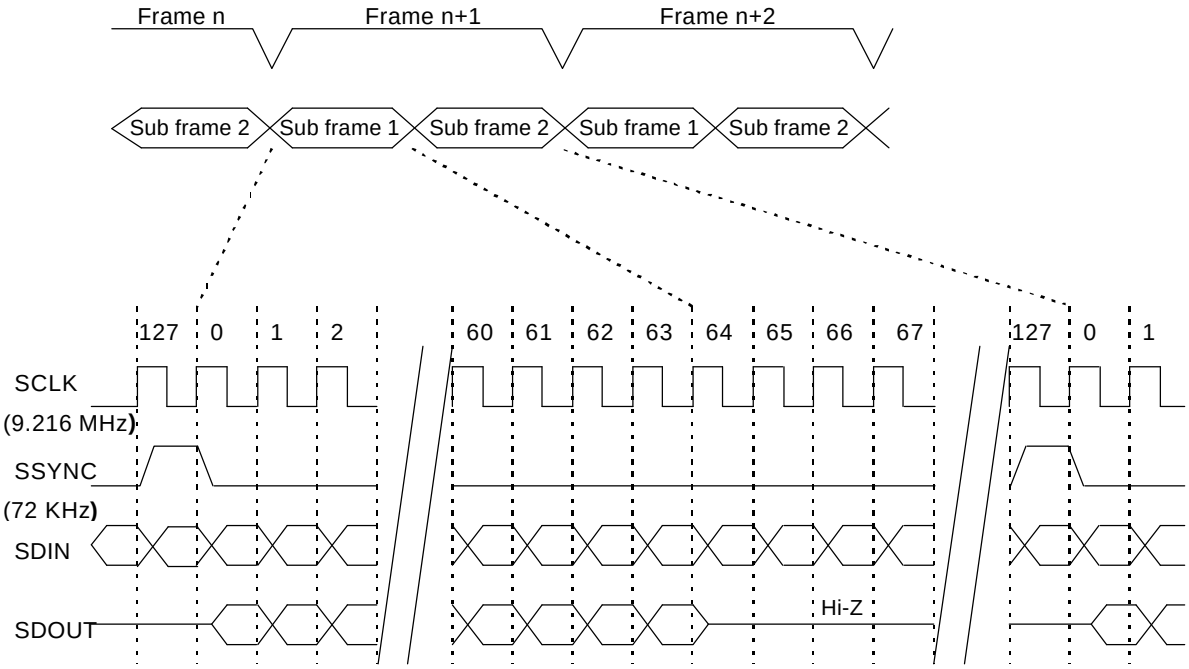


Figure 5.4.B Serial Interface Timing

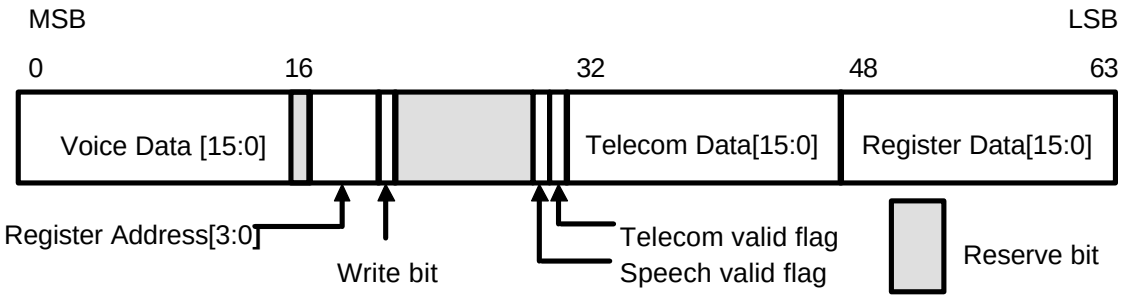
One frame of data consists of 128 bits. A frame is divided into two subframes, each consisting of 64 bits. The TC35143BF uses subframe 1 to communicate with the master device. The TC35143BF latches the SDIN data into its internal circuit synchronously with falling edges of SCLK. It outputs the SDOUT data synchronously with rising edges of SCLK. SSYNC is a frame synchronizing signal which is driven high (= 1) for a duration of the last bit of each frame. The TC35143BF uses SSYNC and a SCLK counter to synchronize the frames being transferred. For details about the AC timing specifications of SCLK, SDIN, and SDOUT, refer to Section 6.4, "A.C. Characteristics."

In a multi-chip configuration, use subframe 2 for other slave devices to communicate with the master device. The TC35143BF uses subframe 1 to communicate with the master device as described above. To prevent the SDOUT outputs of multiple chips from conflict, make sure that when other slave device is communicating, TC35143BF has its SDOUT placed in the high-impedance state. Furthermore, in cases where only one TC35143BF is connected to the master device, make sure the SDOUT output level is fixed low for a duration of subframe 2 to prevent it from being left open. Use a control register to set the status of the SDOUT pin during a subframe 2 period. For details, refer to the description of the SIFZERO [W:1:15] bit of general-purpose I/O port in Section 5.6.

For any one of the function blocks to be operated, SCLK and SSYNC must be input. Note that interrupt output signals are generated regardless of whether SCLK is input.

5.4.3 SIB Data Format

Figure 5.4.C shows the data format of SIB subframe 1 in the TC35143BF. The SDIN frame represents the frames input to the TC35143BF. The SDOUT frame represents the frames output by the TC35143BF.



Frame Bit	SDIN Field Definition	SDOUT Field Definition
[0:15]	Voice DAC Data (16 bits) ; Bit[0]=MSB	Voice ADC Data (16 bits) ; Bit[0]=MSB
[17:20]	Register Address (4 bits) ; Bit[17]=MSB	Register Address (4 bits) ; Bit[17]=MSB
[21]	Write Bit (Write=1)	Must write to 0
[30]	Voice Valid DAC Sample Flag	Voice Valid ADC Flag
[31]	Telecom Valid DAC Sample Flag	Telecom Valid ADC Flag
[32:47]	Telecom DAC Data (16 bits) ; Bit[32]=MSB	Telecom ADC Data (16 bits) ; Bit[32]=MSB
[48:63]	Register Data (16 bits) ; Bit[48]=MSB	Register Data (16 bits) ; Bit[48]=MSB

Supplement 1) The reserved bits are handled as follows:

SDIN frame : All bits must be filled with 0s.

SDOUT frame : The TC35143BF always outputs a logic 0 to the reserved bits.

Supplement 2) Since the ADC/DAC's conversion accuracy is 14 bits, the 2 least significant bits of the Speed Data field are handled as follows:

SDIN frame : The TC35143BF ignores the 2 least significant bits.

SDOUT frame : The TC35143BF outputs an indeterminate state for the 2 least significant bits.

Figure 5.4.C Sub frame format

The SIB subframe is comprised of three data fields and handshaking flags. The DAC data in the Voice and Telecom units is transferred from the SIB master processor to the TC35143BF using the SDIN frame. Similarly, the ADC data in the Voice and Telecom units is transferred from the TC35143BF to the SIB master processor using the SDOUT frame. The valid flags are used to transfer sample data. For details about the transfer procedure and timing, refer to Section 5.5.

The 16 bits wide control register field, not just the control and status bits, includes the data bits used to transfer the sample data of the internal 10-bit ADC. For details about the 10-bit ADC's data transfer procedure, refer to Section 5.11. There are 16 control registers for the SDIN and the SDOUT frames each. The SDIN frame's address field is used to choose the register type. For details about the register types and functions, refer to Sections 5.5 and 5.6. The SDIN frame's Write bit is used for handshaking of the control registers. For details about the handshaking procedure and timing, refer to Section 5.4.4.

5.4.4 Handshaking Procedure for the Control Register Field

The SDIN frame's Write bit is used for the handshaking of control registers. Figure 5.4.D shows the update timing of the internal register. For reading from the register, a master processor sets the desired address and at the same time sets the Write bit to “0”. TC35143BF sets a register data corresponds to a address into output buffer at the SCLK falling edge of bit 47 after recognizing write bit = “0”. The buffer data is output from the SDOUT pin into the SDOUT stream from bit 48. Simultaneously in the frame whose Write bit = “0”, the control data field of the SDIN stream is ignored, so an internal input register is not updated.

For writing to the register, set the Write bit to “1”. At this time, a master processor sets the address and a control data simultaneously. TC35143BF internal control register are updated at the SCLK rising edge of bit 64 after recognizing write bit = “1”. This means that the control data field of SDOUT stream in subframe 1 whose Write bit = “1” is the data immediately before being updated.

The address of SDIN stream is output from SDOUT stream directly.

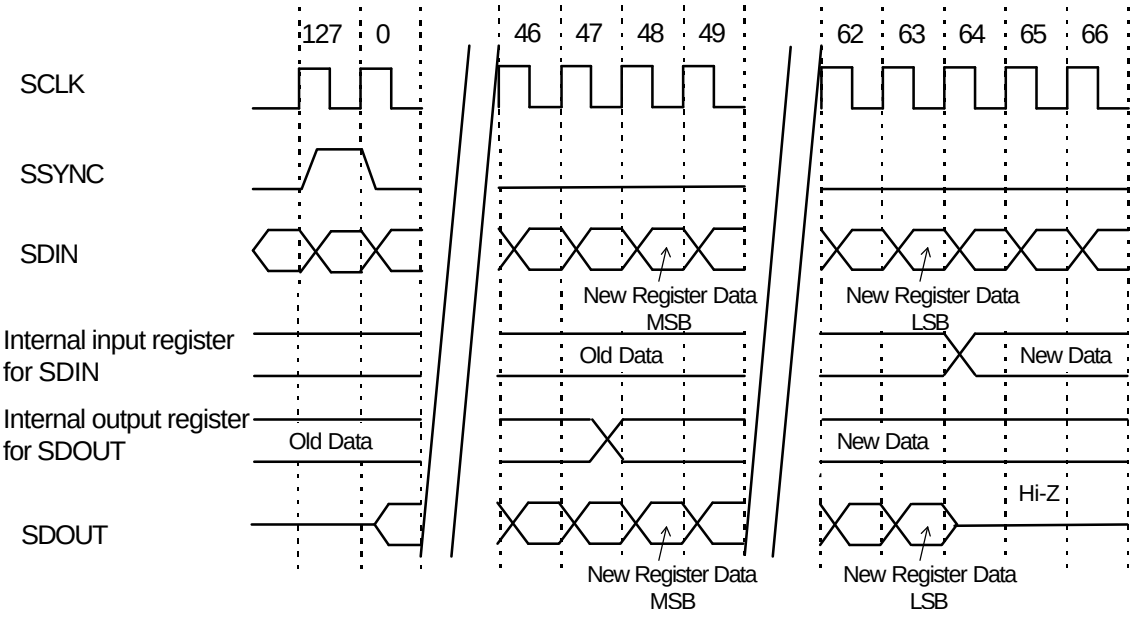


Figure 5.4.D Control register up-date timing during subframe 1

5.5 Line and Voice Interface Sample Data Handshake

Figure 5.5.A shows the ADC and DAC sampling clock generating circuits in the Voice and Telecom blocks. Figure 5.5.B shows sampling clock timing diagrams. The sampling clocks can be set independently for the Telecom and Voice blocks. Use TDIV [W:5:6-0] and VDIV [W:7:6-0] for this setting. For details on how to set, refer to the chapters where the Telecom and Voice blocks are described. The host processor first sets the desired sampling frequencies to TDIV and VDIV. Then it enables the required circuit blocks. The sample counter starts counting after the circuit blocks are enabled. The sample counter counts up the 288 kHz clock derived from SCLK until the values set by TDIV and VDIV are reached. If the settings of TDIV or VDIV are changed in the middle of counting, the clock generation gets out of synchronization, resulting in an underwrite or underread of data. Therefore, be sure to disable the circuit blocks before changing the settings of sampling frequencies. Then, after setting the sampling frequencies, renewable the circuit blocks.

When the sample counter has completed one count up, the sampling pulse is toggled twice. It is synchronized to the sampling pulse, and the data request flag (valid flag) for receiving data becomes invalid.

The Telecom and Voice data are communicated with an SIB master processor using a flag called the "valid flag." If an SIB master processor has the same sample counter of TC35143BF, the data communication is possible by only using valid flag.

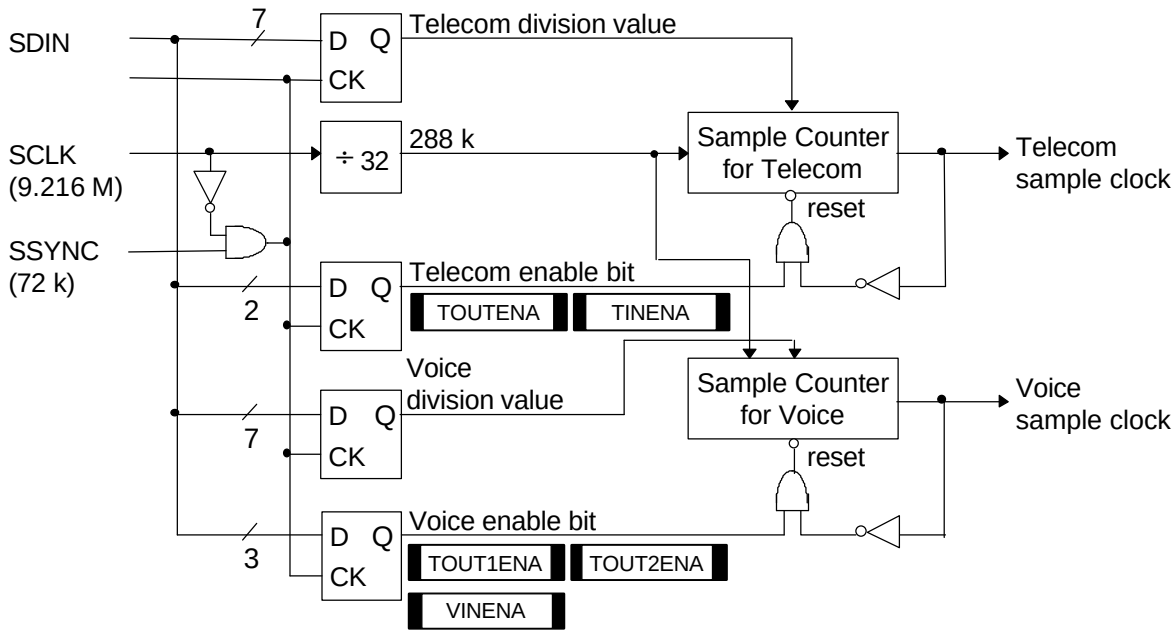


Figure 5.5.A Sampling clock generator

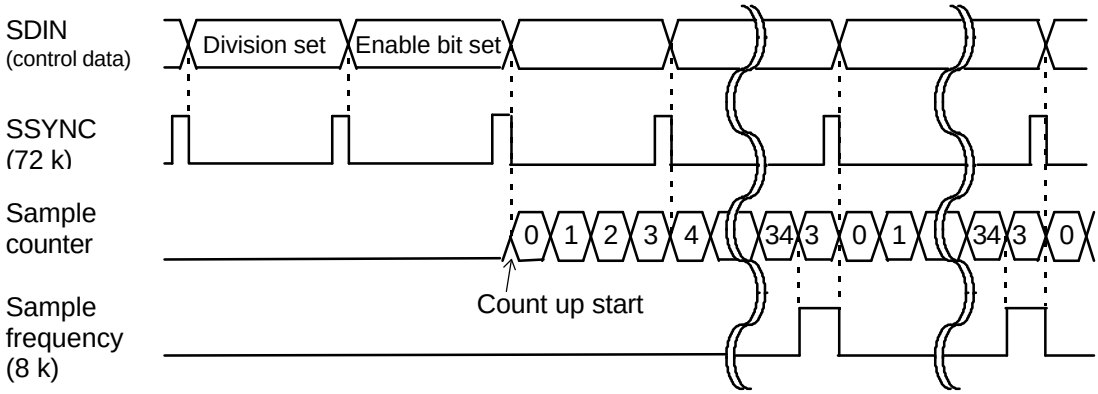


Figure 5.5.B Sampling clock timing example
(Division value=24h, Sampling frequency = 8 kHz)

5.5.1 Voice and Telecom Input Data Transfer Timings

Figure 5.5.C shows ADC data handshaking timing for the Voice and Telecom input signals. Shown in this diagram are examples where the sampling frequency in the Telecom unit is set to 8 kHz (TDIV = 24h) and that in the Voice unit is set to 22.15 kHz (VDIV = Dh).

The ADC data handshaking basically is accomplished by using the valid flag. The valid flag is provided individually for the Telecom and Voice units. These valid flags are fixed to 0 when the corresponding input path is disabled. For example, if the Telecom input path is disabled (using the TINENA bit), tel_valid flag does not turn on. Also, even when the input path is enabled, these flags indicate a 0 until the first converted data is prepared.Specifically, after enable setting, the valid flag becomes valid after the 65SSYNC interval (approximately 1 ms) has passed.

The valid flag has two operation modes. The DFLGENA [W:D:12] is used to set the modes. If DFLGENA is 0, the valid flag is always 1 in a subframe in which the ADC data is output from the SDOUT stream. The Telecom and Voice valid flags both behave in the same way. If DFLGENA is 1, the Telecom and Voice valid flags behave a little differently. The Telecom valid flag is set to 1 in only the subframe immediately after the Telecom data field in SDOUT stream is updated to new data. Although the data in the SDOUT stream itself remains valid until the data is updated to the next sample data, the valid flag indicates a 0. The Voice valid flag is set to 1 in only the subframe immediately before the Voice data field in SDOUT stream is updated to new data. Although the valid flag indicates a 0 before it is set to 1 after the data is updated to new sample data, the data in the SDOUT stream itself is valid.

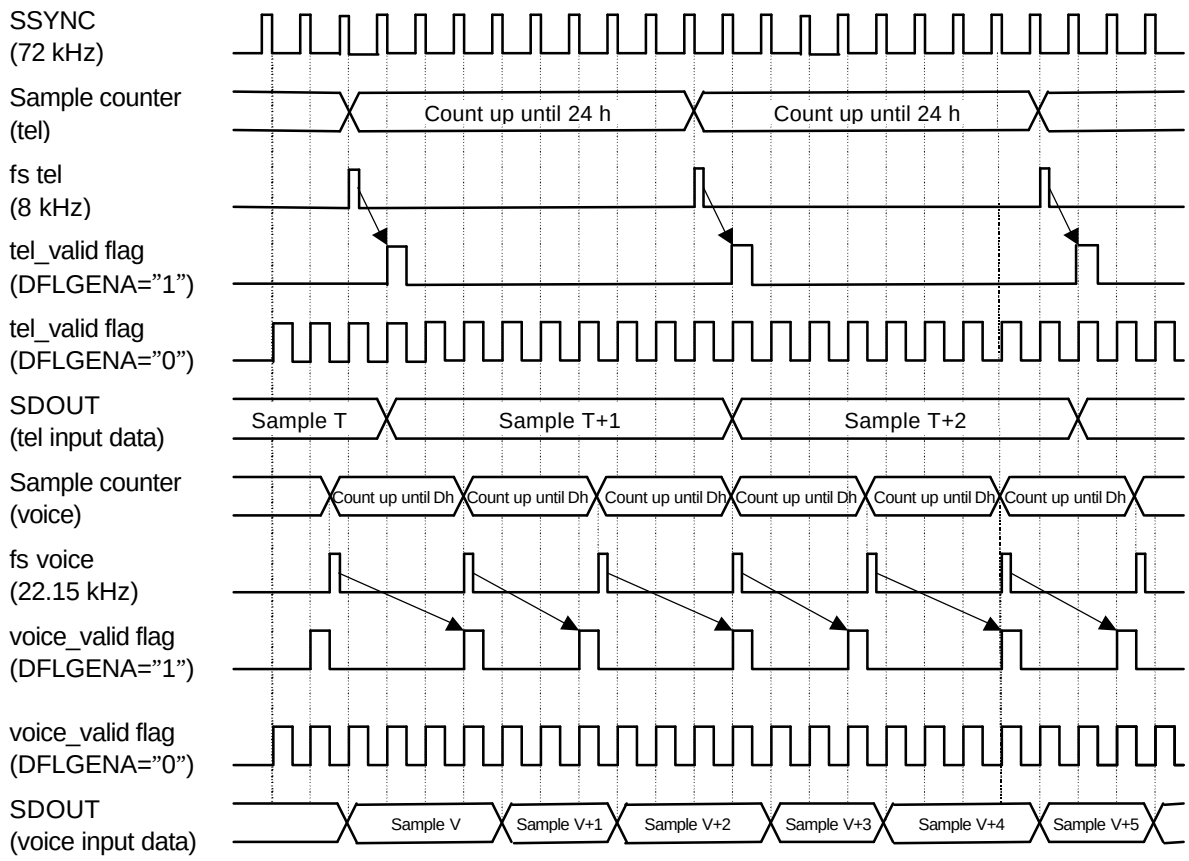


Figure 5.5.C ADC data transfer timing

The host processor normally sets DFLGENA to 1 and receives the ADC data synchronously with the valid flag = 1. If a master processor uses a timer or a counter synchronizes with SCLK as handshake trigger, the data handshaking can be accomplished without monitoring the valid flags. Table 5.5.A shows the registers that contain the DFLGENA bit.

Table 5.5.A Mode Register (Address D)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15 to 14	W	RESERVED	These are spare bits. Set them to 00b.	0
	R	RESERVED	These are spare bits. They indicate a 0.	0
13	W	VOFFCAN	This bit enables or disables the offset canceler of the Speech input unit. 0: Disabled. 1: Enabled.	0
	R	VOFFCAN	This bit indicates status of whether the offset canceler of the Speech input unit is enabled or disabled. 0: Disabled. 1: Enabled.	0
12	W	DFLGENA	This bit sets the display mode of the valid flag in the SDOUT frame. 0: Static mode. 1: Dynamic mode.	0
	R	DFLGENA	This bit indicates the setup display mode of the valid flag in the SDOUT frame. 0: Static mode. 1: Dynamic mode.	0
11	W	RESERVED	This is a spare bit. Set it to 0.	0
	R	RESERVED	This is a spare bit. This indicates a 0.	0
10 to 8	W	VCOF[2:0]	These bits select the frequency response of the Voice interface's digital filter. Choose the filter characteristic according to the sampling frequency. For the setup contents, see the table below. For details about filter characteristics, refer to 5.10.3. **Voice interface sampling frequency** / **VCOF[2:0]** 8 kHz / 001b 11.08 kHz / 001b 16 kHz / 100b 22.15 kHz / 100b (Note) Do not set any other code.	1
	R	VCOF[2:0]	These bits show the selected frequency response settings of the Voice interface's digital filter. For the contents of setup code, refer to the explanation of the write register above.	1
7 to 0	W	RESERVED	These are spare bits. Set them to 0.	0
	R	RESERVED	These are spare bits. They indicate a 0.	0

5.5.2 Voice and Telecom Output Data Transfer Timings

Figure 5.5.D shows DAC data handshaking timings for the Voice and Telecom output signals. Shown in this diagram are examples where the sampling frequency in the Telecom unit is set to 8 kHz (TDIV = 24h) and that in the Voice unit is set to 22.15 kHz (VDIV = Dh).

The DAC data handshaking is accomplished by using the valid flag. The valid flag is provided individually for the Telecom and Voice units. Unlike for the ADC data, the Telecom and Voice valid flags behave in the same way. Also, a register bit to set the operation modes (a bit equivalent to DFLGENA) is not provided.

If the output block is disabled, the TC35143BF does not output the corresponding analog signal even when the valid flag is 1. When the output block is enabled, the data in the frame whose valid flag = 1 is taken in and is output from the analog pins after being converted by the DAC. The data in the frames whose valid flag = 0 are not taken in.However, after enable setting, the valid flag is invalid for the 65SSYNC interval (approximately 1 ms) until operation of the analog circuit stabilizes, so please wait.

The host processor prepares an SCLK-synchronized timer or counter to synchronize its operation with the TC35143BF's sampling timing. The host processor sets the valid flag to 1 and at the same time writes the sample data into the data field of the SDIN stream before the next sampling timing as shown below. Since the TC35143BF does not take in data from the frames whose valid flag = 0, there will be no problem even when some data is written into those frames by the host processor.

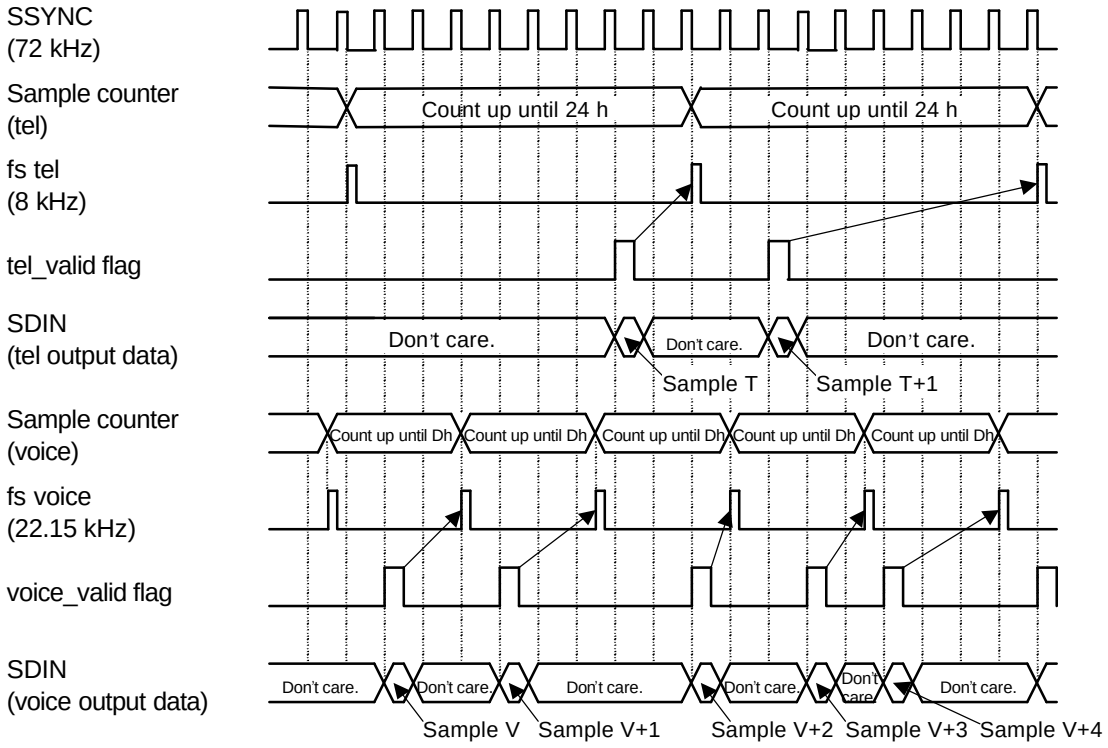


Figure 5.5.D Example of DAC data transfer timing

5.6 Control Register

The TC35143BF has a 16 bits wide register field that is controlled via the SIB interface. The register field for the data (SDIN) that is input from the SIB master chip to the TC35143BF is called the "write" register. The register field for the data (SDOUT) that is output from the TC35143BF to the SIB master chip is called the "read" register. There are 16 register addresses for read and write each. Most bits at the same positions in the write and the read registers have the same effect, but some bits have different effects.

The SIB master chip controls the TC35143BF by writing and reading to and from the write and read registers. Since write and read to and from these registers are performed on one address at a time, note that even when rewriting one bit, data is written to all other bits at the same address also. The bit positions are described as follows:

FORMAT:[W/R : ADDRESS : BIT]	W/R	W (Write) or R (Read)
	ADDRESS	0 to F (Hex-Decimal)
	BIT	0 (LSB) to 15 (MSB)

Example: The Telecom interface's loop test control bit is located at bit 7 of write register 5. Therefore, this bit is described as follows (see Tables 5.6.B to E for register maps):

TLOOP [W : 5 : 7]

The control registers described above are outlined in Table 5.6.A .

Table 5.6.A TC35143BF Control Register

ADDRESS	R/W	Symbol	Description
0H	W	IODAT	**I/O port data :** Control register for I/O port output level
	R	IODAT	**I/O port data :** I Status register for I/O port level
1H	W	IODIR	**I/O port direction:** Control register for I/O port input/output direction
	R	IODIR	**I/O port direction :** Status register for I/O port input/output direction
2H	W	RISINT	**Rising edge interrupt:** Setting register for rising edge trigger of interrupt factors
	R	RISINT	**Rising edge interrupt:** Status register for rising edge trigger of interrupt factors
3H	W	FALINT	**Falling edge interrupt:** Setting register for falling edge trigger of interrupt factors
	R	FALINT	**Falling edge interrupt:** Setting register for falling edge trigger of interrupt factors
4H	W	INTCLR	**Interrupt clear:** Setting register for interrupt clear
	R	INTCLR	**Interrupt status:** Status register for interrupt factors
5H	W	TELA	**Telecom control A:** Setting register for sampling frequency of telecom part
	R	TELA	**Telecom control A:** Status register for sampling frequency of telecom part
6H	W	TELB	**Telecom control B:** Control register for telecom part
	R	TELB	**Telecom control B:** Status register for telecom part control
7H	W	VOICEA	**Voice control A:** Setting register for sampling frequency of voice part
	R	VOICEA	**Voice control A:** Status register for sampling frequency of voice part
8H	W	VOICEB	**Voice control B:** Control register for voice part
	R	VOICEB	**Voice control B:** Status register for voice part control
9H	W	TSC	**Touch screen:** Control register for touch screen
	R	TSC	**Touch screen:** Status register for touch screen control
AH	W	ADC	**ADC control:** Control register for 10 bit ADC
	R	ADC	**ADC control:** Status register for 10 bit ADC control

BH	W	RSV	**Reserved**
	R	ADCDAT	**ADC data:** Data register of 10 bit ADC
CH	W	RSV	**Reserved**
	R	DATE	**DATE:** Indicates development date
DH	W	MODE	**Mode:** Sets the operation mode.
	R	MODE	**Mode:** Indicates the setup state of operation mode.
EH	W	RSV	**Reserved**
	R	RSV	**Reserved**
FH	W	RSV	**Reserved**
	R	RSV	**Reserved**

5.6.1 Write Register Map

Table 5.6.B and Table 5.6.C show the Write Register maps. Bit width is 16. Table 5.6.B shows the upper 8bits and Table 5.6.C shows lower 8bits. Description of each bit is described in after section 5.7.

Table 5.6.B TC35143BF Write Register Map (Higher Bits)

ADD-RESS	BIT CONTENTS								MNEMONIC
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	
0 H	IRQACT	-	-	-	-	-	IODAT9	IODAT8	IODAT
	0	0	0	0	0	0	0	0	
1 H	SIFZERO	-	-	-	-	-	IODIR9	IODIR8	IODIR
	0	0	0	0	0	0	0	0	
2 H	ACRINT	TCRINT	MXRINT	PXRINT	ADCRINT	-	IORINT9	IORINT8	RISINT
	0	0	0	0	0	0	0	0	
3 H	ACFINT	TCFINT	MXFINT	PXFINT	ADCFINT	-	IOFINT9	IOFINT8	FALINT
	0	0	0	0	0	0	0	0	
4 H	ACICLR	TCICLR	MXICLR	PXICLR	ADCICLR	-	IOICLR9	IOICLR8	INTCLR
	0	0	0	0	0	0	0	0	
5 H	TCOF2	TCOF1	TCOF0	-	-	-	-	-	TELA
	0	0	1	0	0	0	0	0	
6 H	TOUTENA	TINENA	TMUTE	TECGAIN	TECENA	-	-	TGAIN	TELB
	0	0	0	0	0	0	0	0	
7 H	VINSEL1	VINSEL0	VOUT2ENA	VGAIN1	VGAIN0	VAMP3	VAMP2	VAMP1	VOICEA
	0	0	0	0	0	0	0	0	
8 H	VOUT1ENA	VINENA	VADMUTE	VHSMUTE	VHSATT2	VHSATT1	VHSATT0	VLOOP	VOICEB
	0	0	0	1	0	0	0	0	
9 H	-	-	-	-	TSCENA	-	TSCMOD1	TSCMOD0	TSC
	0	0	0	0	0	0	0	0	
A H	ADCENA	-	-	-	-	-	-	-	ADC
	0	0	1	0	0	1	0	1	
B H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
C H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
D H	-	-	VOFFCAN	DFLGENA	-	VCOF2	VCOF1	VCOF0	MODE
	0	0	0	0	0	0	0	1	
E H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
F H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	

(Note) Upper : BIT Mnemonic, Lower : default value, - : reserved

Table 5.6.C TC35143BF Write Register Map (Lower Bits)

ADD-RESS	BIT CONTENTS								MNEMONIC
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0 H	IODAT7	IODAT6	IODAT5	IODAT4	IODAT3	IODAT2	IODAT1	IODAT0	IODAT
	0	0	0	0	0	0	0	0	
1 H	IODIR7	IODIR6	IODIR5	IODIR4	IODIR3	IODIR2	IODIR1	IODIR0	IODIR
	0	0	0	0	0	0	0	0	
2 H	IORINT7	IORINT6	IORINT5	IORINT4	IORINT3	IORINT2	IORINT1	IORINT0	RISINT
	0	0	0	0	0	0	0	0	
3 H	IOFINT7	IOFINT6	IOFINT5	IOFINT4	IOFINT3	IOFINT2	IOFINT1	IOFINT0	FALINT
	0	0	0	0	0	0	0	0	
4 H	IOICLR7	IOICLR6	IOICLR5	IOICLR4	IOICLR3	IOICLR2	IOICLR1	IOICLR0	INTCLR
	0	0	0	0	0	0	0	0	
5 H	TLOOP	TDIV6	TDIV5	TDIV4	TDIV3	TDIV2	TDIV1	TDIV0	TELA
	0	0	1	0	0	1	0	0	
6 H	TAMP2	TAMP1	TAMP0	TCLPCLR	THPFENA	-	-	-	TELB
	0	0	0	0	0	0	0	0	
7 H	VAMP0	VDIV6	VDIV5	VDIV4	VDIV3	VDIV2	VDIV1	VDIV0	VOICEA
	0	0	1	0	0	1	0	0	
8 H	VDAMUTE	VCLPCLR	VSPMUTE	VDAATT1	VDAATT0	VSPATT2	VSPATT1	VSPATT0	VOICEB
	0	0	1	0	0	0	0	0	
9 H	TSPYGND	TSMYGND	TSPXGND	TSMXGND	TSPYPOW	TSMYPOW	TSPXPOW	TSMXPOW	TSC
	0	0	0	0	0	0	0	0	
A H	ADCSTART	-	EXREFENA	ADCIN2	ADCIN1	ADCIN0	-	ADSYNCENA	ADC
	0	0	0	0	0	0	0	0	
B H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
C H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
D H	-	-	-	-	-	-	-	-	MODE
	0	0	0	0	0	0	0	0	
E H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
F H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	

(Note) Upper : BIT Mnemonic, Lower : default value, - : reserved

5.6.2 Read Register Map

Table 5.6.D and Table 5.6.E show the Read Register maps. The bit width is 16. Table 5.6.D shows upper 8bit and Table 5.6.E shows lower 8bit. Description of each bit is described in after section 5.7.

Table 5.6.D TC35143BF Read Register Map (Higher Bits)

ADD-RESS	BIT CONTENTS								MNEMONIC
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	
0 H	IRQACT	-	-	-	-	-	IODAT9	IODAT8	IODAT
	0	0	0	0	0	0	*	*	
1 H	SIFZERO	-	-	-	-	-	IODIR9	IODIR8	IODIR
	0	0	0	0	0	0	0	0	
2 H	ACRINT	TCRINT	MXRINT	PXRINT	ADCRINT	-	IORINT9	IORINT8	RISINT
	0	0	0	0	0	0	0	0	
3 H	ACFINT	TCFINT	MXFINT	PXFINT	ADCFINT	-	IOFINT9	IOFINT8	FALINT
	0	0	0	0	0	0	0	0	
4 H	ACINTST	TCINTST	MXINTST	PXINTST	ADCINTST	-	IOINTST9	IOINTST8	INTSTAT
	0	0	0	0	0	0	0	0	
5 H	TCOF2	TCOF1	TCOF0	-	-	-	-	-	TELA
	0	0	1	0	0	0	0	0	
6 H	TOUTENA	TINENA	TMUTE	TECGAIN	TECENA	-	-	TGAIN0	TELB
	0	0	0	0	0	0	0	0	
7 H	VINSEL1	VINSEL0	VOUT2ENA	VGAIN1	VGAIN0	VAMP3	VAMP2	VAMP1	VOICEA
	0	0	0	0	0	0	0	0	
8 H	VOUT1ENA	VINENA	VADMUTE	VHSMUTE	VHSATT2	VHSATT1	VHSATT0	VLOOP	VOICEB
	0	0	0	1	0	0	0	0	
9 H	-	-	TSMXLOW	TSPXLOW	TSCENA	-	TSCMOD1	TSCMOD0	TSC
	0	0	0	0	0	0	0	0	
A H	ADCENA	-	-	-	-	-	-	-	ADC
	0	0	1	0	0	1	0	1	
B H	ADCVAL	ADCDAT9	ADCDAT8	ADCDAT7	ADCDAT6	ADCDAT5	ADCDAT4	ADCDAT3	ADCDAT
	1	*	*	*	*	*	*	*	
C H	DATE15	DATE14	DATE13	DATE12	DATE11	DATE10	DATE9	DATE8	DATE
	1	0	0	1	0	1	1	1	
D H	-	-	VOFFCAN	DFLGENA	-	VCOF2	VCOF1	VCOF0	MODE
	0	0	0	0	0	0	0	1	
E H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
F H	-	-	-	-	-	-	-	-	RSV
	1	1	1	1	1	1	1	1	

(Note) Upper : BIT Mnemonic, Lower : default value, - : reserved, * : undefined

Table 5.6.E TC35143BF Read Register Map (Lower Bits)

ADD-RESS	BIT CONTENTS								MNEMONIC
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
0 H	IODAT7	IODAT6	IODAT5	IODAT4	IODAT3	IODAT2	IODAT1	IODAT0	IODAT
	*	*	*	*	*	*	*	*	
1 H	IODIR7	IODIR6	IODIR5	IODIR4	IODIR3	IODIR2	IODIR1	IODIR0	IODIR
	0	0	0	0	0	0	0	0	
2 H	IORINT7	IORINT6	IORINT5	IORINT4	IORINT3	IORINT2	IORINT1	IORINT0	RISINT
	0	0	0	0	0	0	0	0	
3 H	IOFINT7	IOFINT6	IOFINT5	IOFINT4	IOFINT3	IOFINT2	IOFINT1	IOFINT0	FALINT
	0	0	0	0	0	0	0	0	
4 H	IOINTST7	IOINTST6	IOINTST5	IOINTST4	IOINTST3	IOINTST2	IOINTST1	IOINTST0	INTSTAT
	0	0	0	0	0	0	0	0	
5 H	TLOOP	TDIV6	TDIV5	TDIV4	TDIV3	TDIV2	TDIV1	TDIV0	TELA
	0	0	1	0	0	1	0	0	
6 H	TAMP2	TAMP1	TAMP0	TCLPST	THPFENA	-	-	-	TELB
	0	0	0	0	0	0	0	0	
7 H	VAMP0	VDIV6	VDIV5	VDIV4	VDIV3	VDIV2	VDIV1	VDIV0	VOICEA
	0	0	1	0	0	1	0	0	
8 H	VDAMUTE	VCLPST	VSPMUTE	VDAATT1	VDAATT0	VSPATT2	VSPATT1	VSPATT0	VOICEB
	0	0	1	0	0	0	0	0	
9 H	TSPYGND	TSMYGND	TSPXGND	TSMXGND	TSPYPOW	TSMYPOW	TSPXPOW	TSMXPOW	TSC
	0	0	0	0	0	0	0	0	
A H	ADCSTART	-	EXREFENA	ADCIN2	ADCIN1	ADCIN0	-	ADSYNCENA	ADC
	0	0	0	0	0	0	0	0	
B H	ADCDAT2	ADCDAT1	ADCDAT0	-	-	-	-	-	ADCDAT
	*	*	*	*	*	*	*	*	
C H	DATE7	DATE6	DATE5	DATE4	DATE3	DATE2	DATE1	DATE0	ID
	0	0	0	1	0	0	1	0	
D H	-	-	-	-	-	-	-	-	MODE
	0	0	0	0	0	0	0	1	
E H	-	-	-	-	-	-	-	-	RSV
	0	0	0	0	0	0	0	0	
F H	-	-	-	-	-	-	-	-	RSV
	1	1	1	1	1	1	1	1	

(Note) Upper : BIT Mnemonic, Lower : default value, - : reserved, * : undefined

5.7 General I/O Ports

Below are the control register for 10 channels general purpose I/O ports. Each I/O port can be controlled individually by these resisters. Since each port is set for the input mode when reset, fix the unused ports to GND or DVDD via a resistor. Never set the unused ports for the output mode because an current could flow in those ports if set for output. There is also a caution to be observed for the ports that are used. When using them as output ports, we recommend to pull them up or down via a resistor because their state immediately after a reset till they are set for output is high impedance.

Table 5.7.A General I/O port data setting register (Address0)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	IRQACT	This bit selects the logical signification of the IRQ terminal. 0: IRQ operates as a high active terminal. 1: IRQ operates as a low active terminal	
	R	IRQACT	This bit indicates the logical signification of the IRQ ternimal. 0: IT means that the IRQ is high active terminal. 1: It means that the IRQ is low active terminal.	
14 to 10	W	RESERVED	These are spare bits. Write a 0 to these bits.	0
	R	RESERVED	These are spare bits. They output a 0.	0
7 to 0	W	IODAT[n] (n=9 to 0)	These bits set the output level of each general-purpose I/O port when the port is directed for output. 0: The general-purpose I/O port outputs a 0. 1: The general-purpose I/O port outputs a 1. (Supplement) The bit numbers and I/O port numbers correspond one for one.	0
	R	IODAT[n] (n=9 to 0)	These bits indicate the input or output level of each I/O port. 0: It means that the input or output level is 0. 1: It means that the input or output level is 1.	0

Table 5.7.B General I/O port direction setting register (Address1)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	SIFZERO	This bit sets the output level of the SDOUT pin during a subframe 2 period. 0: SDOUT is tristated (high impedance). 1: SDOUT is set to 0.	0
	R	SIFZERO	This bit indicates the output level that is set for the SDOUT pin during a subframe 2 period. 0: Indicates that the SDOUT output is tristated. 1: Indicates that the SDOUT output is set to 0.	0
14 to 10	W	RESERVED	These are spare bits. Write a 0 to these bits.	0
	R	RESERVED	These are spare bits. They output a 0.	0
9 to 0	W	IODIR[n] (n=9 to 0)	These bits set the input/output mode of each general-purpose I/O port. 0: The I/O port is set for the input mode. 1: The I/O port is set for the output mode.	0
	R	IODIR[n] (n=9 to 0)	These bits indicate the input/output mode that is set for each general-purpose I/O port. 0: It means that the I/O port is set for the input mode. 1: It means that the I/O port is set for the output mode.	0

5.8 Interrupt

The TC35143BF allows the status of various interrupt sources to be represented by the IRQ pin. When a specified interrupt source became active, its active state is reflected directly in the IRQ pin. A control register is used to specify an interrupt source. By default, all interrupt sources are disabled (inactive). In addition to an interrupt source, it is possible to specify an interrupt trigger, which can be a rising or a falling edge. In either case, a control register is used to set the trigger edge. If several interrupt sources are specified, they are OR'ed before their active state is represented by the IRQ pin.

Tables 5.8.A and 5.8.B show the interrupt sources and edge trigger specifying registers. Once an interrupt source is activated, the asserted interrupt signal must be cleared to allow for the next interrupt to be accepted. The interrupt source is cleared within 200 ns (max) from a low to high transition in the clear register. Clearing takes place at a rising edge of SCLK. After clearing an interrupt, reset the clear register to 0 to allow for the next interrupt to be cleared. An interrupt status register is located at the same address as is the clear register. Table 5.8.C lists the interrupt clear and status registers.

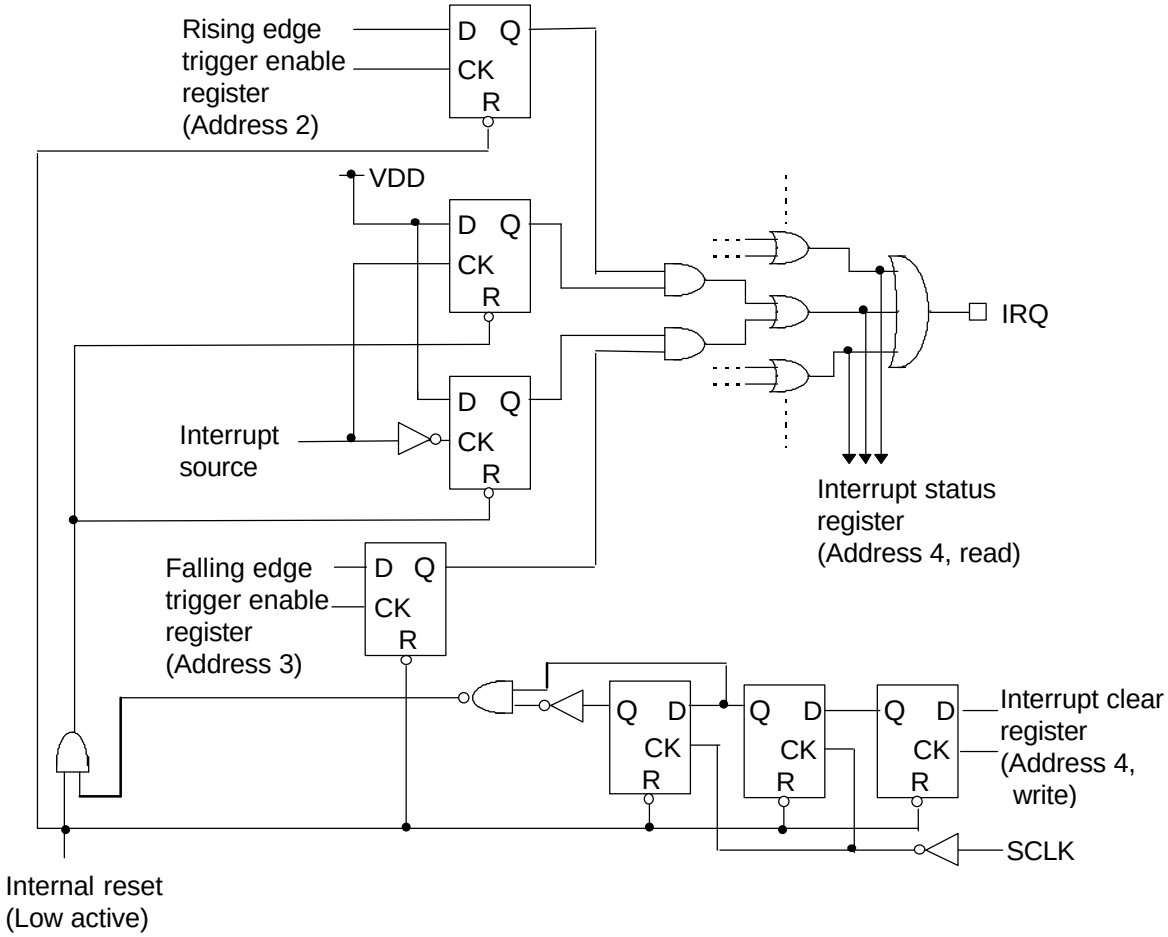


Figure 5.8.A Interrupt block diagram

Table 5.8.A Rising edge interrupt enable register

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	ACRINT	0: The rising-edge trigger of the Speech input clip detection flag is disabled. 1: The rising-edge trigger of the Speech input clip detection flag is enabled.	0
	R	ACRINT	0: Indicates that the rising-edge trigger of the Speech input clip detection flag is disabled. 1: Indicates that the rising-edge trigger of the Speech input clip detection flag is disabled.	0
14	W	TCRINT	0: The rising-edge trigger of the Telecom input clip detection flag is disabled. 1: The rising-edge trigger of the Telecom input clip detection flag is enabled.	0
	R	TCRINT	0: Indicates that the rising-edge trigger of the Telecom input clip detection flag is disabled. 1: Indicates that the rising-edge trigger of the Telecom input clip detection flag is enabled.	0
13	W	MXRINT	0: The falling-edge trigger of the TSMX pin signal is disabled. 1: The falling-edge trigger of the TSMX pin signal is enabled.	0
	R	MXRINT	0: Indicates that the falling-edge trigger of the TSMX pin signal is disabled. 1: Indicates that the falling-edge trigger of the TSMX pin signal is enabled.	0
12	W	PXRINT	0: The falling-edge trigger of the TSPX pin signal is disabled. 1: The falling-edge trigger of the TSPX pin signal is enabled.	0
	R	PXRINT	0: Indicates that the falling-edge trigger of the TSPX pin signal is disabled. 1: Indicates that the falling-edge trigger of the TSPX pin signal is enabled.	0
11	W	ADCRINT	0: The rising-edge trigger for the completion of the 10-bit ADC conversion is disabled. 1: The rising-edge trigger for the completion of the 10-bit ADC conversion is enabled.	0
	R	ADCRINT	0: Indicates that the rising-edge trigger for the completion of the 10-bit ADC conversion is disabled. 1: Indicates that the rising-edge trigger for the completion of the 10-bit ADC conversion is enabled.	0
10	W	RESERVED	This is a spare bit. Write a 0 to it.	0
	R	RESERVED	This is a spare bit. It indicates a 0.	0
9 to 0	W	IORINT[n] (n=9 to 0)	0: The rising-edge trigger of the general-purpose I/O port is disabled. 1: The rising-edge trigger of the general-purpose I/O port is enabled. (Supplement) The bit numbers and I/O port numbers correspond one for one.	0
	R	IORINT[n] (n=9 to 0)	0: Indicates that the rising-edge trigger of the general-purpose I/O port is disabled. 1: Indicates that the rising-edge trigger of the general-purpose I/O port is enabled.	0

Table 5.8.B Falling edge interrupt enable register (Address3)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	ACFINT	0: The falling-edge trigger of the Speech input clip detection flag is disabled. 1: The falling-edge trigger of the Speech input clip detection flag is enabled.	0
	R	ACFINT	0: Indicates that the falling-edge trigger of the Speech input clip detection flag is disabled. 1: Indicates that the falling-edge trigger of the Speech input clip detection flag is enabled.	0
14	W	TCFINT	0: The falling-edge trigger of the Telecom input clip detection flag is disabled. 1: The falling-edge trigger of the Telecom input clip detection flag is enabled.	0
	R	TCFINT	0: Indicates that the falling-edge trigger of the Telecom input clip detection flag is disabled. 1: Indicates that the falling-edge trigger of the Telecom input clip detection flag is enabled.	0
13	W	MXFINT	0: The rising-edge trigger of the TSMX pin signal is disabled. 1: The rising-edge trigger of the TSMX pin signal is enabled.	0
	R	MXFINT	0: Indicates that the rising-edge trigger of the TSMX pin signal is disabled. 1: Indicates that the rising-edge trigger of the TSMX pin signal is enabled.	0
12	W	PXFINT	0: The rising-edge trigger of the TSPX pin signal is disabled. 1: The rising-edge trigger of the TSPX pin signal is enabled.	0
	R	PXFINT	0: Indicates that the rising-edge trigger of the TSPX pin signal is disabled. 1: Indicates that the rising-edge trigger of the TSPX pin signal is enabled.	0
11	W	ADCFINT	0: The falling-edge trigger for the completion of the 10-bit ADC conversion is disabled. 1: The falling-edge trigger for the completion of the 10-bit ADC conversion is enabled.	0
	R	ADCFINT	0: Indicates that the falling-edge trigger for the completion of the 10-bit ADC conversion is disabled. 1: Indicates that the falling-edge trigger for the completion of the 10-bit ADC conversion is enabled.	0
10	W	RESERVED	This is a spare bit. Write a 0 to it.	0
	R	RESERVED	This is a spare bit. It indicates a 0.	0
9 to 0	W	IOFINT[n] (n=9 to 0)	0: The falling-edge trigger of the general-purpose I/O port is disabled. 1: The falling-edge trigger of the general-purpose I/O port is enabled. (Supplement) The bit numbers and I/O port numbers correspond one for one.	0
	R	IOFINT[n] (n=9 to 0)	0: Indicates that the falling-edge trigger of the general-purpose I/O port is disabled. 1: Indicates that the falling-edge trigger of the general-purpose I/O port is enabled.	0

Table 5.8.C Interrupt Source Reset Register (Address4)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	ACICLR	The interrupt requested by the Speech input clip signal is cleared as this bit is set from 0 to 1.	0
	R	ACINTST	0: Indicates that the interrupt requested by the Speech input clip signal is inactive. 1: Indicates that the interrupt requested by the Speech input clip signal is active.	0
14	W	TCICLR	The interrupt requested by the Telecom input clip signal is cleared as this bit is set from 0 to 1.	0
	R	TCINTST	0: Indicates that the interrupt requested by the Telecom input clip signal is inactive. 1: Indicates that the interrupt requested by the Telecom input clip signal is active.	0
13	W	MXICLR	The interrupt requested by the TSPY pin signal is cleared as this bit is set from 0 to 1.	0
	R	MXINTST	0: Indicates that the interrupt requested by the TSMX pin signal is inactive. 1: Indicates that the interrupt requested by the TSMX pin signal is active.	0
12	W	PXICLR	The interrupt requested by the TSPX pin signal is cleared as this bit is set from 0 to 1.	0
	R	PXINTST	0: Indicates that the interrupt requested by the TSPX pin signal is inactive. 1: Indicates that the interrupt requested by the TSPX pin signal is active.	0
11	W	ADCICLR	The interrupt requested for the completion of ADC conversion is cleared as this bit is set from 0 to 1.	0
	R	ADCINTST	0: Indicates that the interrupt requested for the completion of ADC conversion is inactive. 1: Indicates that the interrupt requested for the completion of ADC conversion is active.	0
10	W	RESERVED	This is a spare bit. Write a 0 to it.	0
	R	RESERVED	This is a spare bit. It indicates a 0.	0
9 to 0	W	IOICLR[n] (n=9 to 0)	The interrupt requested by a general-purpose I/O port is cleared as this bit is set from 0 to 1. (Supplement) The bit numbers and I/O port numbers correspond one for one.	0
	R	IOINTST[n] (n=9 to 0)	0: Indicates that the interrupt requested by a general-purpose I/O port is inactive. 1: Indicates that the interrupt requested by a general-purpose I/O port is active.	0

5.9 Telecom Interface

Figure 5.9.A shows a block diagram of the telecom Interface.

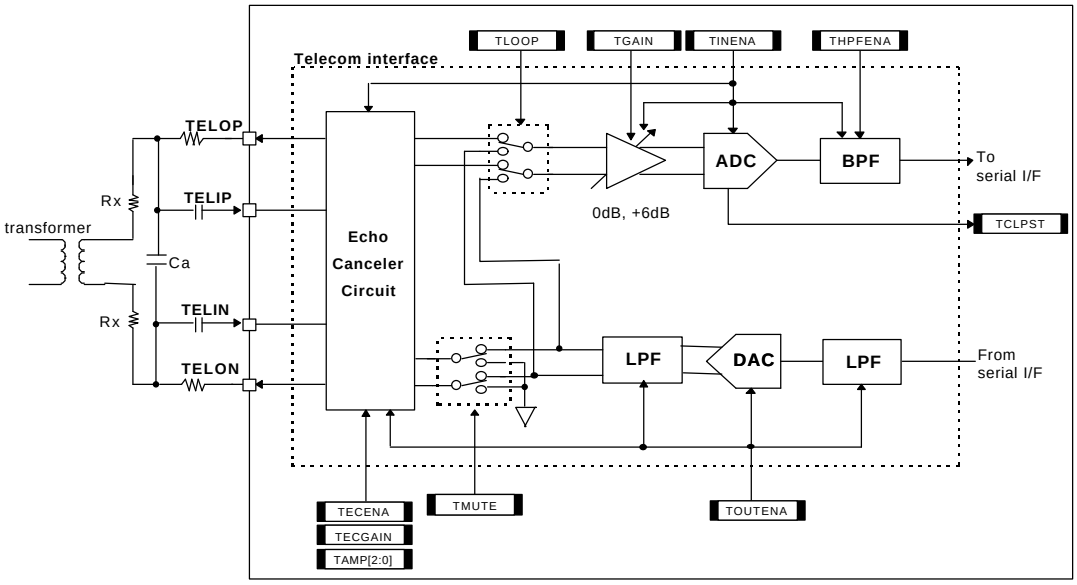


Figure 5.9.A Telecom interface block diagram

The Telecom interface is divided into three blocks: analog echo canceler, receive circuit block, and transmit circuit block. The transmit and receive paths can be enabled and disabled independently of each other. Disabling these paths help to reduce power consumption. The TINENA [W:6:14] and TOUTENA [W:6:15] are used to enable and disable the paths. The ADC and DAC sampling frequencies can be selected from 7.2 kHz, 8 kHz, and 9.6 kHz. The TDIV [W:5:6-0] are used to set the sampling frequency. In this case, the ADC and DAC should be set the same sampling frequency. It is impossible to set different sampling frequencies. The TLOOP [W:5:7] is used to set the analog loop path. This function is provided for evaluation purpose.

The analog echo canceler cancels only the transmit outputs feed-through signal. Based on a full-differential configuration, it provides the sufficient dynamic range necessary to transmit and receive modem-modulated signals. For details about circuit operation, refer to paragraph 5.9.1. The receive block is comprised of an analog attenuator, an ADC, and a digital BPF. The attenuator is controlled in two steps by 6 dB each. The TGAIN [W:6:8] is used to set the attenuator. The ADC turns on the TCLPST [R:6:4] status when the signal level is saturated. The host processor can adjust the input level using TGAIN when clipping is detected while monitoring the status. Since TCLPST remains intact once it is turned on, be sure to clear it using TCLPCLR [W:6:4]. TCLPST can be specified as an interrupt source. For this specification, use TCRINT [W:2:15] and TCFINT [W:3:15]. The digital BPF is configured with cascaded HPF and LPF. The HPF's cut-off frequency is approx. 300 Hz, so that the high-pass characteristic must be disabled in order for a low-frequency call progress tone to be detected. The THPFENA [W:6:3] is used to disable/enable the HPF. For the BPF's frequency characteristics, refer to paragraph 5.9.3.

The transmit block consists of a bandwidth-limiting digital LPF, a DAC, and a smoothing analog filter. The transmit outputs can be turned off by an analog muting switch to prevent feed-through of the transmit outputs. This is effective for half-duplex applications. The TMUTE [W:6:13] is used to set analog muting.

(Note) If carrying out enabling setting from the enable bit,please take note of the following points in the setting procedure.
If enabling both the transmitting side and the receiving side, carry out TINENA and TOUTENA enable setting simultaneously (on the same frame). If only the transmission side is enabled, and one continues to set the receiving side to enable for the first time, the receiving data may be incorrect in some cases.
It is possible to set one side to disable when both the transmission side and the receiving side are enabled.

The table below shows the registers of the telecom interface.

Table 5.9.A Telecom Interface Register A (Address 5)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15 to 13	W	TCOF[2:0]	These bits select the frequency response of the Telecom interface's digital filter. Choose the filter characteristic according to the sampling frequency. For the setup contents, see the table below. For details about filter characteristics, refer to 5.9.3. **Telecom interface sampling frequency** / **TCOF[2:0]** 7.2 kHz / 000b 8 kHz / 001b 9.6 kHz / 010b (Note) Do not set any other code.	1h
	R	TCOF[2:0]	These bits show the selected frequency response settings of the Telecom interface's digital filter. For the contents of setup code, refer to the explanation of the write register above.	1h
12 to 8	W	RESERVED	These bits are spare bits. Write a 0 to them.	0
	R	RESERVED	These are spare bits. They indicate a 0.	0
7	W	TLOOP	This bit sets the DAC to ADC loopback switch of the Telecom interface. This switch is used for test. 0 : Loopback disable 1 : Loopback enable	0
	R	TLOOP	0: Indicates that the line is not in a loopback mode. 1: Indicates that the line is in a loopback mode.	0
6 to 0	W	TDIV[6:0]	These bits set the sampling frequency. The desired frequency can be selected from three. The relationship between the sampling frequencies and the codes set is shown below. All other codes are inhibited for write. If those codes are written inadvertently, the filter may not output correct data. Nor can the data and valid data flag be output at the correct timing. **TDIV[6:0]** / **Sampling Frequency** 28h / 7.2 kHz 24h / 8 kHz 1Eh / 9.6 kHz	24h
	R	TDIV[6:0]	This bit indicates the sampling frequency that is set. For the relationship between code representation and frequencies, refer to the write register described above.	24h

Table 5.9.B Telecom Interface Register A(Address 6)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	TOUTENA	This bit enables the circuit on the DA side of the telecom interface. 0 : Disabled. 1 : Enabled.	0
	R	TOUTENA	This bit indicates setup status of whether the Telecom transmit unit is enabled or disabled. 0: Disabled. 1: Enabled.	0
14	W	TINENA	This bit enables the circuit on the AD side of the telecom interface. 0 : Disabled. 1 : Enabled.	0
	R	TINENA	This bit indicates setup status of whether the Telecom receive unit is enabled or disabled. 0: Disabled. 1: Enabled.	0
13	W	TMUTE	This bit disconnects the LPF output signal path located in the post-DAC stage of the telecom interface. 0 : Unmuted. 1 : Muted.	0
	R	TMUTE	This bit indicates the setup status of the Telecom transmit unit's mute switch. 0: Unmuted. 1: Muted.	0
12	W	TECGAIN	This bit controls the feedback gain echo canceler of the telecom interface. 0 : Ri = 26.23 kΩ 1 : Ri = 20 kΩ	0
	R	TECGAIN	This bit indicates the feedback gain control status of the Telecom echo canceler. 0 : Ri = 26.23 kΩ 1 : Ri = 20 kΩ	0
11	W	TECENA	This bit enables the echo canceler of the telecom interface. 0 : Disabled. 1 : Enabled.	0
	R	TECENA	This bit indicates setup status of whether the Telecom echo canceler is enabled or disabled. 0: Disabled. 1: Enabled.	0
10 to 9	W	RESERVED	These are reserved bits. Write 0 to these bits.	0
	R	RESERVED	These are spare bits. They indicate a 0.	0
8	W	TGAIN	This bit controls the amp gain at the pre-ADC stage of the telecom input path. 0 : 0 dB 1 : +6 dB	0
	R	TGAIN	This bit indicates the ADC pre amp gain setup status of the Telecom input path. 0 : 0 dB 1 : +6 dB	0

7 to 5	W	TAMP[2:0]	These bits control the receive amp gain in the echo canceler. The relationship between TAMP [2:0] and the gain is shown below. **TAMP[2:0] gain (dB)** 0h 0 1h +1.5 2h +3.0 3h +4.5 4h +6.0 5 +7.5 6h +9.0 7h +10.5	0h
	R	TAMP[2:0]	These bits indicate the internal receive amp gain setup status in the echo canceler. For the relationship between the code and the gain, refer to the write register described above.	0
4	W	TCLPCLR	This bit resets the AD clip flag of the telecom input ADC. The clip flag is reset to 0 at a high-going transition of this bit.	0
	R	TCLPST	This bit indicates the status of the ADC clip of the telecom interface. 0 : Saturation not detected. 1 : Saturation detected. Once set to 1, this flag remains set until it is reset by the TCLPCLR bit.	0
3	W	THPFENA	This bit enables or disables the HPF of the Telecom input path. 0: Disabled. 1: Enabled.	0
	R	THPFENA	This bit indicates setup status of whether the HPF of the Telecom input path is enabled or disabled. 0: Disabled. 1: Enabled.	0
2 to 0	W	RESERVED	These are spare bits. Write a 0 to these bits.	0
	R	RESERVED	These are spare bits. They indicate a 0.	0

5.9.1 Functional Description of Analog Echo Canceler

Figure 5.9.B shows a block diagram of the analog echo canceler in which a 600 Ω line load is assumed. To take full performance of the echo canceler, it is necessary to adjust an external resistor (Rx) according to the transformer's winding resistance. For details on how to adjust, refer to paragraph 5.9.2. The canceler operation is controlled by TECENA [W:6:11] and TECGAIN [W:6:12]. Use TECENA to disable/enable the canceler function and TECGAIN to set the outputs signal's feedback amount. Even when the canceler is disabled by TECENA, its power consumption is not reduced. Use TAMP [W:6:7-5] to set the receive gain. For the relationship between the setup code and gain, refer to the explanation of registers in this manual. It can be used as a complementary amp for TGAIN.

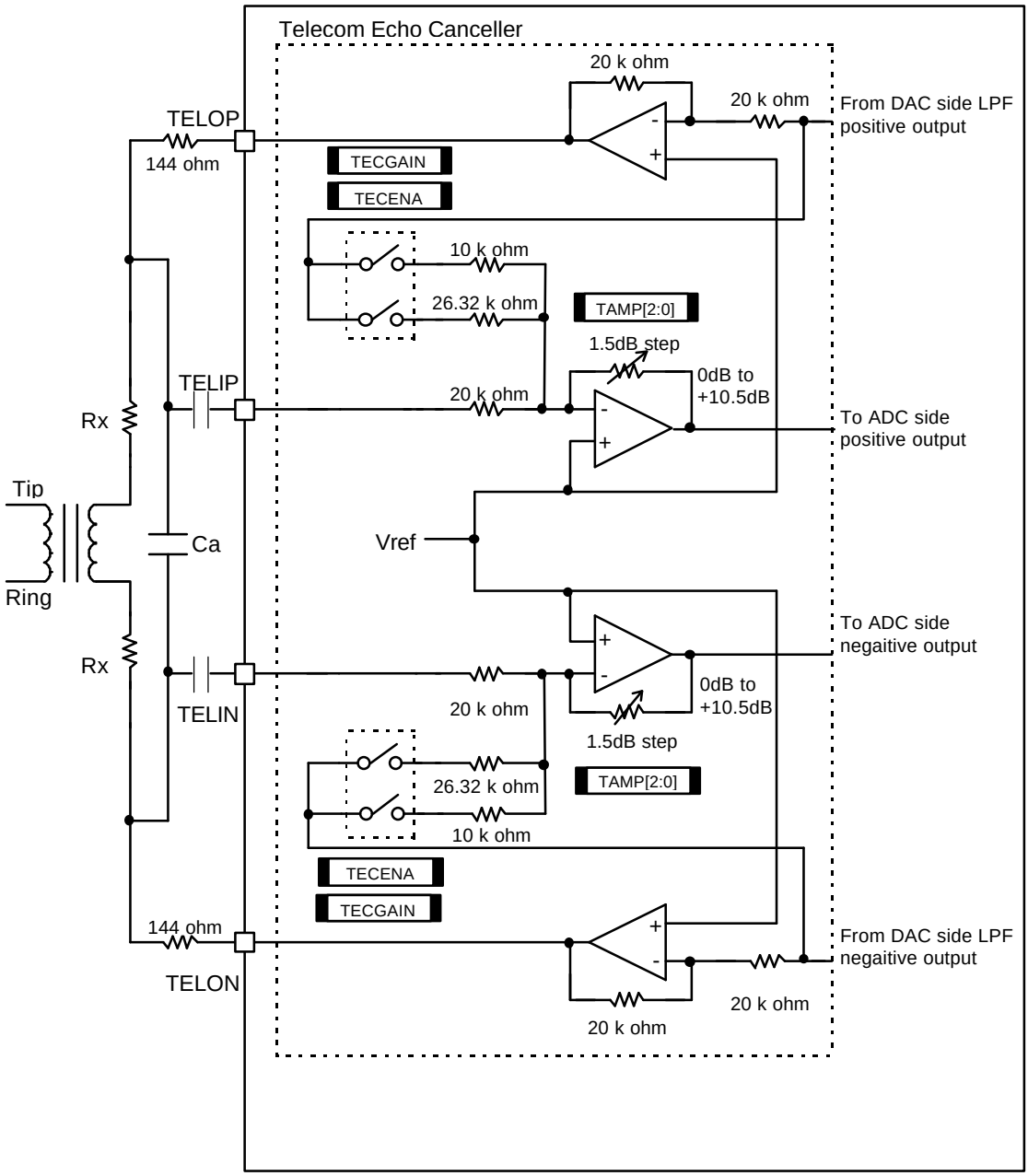


Figure 5.9.B Analog Echo Canceler Block Diagram

5.9.2 Functional Description of Analog Echo Canceler

Figure 5.9.C shows the equivalent circuit of the analog echo canceler. In this diagram, Ri is the transformer winding resistance, which is defined to be the same value on the primary and the secondary sides. The Rx is a resistor for adjusting the winding resistance. A 600 Ω termination is assumed for the line load.

The modem outputs signal is output from TELOP (TELON) to the line. Part of the signal feed through from TELIP (TELIN). The amount of the feed-through signal depends on the transformer winding resistance (Ri). Inside the modem, on the other hand, a polarity-inverted signal of the outputs signal is fed back from the outputs amp to the input amp via Rb, thereby canceling the feed-through signal. This cancellation helps to increase the allowable input dynamic range.

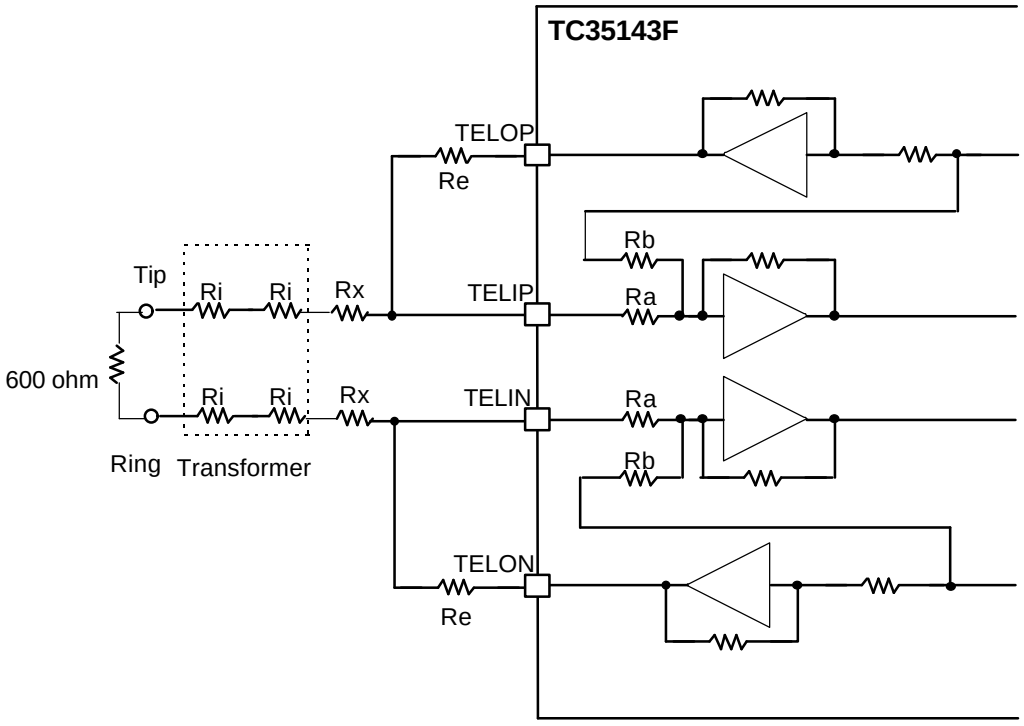


Figure 5.9.C Equivalent circuit of echo canceler

The outputs resistance, Rout, that appears to TELOP is as follows:

$$Rout = 2 \times Ri + Rx + Re$$

With the differential configuration taken into account, the maximum efficiency is obtained when Rout is 300 Ω (600/2). Therefore, the following relationship is established:

$$2 \times Ri + Rx + Re = 300$$

If it is assumed that the maximum value of a transformer's winding resistance generally is 156 Ω (2Ri) and Rx is 0 Ω , then Re = 144 Ω. In this case, the signal level running around from TELOP into TELIP is as follows:

$$Vout \times (156+300)/(144+156+300) = Vout \times 456/600$$

Therefore, regarding the internal feedback amount of the echo canceler necessary to cancel the run-around signal, the following condition must be met:

$$Rb/Ra = 600/456$$

Since Ra in the TC35143BF is 20 kΩ, Rb is determined as follows:

$$Rb = 600/456 \times 20k = 26.32k\Omega$$

If the winding resistance is smaller than 156Ω, adjust the total resistance of (2Ri + Rx) until it equals 156Ω by adding a wanted resistance to Rx. In this case, the echo canceler's feedback amount must be set to 26.32kΩ by using TECGAIN [W:6:12].

If the winding resistance is 0Ω, set Re = 300Ω. In this case, Rx is unnecessary. In this case, maximum cancellation performance can be achieved by setting the echo canceler's feedback amount to 10kΩ using TECGAIN [W:6:12].

5.9.3 Receive Band-pass Filter Characteristics

Figures 5.9.D, 5.9.E and 5.9.F show the characteristics of the band-pass filter (BPF) that is inserted in the Telecom interface receive path. Shown here are only the high-pass characteristics of the filter in the low-frequency range. Although high-pass characteristics normally are inserted for canceling DC offset and limiting the bandwidth, they prevent the high-pass characteristics to low-frequency call progress tone detection. In such a case, THPENA [W:6:3] can be used to disable the high-pass characteristics. The dotted lines in the diagrams show the frequency responses where the high-pass characteristic is enabled. The low-pass characteristic of the BPF is that frequencies are cut off at about 3 kHz.

The transmit path of the Telecom interface has a low-pass filter (LPF) inserted in it. The low-pass characteristic of this LPF is that frequencies are cut off at about 3 kHz, as in the case of the BPF inserted in the receive path.

For both transmit and receive operations, three types of filter characteristics are available to choose from according to the ADC and DAC sampling frequencies. Set the appropriate filter characteristic using the control register. For the relationship between the sampling frequencies and the filter characteristics to be selected, refer to Table 5.9.A (Telecom interface register A).

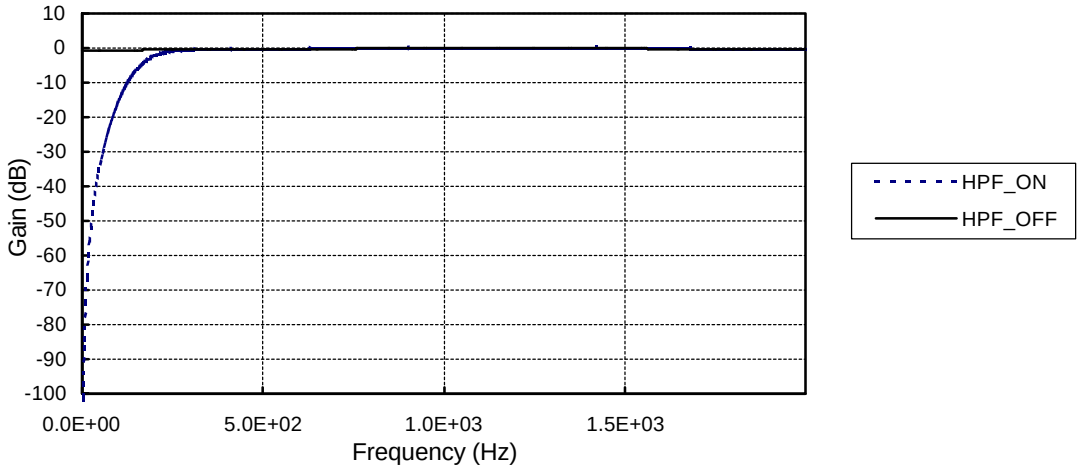


Figure 5.9.D Input BPF frequency response (when sampling frequency = 7.2 kHz)

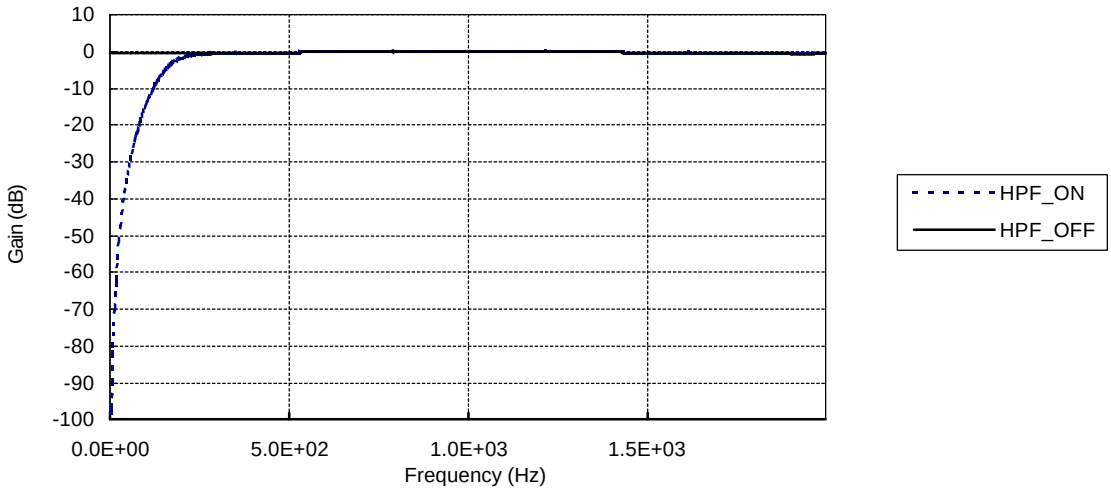


Figure 5.9.E Input BPF frequency response (when sampling frequency = 8 kHz)

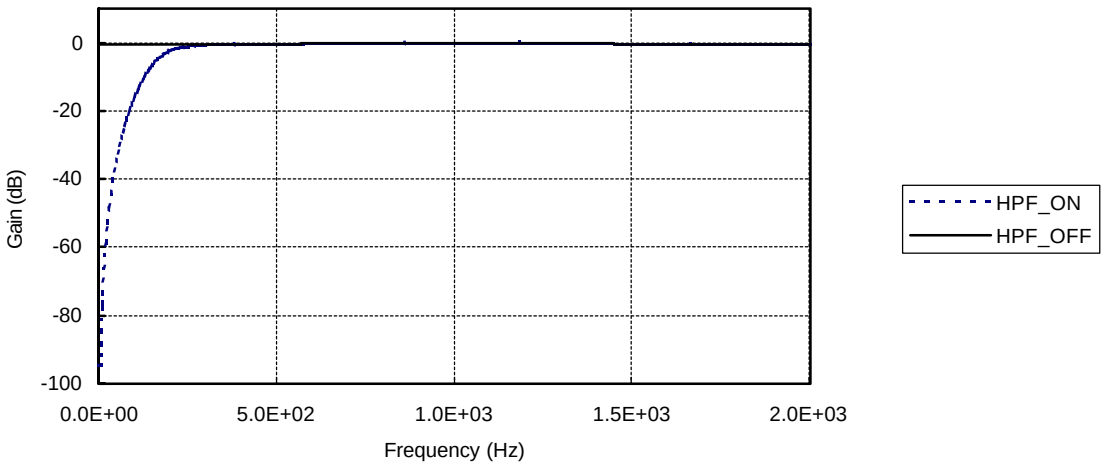


Figure 5.9.F Input BPF frequency response (when sampling frequency = 9.6 kHz)

5.9.4 Relationship Between Analog Signal and Digital Code

Fig. 5.9.D shows the relationship between the circuit interface analog output signal and the digital code input to the SDIN stream. The analog waveform in the diagram is the signal waveform in the event that it has been full-scale output to the differential output.

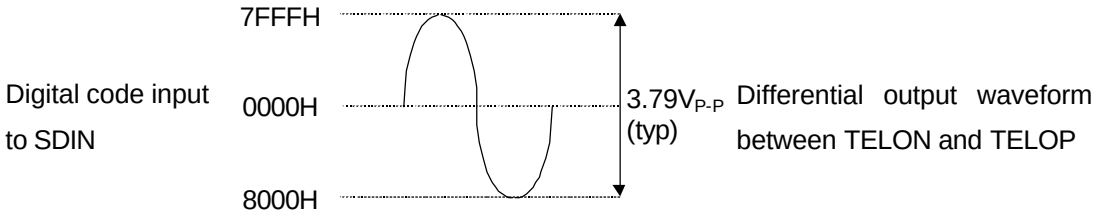


Figure 5.9.G Relationship Between Circuit Output Signal and Digital Code

(Supplement 1) Digital code is a complement expression to coded 2.

Fig. 5.9.E shows the relationship between the circuit interface analog input signal and the digital code output to the SDOUT stream. The analog waveform in the diagram is the signal waveform in the event that it has been full-scale output to the differential output.

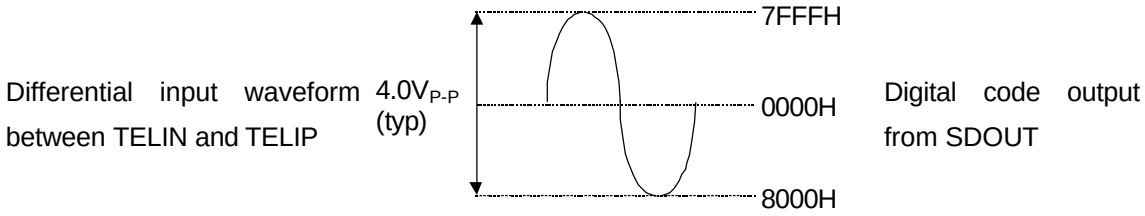


Figure 5.9.H Relationship Between Circuit Input Signal and Digital Code

(Supplement 1) Digital code is a complement expression to coded 2.
(Supplement 2) Gain amplifier setting is always set to 0 dB.

5.10 Voice Interface

The following figure shows the voice interface block diagram.

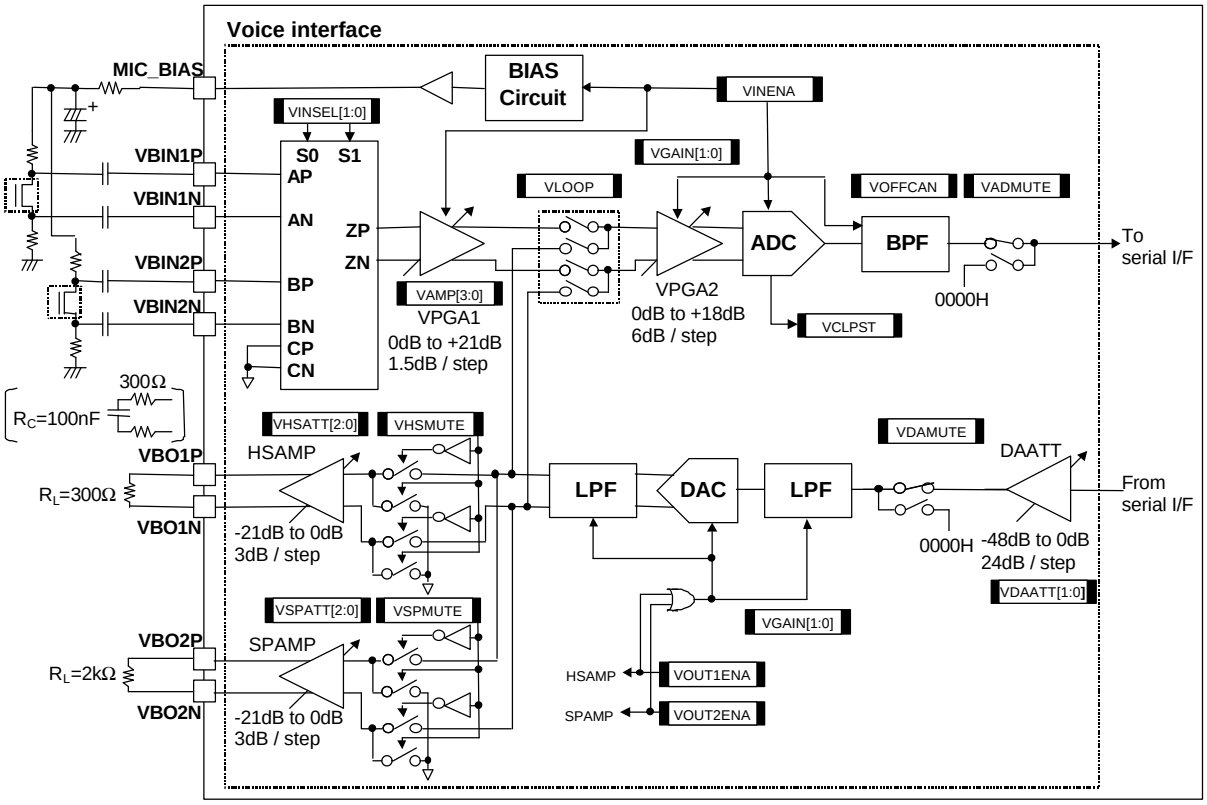


Figure 5.10.A Voice Interface Block Diagram

The Voice interface is divided into two blocks: a receive circuit and a transmit circuit block. The transmit and receive terminals are provided for two channels each. These circuits are configured to accommodate both hands-free and handset applications and almost do not require external parts.

The transmit block contains input terminals for external microphones (VBIN2P, VBIN2N) and handset microphones (VBIN1P, VBIN1N) and an analog switch to choose between these inputs. The switch is controlled by VINSEL [W:7:15-14].

The receive block has outputs terminals for external speakers (VBO2P, VBO2N) and handset receivers (VBO1P, VBO1N). An outputs amp and an analog mute switch are included for each speaker output. The outputs amp can be adjusted for gain by using VHSATT [W:8:11-9] (for handset receivers) and VSPATT [W:8:2-0] (for external speakers). The mute switch can be controlled by VHSMUTE [W:8:12] (for handset receivers) and VSPMUTE [W:8:5] (for external speakers) independently of each other.

The transmit and receive paths can be enabled/disabled independently of each other. The device power consumption can be reduced by disabling these paths. This setting is accomplished using VOUT2ENA [W:7:13], VOUT1ENA [W:8:15], and VINENA [W:8:14].

The ADC and DAC sampling frequencies can be selected from four frequencies: 8 kHz, approx. 11.08 kHz, 16 kHz, and approx. 22.15 kHz. However, when operating the Telecom CODEC simultaneously with the Voice Interface, the contents of settings are subject to limitations. For details, refer to the description of VDIV [W:7:6-0] in Table 5.10.A. This VDIV [W:7:6-0] is used to set the sampling frequencies. Reenable the ADC and DAC after setting the sampling frequency with VDIV. The VLOOP [W:8:8] is used to set the analog loop path. This is a function provided for evaluation purposes.

The transmit block is configured with analog amps, ADC, and digital BPF. The amps are controlled by a combination of 15-levels (in 1.5 dB step) and 4-levels (in 6 dB step) control. These controls are performed using VAMP [W:7:10-7] and VGAIN [W:7:12-11]. The ADC turns on the status VCLPST [R:8:6] when the signal level is saturated. The host processor can adjust the input level using VAMP and VGAIN when clipping is detected while monitoring the status. Since VCLPST remains intact once it is turned on, be sure to clear it using VCLPCLR [W:8:6]. The VCLPST can be specified as an interrupt source. For this specification, use ACRINT [W:2:15] and ACFINT [W:3:15]. The digital BPF is configured with cascaded HPF and LPF. To cancel the input signal DC offset, enable the HPF characteristic. Use VOFCAN [W:D:13] to enable/disable the HPF characteristic. (See Table 5.5.A.) The VADMUTE [W:8:13] is used to control the digital mute switch. When the mute switch is turned on, a digital code equivalent to no-signal representation is input.

The receive block consists of a bandwidth limiting digital attenuator, LPF, DAC, and an output amp. The digital mute switch allows transmit output to be turned off, thereby preventing the transmit output from running around into the transmitter. This is effective for half-duplex applications. The VDAMUTE [W:8:7] is used to set this switch. When the mute switch is turned on, a digital code equivalent to no-signal representation is output. The mute switch is followed by the digital attenuator. It is capable of 3-levels control in 24 dB step. The VDAATT [W:8:4-3] is used to set this attenuator. When combined with HSAMP or SPAMP, it allows for sophisticated tone control.

5.10.1 Configuration of External Microphone Circuit

Figures 5.10.B and 5.10.C show typical configurations of microphone circuits. In either case, the circuit uses a capacitor microphone. The microphone bias voltage is supplied from the MICBIAS pin. To stabilize the bias voltage, insert a resistor of about 2 kΩ (R5) and a capacitor of 10 uF (C5) in series between the MICBIAS pin and the analog GND. Note that when the signal input path is disabled by setting VINENA [W:8:14], the device also stops supplying the bias voltage.

For a differential configuration, the high-pass characteristic is materialized using resistors R1 to R4 and capacitors C1 to C4. Choose the capacitor value that will help to attenuate the microphone peak frequency.

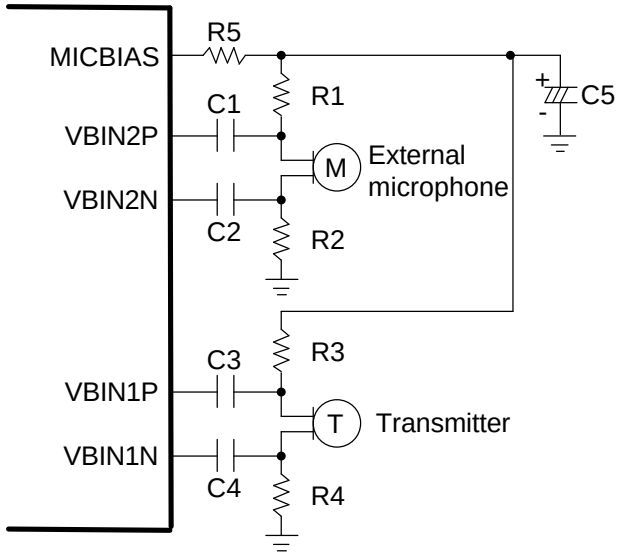


Figure 5.10.B Example for connecting a condenser microphone (for differential configuration)

For a single configuration, input a signal to VBIN1P and VBIN2P. In this case, insert capacitors between the VBIN1P and VBIN2P pins and the analog GND that have the same capacitance values as those connected to the VBIN1N and VBIN2N pins. Also, connect one side of the microphone directly to the analog GND.

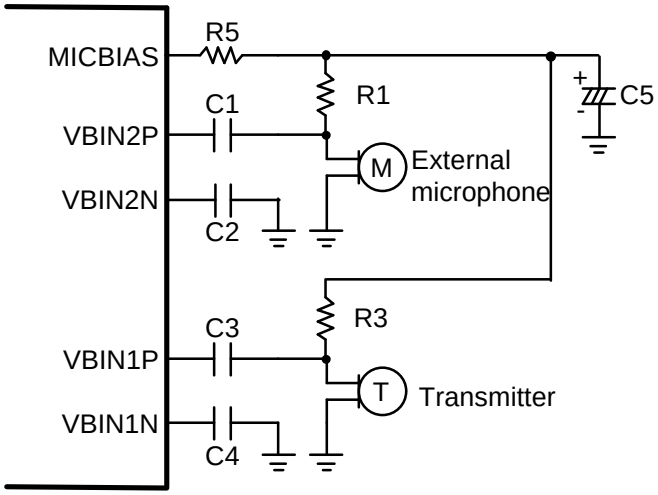


Figure 5.10.C Example for connecting a condenser microphone (for single configuration)

5.10.2 Configuration of External Speaker Circuit

Figures 5.10.D and 5.10.E show typical configurations of speaker circuits. Here, VBO1P and VBO1N are the signal outputs pins for a handset receiver. The handset receiver amp can drive typically a 100 nF load for ceramic receivers or a 300 Ω load for dynamic receivers directly. However, if your application drives a general 8, 16, or 32 Ω speaker load, add a speaker amp external to the chip.

For a differential configuration, no capacitor is required for eliminating DC offsets. Use resistors R1 to adjust the sound volume of the receiver. Remove these resistors if the sound volume does not need to be adjusted. Use R3 and R6 to adjust the sound volume of the external speaker.

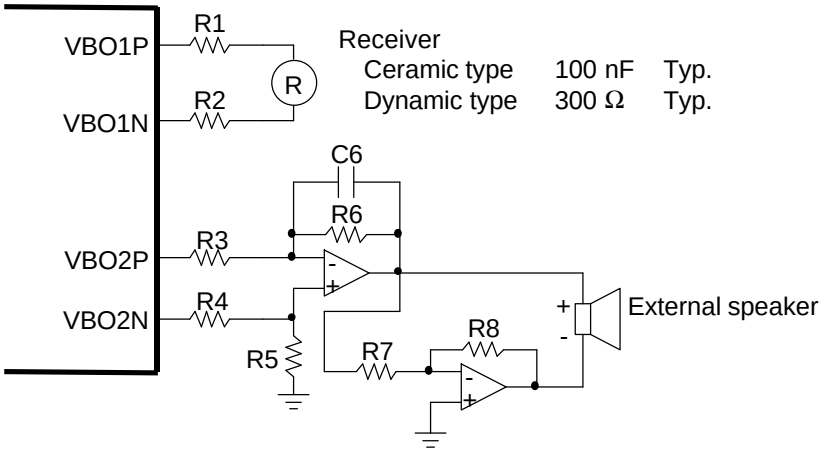


Figure 5.10.D Example of a speaker circuit (for differential configuration)

When using the VBO2 side in a single configuration, connect VBO2P to the receiver or speaker via a capacitor to eliminate the DC offset and a resistor to adjust the sound volume. In this case, Toshiba recommends connecting the same load to VBO2N as one used for VBO2P. This helps to improve the output amp's drive balance. On the other hand, using VBO1P and VBO1N in a single configuration is prohibited. Connect them in a differential configuration as shown in the diagram above.

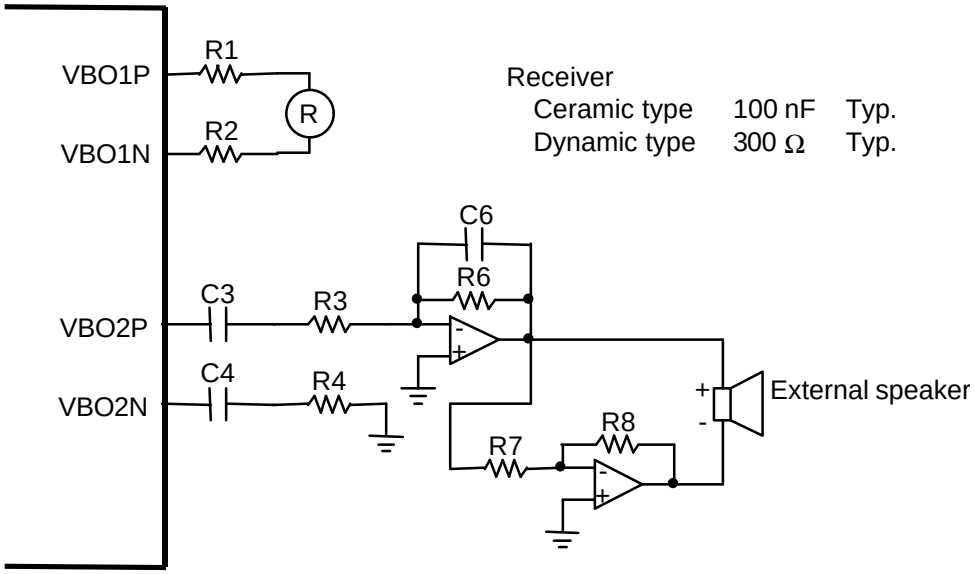


Figure 5.10.E Example of a speaker circuit (Using VBO2 in a single configuration)

The table below shows the control register of voice interface.

Table 5.10.A Voice Interface Register A (Address 7)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15 to 14	W	VINSEL[1:0]	These bits select analog input pins to the voice input path. 0h : Muted (Connected to the reference voltage inside the chip) 1h : Full-differential input pins VBIN1P and VBIN1N are selected. 2h : Full-differential input pins VBIN2P and VBIN2N are selected. 3h : Inhibited for write.	0h
	R	VINSEL[1:0]	These bits indicate the select status of the voice analog input pins. For details about the code and the corresponding status, refer to the write register described above.	0
13	W	VOUT2ENA	This bit enables the output amp for external speaker (SPAMP). 0 : Disabled. 1 : Enabled.	0
	R	VOUT2ENA	This bit indicates setup status of whether the Voice output amp SPAMP is enabled or disabled. 0 : Disabled. 1 : Enabled.	0
12 to 11	W	VGAIN[1:0]	These bits control the amp gain of the pre-AD stage in the voice input path. For details, see the table below. **VGAIN[1:0] VPGA1 gain (dB) comment** 0h 0 default 1h +6 2h +12 3h +18	0h
	R	VGAIN[1:0]	These bits indicate the setup status of the amp gain of the Voice input path. For details between the code representation and the corresponding gain, refer to the write register described above.	0h

<table>
<tr><td rowspan="2">10 to 7</td><td>W</td><td>VAMP[3:0]</td><td>These bits control the gain of the microphone amp in the voice input path. For details, see the table below.

VAMP[3:0] — VPGA1 gain (dB) — comment
0h — 0 — default
1h — +1.5
2h — +3.0
3h — +4.5
4h — +6.0
5h — +7.5
6h — +9.0
7h — +10.5
8h — +12.0
9h — +13.5
Ah — +15.0
Bh — +16.5
Ch — +18.0
Dh — +19.5
Eh — +21.0
Fh — +21.0</td><td>0h</td></tr>
<tr><td>R</td><td>VAMP[3:0]</td><td>These bits indicate the setup status of the VPGA1 amp of the Speech input unit. For details about code representation and the corresponding gain, refer to the write register described above.</td><td>0</td></tr>
<tr><td rowspan="2">6 to 0</td><td>W</td><td>VDIV[6:0]</td><td>These bits comprise a sampling frequency setup register for the Voice unit. One of the four frequencies shown below can be set.
The following shows the relationship between VDIV [6-0] and the sampling frequencies. Writing any other codes is inhibited. If one of those codes is written inadvertently, the TC35143BF may not be able to send or receive sampling data correctly.

VDIV[6:0] — Sampling Frequency — AD side — DA side — comment
24h — 8 kHz — Available — Available — Default
1Ah — 11.08 kHz — Available, subject to restrictions. — Available, subject to restrictions.
12h — 16 kHz — Available, subject to restrictions. — Available, subject to restrictions.
0Dh — 22.15 kHz — Available, subject to restrictions. — Available, subject to restrictions.

<u>The restriction except for 8kHz sampling frequency</u>.
The restriction depend on the operation condition in the Telecom unit. Make sure the unused block are disabled. The restriction is shown below.
<u>(The restriction when both ADC and DAC are disabled in the Telecom unit)</u>
If either ADC or DAC is enabled in the Voice unit, 8kHz, 11.08kHz, 16kHz and 22.15kHz are available.
If both ADC and DAC are enabled in the Voice unit, 8kHz, 11.08kHz and 16kHz are available.
<u>(The restriction when at least either ADC or DAC is enabled in the Telecom unit)</u>
If either ADC or DAC is enabled in the Voice unit, 8kHz, 11.08kHz and 16kHz are available.
If both ADC and DAC are enabled in the Voice unit, 8kHz is available.</td><td>24h</td></tr>
<tr><td>R</td><td>VDIV[6:0]</td><td>These bits indicate the Speech unit's sampling frequency.
For details about the code and the corresponding gain, refer to the write register described above.</td><td>24h</td></tr>
</table>

The table below shows the registers of voice interface.

Table 5.10.B Voice Interface Register B (Address 8)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	VOUT1ENA	This bit enables the output amp for handset receiver (HSAMP) 0 : Disabled. 1 : Enabled.	0
	R	VOUT1ENA	This bit indicates setup status of whether the voice output amp HSAMP is enabled or disabled. 0: Disabled. 1: Enabled.	0
14	W	VINENA	This bit enables the ADC in the voice input path. 0 : Disabled. 1 : Enabled.	0
	R	VINENA	This bit indicates setup status of whether the voice input path is enabled or disabled. 0: Disabled. 1: Enabled.	0
13	W	VADMUTE	This bit controls the voice input digital mute switch. 0 : Unmuted. 1 : Muted.	0
	R	VADMUTE	This bit indicates setup status of the voice input digital mute switch. 0 : Unmuted. 1 : Muted.	0
12	W	VHSMUTE	This bit controls the voice output HSAMP's analog mute switch. 0 : Unmuted. 1 : Muted.	1
	R	VHSMUTE	This bit indicates the setup status of the voice output HSAMP's analog mute switch. 0 : Unmuted. 1 : Muted.	1
11 to 9	W	VHSATT[2:0]	These bits control the attenuator of the voice output amp HSAMP. The relationship between VHSATT [2:0] and the HSAMP gain is shown below. **VHSATTP[2:0] HSAMP gain (dB)** 0h 0 1h -3 2h -6 3h -9 4h -12 5 -15 6h -18 7h -21	0
	R	VHSATT[2:0]	These bits indicate the setup status of the voice output amp HSAMP's attenuator. For details about the code and the corresponding gain, refer to the write register described above.	0

8	W	VLOOP	This bit controls the loopback path of the voice interface. 0: The loop back path is disabled. 1: The loop back path is enabled.	0
	R	VLOOP	This bit indicates the setup status of the loopback path of the voice interface. 0: The loop back path is disabled. 1: The loop back path is enabled.	0
7	W	VDAMUTE	This bit controls the voice output digital mute switch. 0: Unmuted. 1: Muted.	0
	R	VDAMUTE	This bit indicates the setup status of the voice output digital mute switch.	0
6	W	VCLPCLR	This bit clears the VCLPST flag to 0. VCLPST flag is cleared when this bit is set from 0 to 1.	0
	R	VCLPST	This bit indicates the status of the ADC clip of the voice interface. 0: Saturation not detected. 1: Saturation detected.	0
5	W	VSPMUTE	This bit controls the voice output SPAMP's analog mute switch. 0: Unmuted. 1: Muted.	1
	R	VSPMUTE	This bit indicates the setup status of the voice output SPAMP's analog mute switch. 0: Unmuted. 1: Muted.	1
4 to 3	W	VDAATT[1:0]	These bits control the digital attenuator DAATT of the voice output path. The relationship between VDAATT [1:0] and the gain is shown below. **VDAATT[1:0] gain (dB)** 0h 0 1h -24 2h -48 3h Muted	0h
	R	VDAATT[1:0]	These bits indicate the setup status of the voice output path digital attenuator DAATT. For the relationship between code representation and the corresponding gain, refer to the write register described above.	0h
2 to 0	W	VSPATT[2:0]	These bits control the attenuator of the voice output amp SPAMP. The relationship between VSPATT [2:0] and the SPAMP gain is shown below. **VSPATTP[2:0] SPAMP gain (dB)** 0h 0 1h -3 2h -6 3h -9 4h -12 5h -15 6h -18 7h -21	0h
	R	VSPATT[2:0]	These bits indicate the setup status of the attenuator of the voice output amp SPAMP. For the relationship between code representation and the corresponding gain, refer to the write register described above.	0h

5.10.3 Voice Interface Receive Filter Characteristics

Figure 5.10.F. shows the characteristics of the band-pass filter (BPF) that is inserted in the Voice interface receive path. Shown here are only the high-pass characteristics of the filter in the low-frequency range. Note also that the sampling frequency is normalized. The high-pass characteristics normally are inserted for canceling DC offset. If your circuit does not require a DC offset canceler, you can use VOFFCAN [W:D:13] to disable the high-pass characteristic. The dotted lines in the diagram show the frequency responses where the high-pass characteristic is enabled. The low-pass characteristic of the BPF is that frequencies are cut off at about Fs/2.

The transmit path of the Voice interface has a low-pass filter (LPF) inserted in it. The low-pass characteristic of this LPF is that frequencies are cut off at about Fs/2, as in the case of the BPF inserted in the receive path.

For both transmit and receive operations, two types of filter characteristics are available to choose from according to the ADC and DAC sampling frequencies. Set the appropriate filter characteristic using the control register. For the relationship between the sampling frequencies and the filter characteristics to be selected, refer to Table 5.5.A (mode register).

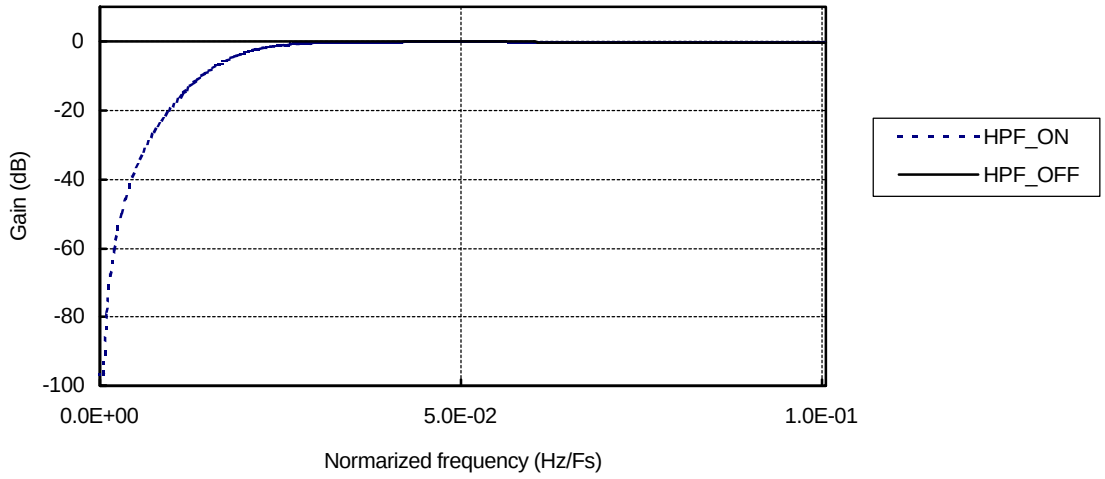
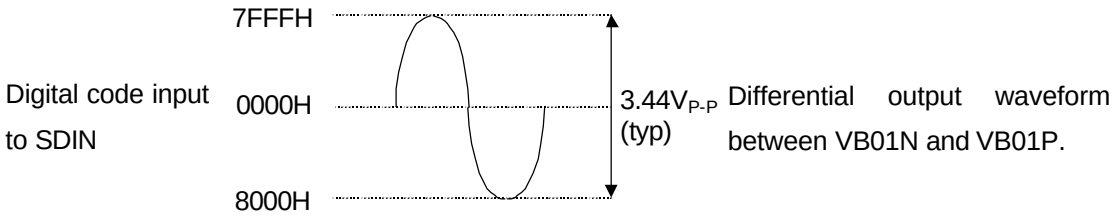


Figure 5.10.F Input BPF frequency response
(when sampling frequency=8kHz,11.08kHz,16kHz,22.15kHz)

5.10.4 Relationship Between Analog Signal and Digital Code

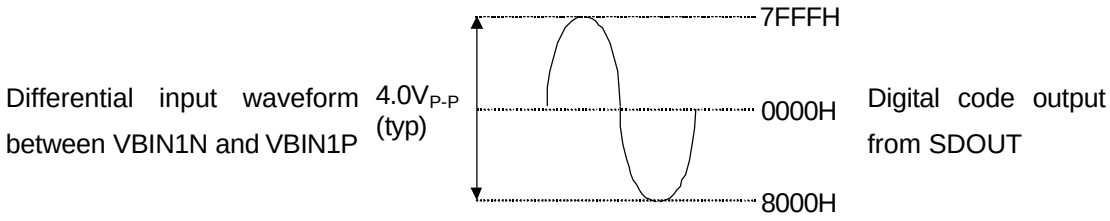
Fig. 5.10.G shows the relationship between the sound interface analog output signal and the digital code input to the SDIN stream. The analog waveform in the diagram is the signal waveform in the event that it has been full-scale output to the differential input.



(Supplement 1) Digital code is a complement expression to coded 2.
(Supplement 2) Attenuator setting is always set to 0 dB.
(Supplement 3) The relationship is exactly the same for VB02N and VB02P.
(Supplement 4) With regard to the lowest 2 bits, TC35143BF ignores data.

Figure 5.10.G Relationship Between Sound Output Interface and Digital Code

Fig. 5.10.H shows the relationship between the sound interface analog input signal and the digital code output to the SDOUT stream. The analog waveform in the diagram is the signal waveform in the event that it has been full-scale input to the differential input.



(Supplement 1) Digital code is a complement expression to coded 2.
(Supplement 2) Gain amplifier setting is always set to 0 dB.
(Supplement 3) The relationship is exactly the same forVBIN2N and VBIN2P.
(Supplement 4) With regard to the lowest 2 bits of the digital code, there is no accuracy, so they are undefined.

Figure 5.10.H Relationship Between Sound Input Signal and Digital Code

5.11 Control Register

The TC35143BF has an interface for a 4-terminal resistor network touch-screen. This interface supports two modes: an X/Y position measurement and an touch detection mode. Measurement in each operation mode can be performed by manipulating the TSC MODE and the POWER/GND switch registers. Position measurement and startup from a standby state can be accomplished using each operation mode. In this section, each operation sequence is explained after the measurement principle.

5.11.1 Principle of Position Measurement

Two measurements are taken to measure a contact position. The measurement of the X plate position performed first yields 2-dimensional X-coordinate position data. The second measurement obtains Y-coordinate position data. Figure 5.11.A shows an example of a contact position measurement. R1 and R2 are the plate resistors of the X plate. R5 is a contact resistor between the X and Y plates. When a bias voltage is applied between TSPX and TSMX by the TC35143BF, the contact point voltage indicates the ratio of resistance R1 and R2. This means that a physical position on X coordinate is known. The contact point voltage is measured via R5 and Y plate using the internal 10-bit ADC. When measuring the X plate position, the Y plate is used as an input interface for the ADC. By measuring the TSMX and TSPX voltages, more accurate measurements can be performed in which the effects of parasitic resistance components, etc. are eliminated.

The same procedure can be followed to measure a physical position on Y coordinate as used for the X coordinate. In this case, the TC35143BF applies the bias voltage between TSPY and TSMY and the contact point voltage is measured via R5 and X plate.

This position measurement is performed by using the position measurement mode.

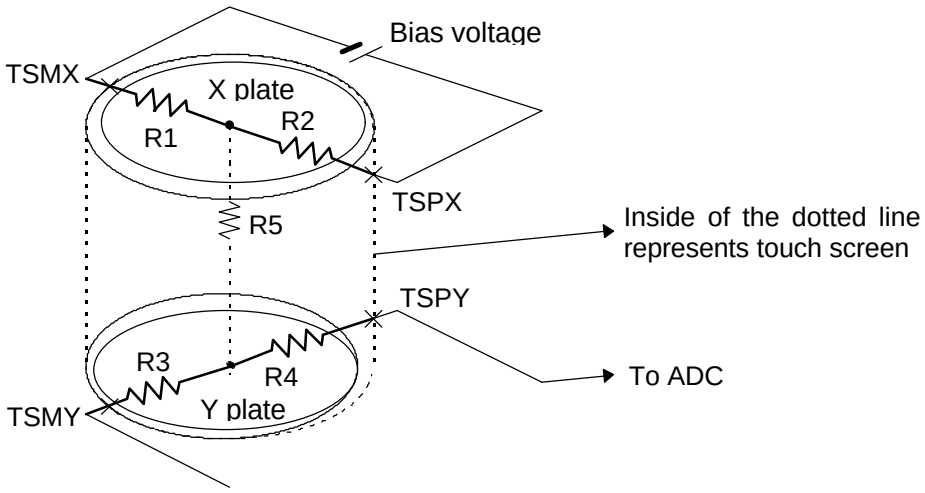


Figure 5.11.A Principle of position measurement

5.11.2 Principle of Position Calibration

For the more exact measurement, the calibration is needed. Calibration means to measure the voltage of a certain point such as (a) to (e) in the following figure, that is to check the linearity of the plate. These certain point measurements are performed by using position measurement mode. Calibration reduces the number of measurement for compensation of touch screen resistance deviation. Following the example of the calibration.

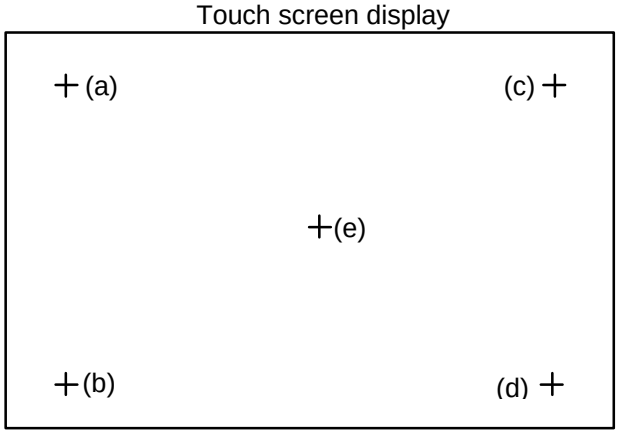


Figure 5.11.B Touch screen calibration position

(1) By stylus, push the point (a) in above figure.
(2) On the position measurement mode, measure the (a) point X coordinate position data.
(3) Measure the voltage of TSPX terminal and TSMX terminal.

By the above actions, the system recognizes the relation between the X physical position on the screen and the voltage of the point. After this calibration, the measurement of the TSPX and TSMX terminal is not needed on the position measurement.

(4) About Y plate, measure by the similar way as the (1), (2) and (3) operation.

(5) About (b), (c), (d), (e) point, the same sequence as the (a) point should be done. A host processor saves the each position data and uses it for position compensation in the position measurement.

5.11.3 Principle of Contact Detection

In addition to the position measurement mode, the TC35143BF has a mode for generating an interrupt signal by detecting contact with the screen. This is called the touch detection mode. Figure 5.11.C shows the principle of touch detection. In touch detection mode, the bias voltage is applied between the X and Y plates via Rint. The bias voltage supplied in touch detection mode is 3.3 V (VDD), and not the ordinary touch-screen bias voltage (1.9 V, type.). If no touch with the screen is detected, R5 is so large that no current flows between the X and Y plates. If touch with the screen is detected, a current flows between the plates causing the voltage TSPX or TSMX to drop. This voltage drop is detected by a Schmitt trigger-type buffer. The amounts of voltage drops in TSPX and TSMX vary with the position at which the screen is touched. Therefore, only if a voltage drop in either TSPX or TSMX can be confirmed, it can be assumed that the screen has been touched.

The outputs voltage of the Schmitt trigger-type buffer is toggled again when a contact point is released as when the screen is touched. The outputs of the Schmitt trigger-type buffer is reflected in TSMXLOW [W:9:13] and TSPXLOW [W:9:12]. These bits indicate a 1 when the screen is touched. Also, these bits are connected to the interrupt control circuit. By specifying a rising edge or falling edge trigger for the interrupt source, it is possible to detect both contact and release. To specify edge triggers, use MXRINT [W:2:13], PXRINT [W:2:12], MXFINT [W:3:13], and PXFINT [W:3:12]. The interrupt status is indicated by MXINTST [R:4:13] and PXINTST [R:4:12].

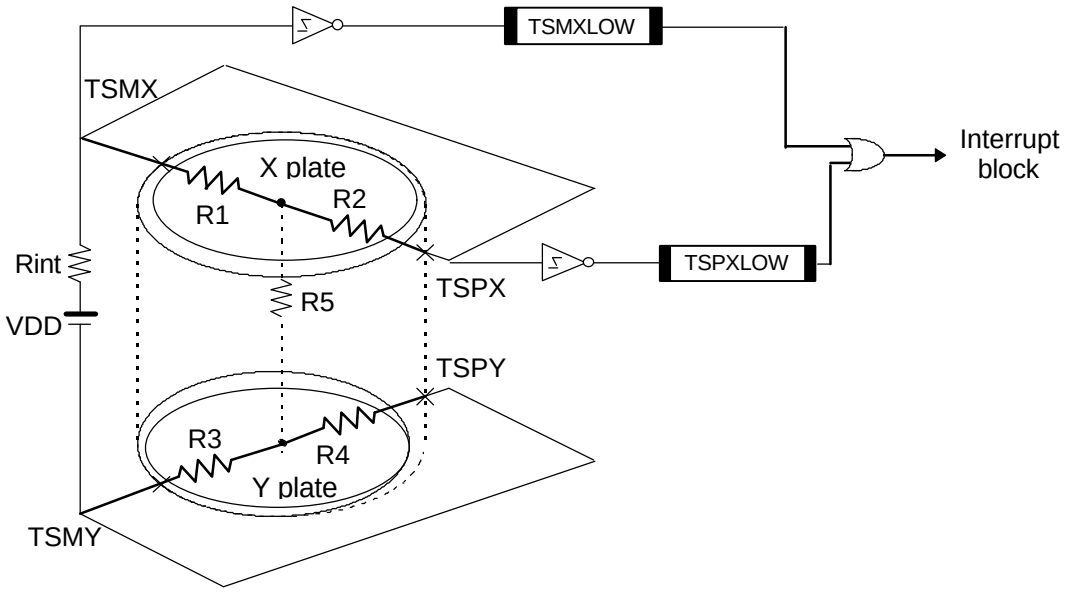


Figure 5.11.C Principle of touch detection

5.11.4 Operation Modes and Block Configuration

Table 5.11.A lists the operation modes of the touch-screen. The operation modes are set by TSCMOD [W:9:9-8]. There are two operation modes: the position measurement and the touch detection mode. The touch detection mode is effective in both standby and normal states. Therefore, startup from a standby state based on touch detection is possible. While the position measurement mode is effective in only normal states.

Table 5.11.A Touch-screen Modes

TSCMOD	Operation Mode
00	Touch detection mode
01	Spare
00	Position measurement mode
11	Spare

The touch-screen is controlled using four pins: TSPX, TSMX, TSPY, and TSMY. Connect a noise-eliminating external capacitor to each pin as shown in Figure 5.11.D.

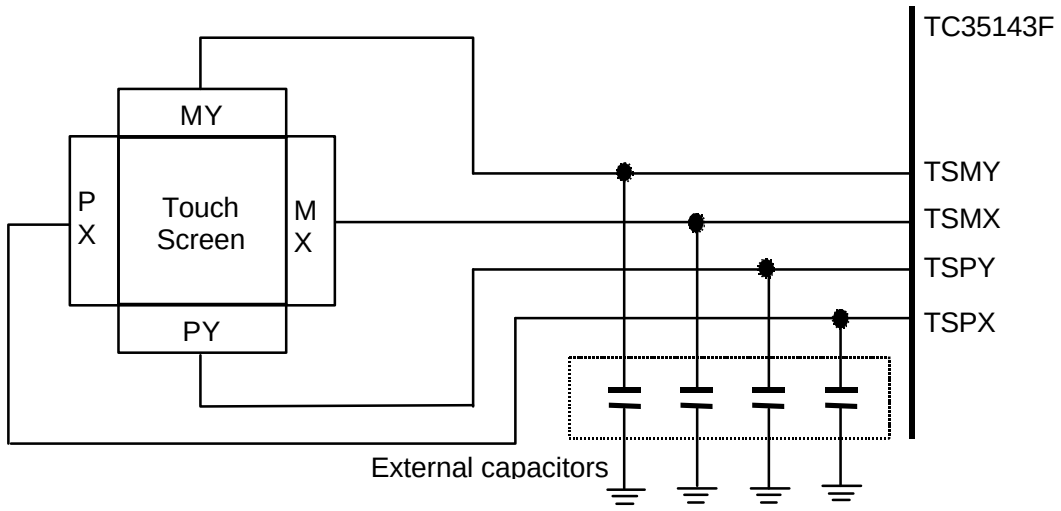


Figure 5.11.D External connections

RC integration circuit (LPF) is composed by a touch screen resistance network and a noise reduction capacitor which are connected with touch screen terminal (TS**). Therefore, the voltage increase according to settling time of the RC integration circuit. Figure 5.11.E shows the equivalent circuit.

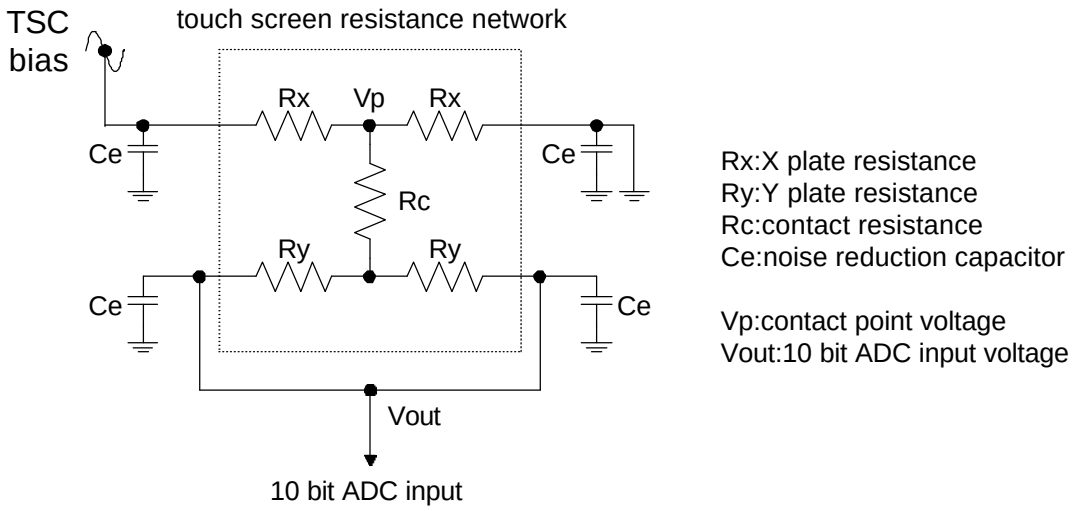


Figure 5.11.E The equivalent circuit in touch screen position measurement

The capacitor (Ce) which connected with Vdd (Touch screen bias voltage) and Vss can be ignored because the power supply is direct current type. When a pen touches a plate, contact point voltage Vp is decided. After that, Vout increase (or decrease) gradually. The following equation represents the voltage transition time.

ts = -R * C * ln(1-0.999)
R : Total resistance which depend on touch screen (Rc+Rp/2)
C : Total capacitance of noise reduction capacitors (2Ce)
(Supplement) Ts of above formula means the time that Vout reach 99.9 % Vp.

An example for calculating measurement period is shown below. Each value below is the ones of a popular touch screen.

Rc = 2500 Ω
Ry = 500 Ω
Ce = 0.01 uF

The touch screen total resistance R and the total capacitance C of the noise reduction capacitor are calculated as follows.

R = Rc + Ry / 2 = 2500 + 500 / 2 = 2750 [Ω]
C = 2 * Ce =2 * Ce = 2 * 0.01 * 10^{-6} = 0.02 [uF]

For these value, we can get

ts = - R * C * ln(1-0.999) = 380 [us]

The 380us is equal to 28 SIB frame.

$380 * 10^{-6} * 72 * 10^{3} = 27.4$ [frames]

This time represent necessary time period for the voltage sampling. In addition, 9us (about 1 frame) is needed for tracking time of 10 bit ADC. 29 frames is necessary for stable measurement in total. However this example is just only for the case that Vp is stable. In an actual application, since a pen is up and down and Vp always change. Therefore, the 29 frame settling time is not sufficient depending on the situation. Oppositely, there is a case that Vout reach Vp within much shorter time than 29 frames. Assuming such a case, we recommend to average an output code by using repeated measurement or median filtering and so on. Decide the capacitor value of Ce after evaluating system stability.

Figure 5.11.F shows a block diagram of the touch-screen interface. The bias voltage, GND, and high-impedance state can be set independently for each pin. The bias voltage is supplied from an internal bias voltage generating circuit. The TSCENA [W:9:11] can be used to enable/disable this bias voltage generating circuit. In case of measuring a position, enable the bias voltage generating circuit after setting an operation mode to position measurement mode by TSCMOD. In touch detection mode, VDD is supplied in place of the bias voltage. When in touch detection mode, this VDD is supplied automatically by an internal decoder by decoding the TSCMOD. At this time, the bias voltage generating circuit is disabled using TSCENA to prevent the conflict with VDD and the bias voltage output. Set an operation mode to touch detection mode after disabling the bias voltage generating circuit by TSCENA.

Use TS**GND [W:9:7-4] and TS**POW [W:9:3-0] to set the pin status. The internal decoder controls the select switch by decoding the TS**GND and TS**POW. Table 5.11.B shows the relationship between control codes and results for the TSPY pin.

When applying a voltage to the touch-screen, choose the bias voltage or GND for the corresponding pin. When measuring the touch-screen voltage, set a high-impedance state for the pin status first, then choose the pins to be measured using ADCIN [W:A:4-2], and feed the measured voltage into the internal 10-bit ADC. The internal multiplexer has general-purpose analog input pins AIN0 through AIN3 also connected to it, so that these general-purpose inputs can be selected using ADCIN. If measuring the terminal voltage of any of the touch screens, TSCMOD must specify the position measurement mode and one of TSPY, TSMY, TSPX, or TSMX in ADCIN. In contrast, when measuring the terminal voltage of AIN0 to AIN3, set the operation mode selected in TSCMOD to either contact detection mode or position measurement mode. Select the terminal to be measured at ADCIN (one of AIN0 to AIN3).

The AIN0 to AIN3 pins have an input leakage current flowing in them if they are steadily subject to the application of a DC voltage (for example, connected directly to a backup battery for monitoring purposes). The amount of this input leakage current depends on which terminal is selected as the ADC input. The pin that have been selected for input to the 10-bit ADC by ADCIN for measurement purposes have a leakage current of approximately 20 μA (max) whereas the nonselected pins have a leakage current of approximately 10 μA (max). For applications that require power savings as in portable terminals, make sure the AIN0–AIN3 pins are not selected unless making measurement in order to minimize the device's power consumption. If the power consumption needs to be reduced further, separate from power supply by using an external device such as an analog switch.

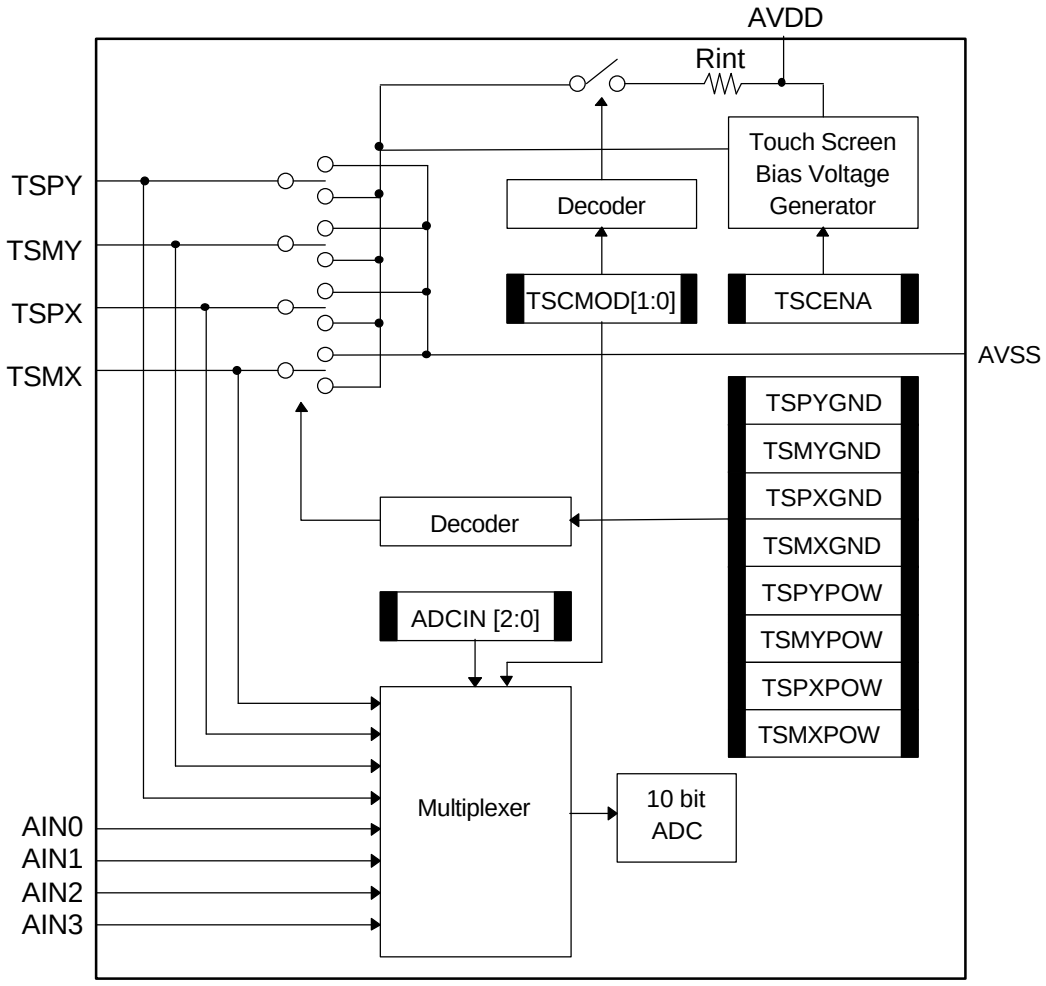


Figure 5.11.E Block diagram of touch-screen interface

Table 5.11.B Status Settings of TSPY

TSPYGND [W:9:7]	TSPYPOW [W:9:3]	TSPY Status
0	0	High impedance
0	1	Bias voltage
1	0	GND
1	1	GND

Table 5.11.C lists the contents of control for the X and Y plate position measurement, position calibration, and touch detection. Position measurement and position calibration are performed in position measurement mode. In position measurement mode, a bias voltage is applied to one plate and the other plate is set to an open state. The voltage on the open plate is measured using the 10-bit ADC. For touch detection, the power supply voltage is used in place of a typical bias voltage. In this case, therefore, the bias circuit must be disabled using TSCENA [W:9:11].

Table 5.11.C Detailed Contents of Settings in Each Mode

ITEM	TSPX	TSMX	TSPY	TSMY	TSC mode	TSC bias
X position measurement	**POW** TSPXGND=0 TSPXPOW=1	**GND** TSMXGND=1 TSMXPOW=0	**ADC input** TSPYGND=0 TSPYPOW=0	**ADC input** TSMYGND=0 TSMYPOW=0	**Position measurement mode** TSCMOD=[1,0]	**Enable** TSCENA=1
Y position measurement	**ADC input** TSPXGND=0 TSPXPOW=0	**ADC input** TSMXGND=0 TSMXPOW=0	**POW** TSPYGND=0 TSPYPOW=1	**GND** TSMYGND=1 TSMYPOW=0	**Position measurement mode** TSCMOD=[1,0]	**Enable** TSCENA=1
X position calibration	**POW** TSPXGND=0 TSPXPOW=1	**GND** TSMXGND=1 TSMXPOW=0	**ADC input** TSPYGND=0 TSPYPOW=0	**ADC input** TSMYGND=0 TSMYPOW=0	**Position measurement mode** TSCMOD=[1,0]	**Enable** TSCENA=1
Y position calibration	**ADC input** TSPXGND=0 TSPXPOW=0	**ADC input** TSMXGND=0 TSMXPOW=0	**POW** TSPYGND=0 TSPYPOW=1	**GND** TSMYGND=1 TSMYPOW=0	**Position measurement mode** TSCMOD=[1,0]	**Enable** TSCENA=1
touch detection	**POW** TSPXGND=0 TSPXPOW=1	**POW** TSMXGND=0 TSMXPOW=1	**GND** TSPYGND=1 TSPYPOW=0	**GND** TSMYGND=1 TSMYPOW=0	**Touch detection mode** TSCMOD=[0,0]	**Disable** TSCENA=0

Table 5.11.D Touch Screen Interface (Address9)

BIT	W/R	SYMBOL	BIT MEANING	DEF.
15 to 14	W	RESERVED	These are spare bits. Write a 0 to these bits.	0
	R	RESERVED	These are spare bits. They output a 0.	0
13	W	RESERVED	This is a spare bit. Write a 0 to this bit.	0
	R	TSMXLOW	This bit indicates the inverted level of the TSMX pin. 0: High level (pen-up state). 1: Low level (pen-down state).	0
12	W	RESERVED	This is a spare bit. Write a 0 to it.	0
	R	TSPXLOW	This bit indicates the inverted level of the TSPX pin. 0: High level (pen-up state). 1: Low level (pen-down state).	0
11	W	TSCENA	This bit enables or disables the touch-screen bias circuit. 0: Disabled. 1: Enabled.	0
	R	TSCENA	This bit indicates status whether the touch-screen bias circuit is enabled or disabled. 0: Disabled. 1: Enabled.	0
10	W	RESERVED	This is a spare bit. Write a 0 to it.	0
	R	RESERVED	This is a spare bit. It outputs a 0.	0
9 to 8	W	TSCMOD[1:0]	These bits set the operation mode of the touch-screen interface. 00: Touch detection mode. 01: Spare mode. 10: Position measurement mode. 11:Spare mode	0
	R	TSCMOD[1:0]	These bits indicate the setup operation mode of the touch-screen interface. 00: Touch detection mode. 01: Spare mode. 10 Position measurement mode. 11:Spare mode	0
7	W	TSPYGND	This is a control bit used to set the TSPY pin to GND. 0: Not set to GND. 1: Set to GND.	0
	R	TSPYGND	This bit indicates status of whether the TSPY pin is set to GND. 0: Not set to GND. 1: Set to GND.	0
6	W	TSMYGND	This is a control bit used to set the TSMY pin to GND. 0: Not set to GND. 1: Set to GND.	0
	R	TSMYGND	This bit indicates status of whether the TSMY pin is set to GND. 0: Not set to GND. 1: Set to GND.	0
5	W	TSPXGND	This is a control bit used to set the TSPX pin to GND. 0: Not set to GND. 1: Set to GND.	0
	R	TSPXGND	This bit indicates status of whether the TSPX pin is set to GND. 0: Not set to GND. 1: Set to GND.	0

4	W	TSMXGND	This is a control bit used to set the TSMX pin to GND. 0: Not set to GND. 1: Set to GND.	0
	R	TSMXGND	This bit indicates status of whether the TSMX pin is set to GND. 0: Not set to GND. 1: Set to GND.	0
3	W	TSPYPOW	This is a control bit used to set the TSPY pin to the bias voltage. 0: Not set to VDD. 1: Set to VDD.	0
	R	TSPYPOW	This bit indicates status of whether the TSPY pin is set to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
2	W	TSMYPOW	This is a control bit used to set the TSMY pin to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
	R	TSMYPOW	This bit indicates status of whether the TSMY pin is set to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
1	W	TSPXPOW	This is a control bit used to set the TSPX pin to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
	R	TSPXPOW	This bit indicates status of whether the TSPX pin is set to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
0	W	TSMXPOW	This is a control bit used to set the TSMX pin to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0
	R	TSMXPOW	This bit indicates status of whether the TSMX pin is set to the bias voltage. 0: Not set to the bias voltage. 1: Set to the bias voltage.	0

5.11.5 Control Procedure for Contact Detection

Fig. 5.11.G shows the control procedure for contact detection of the touch screen. With regard to procedure, execute this procedure without fail.

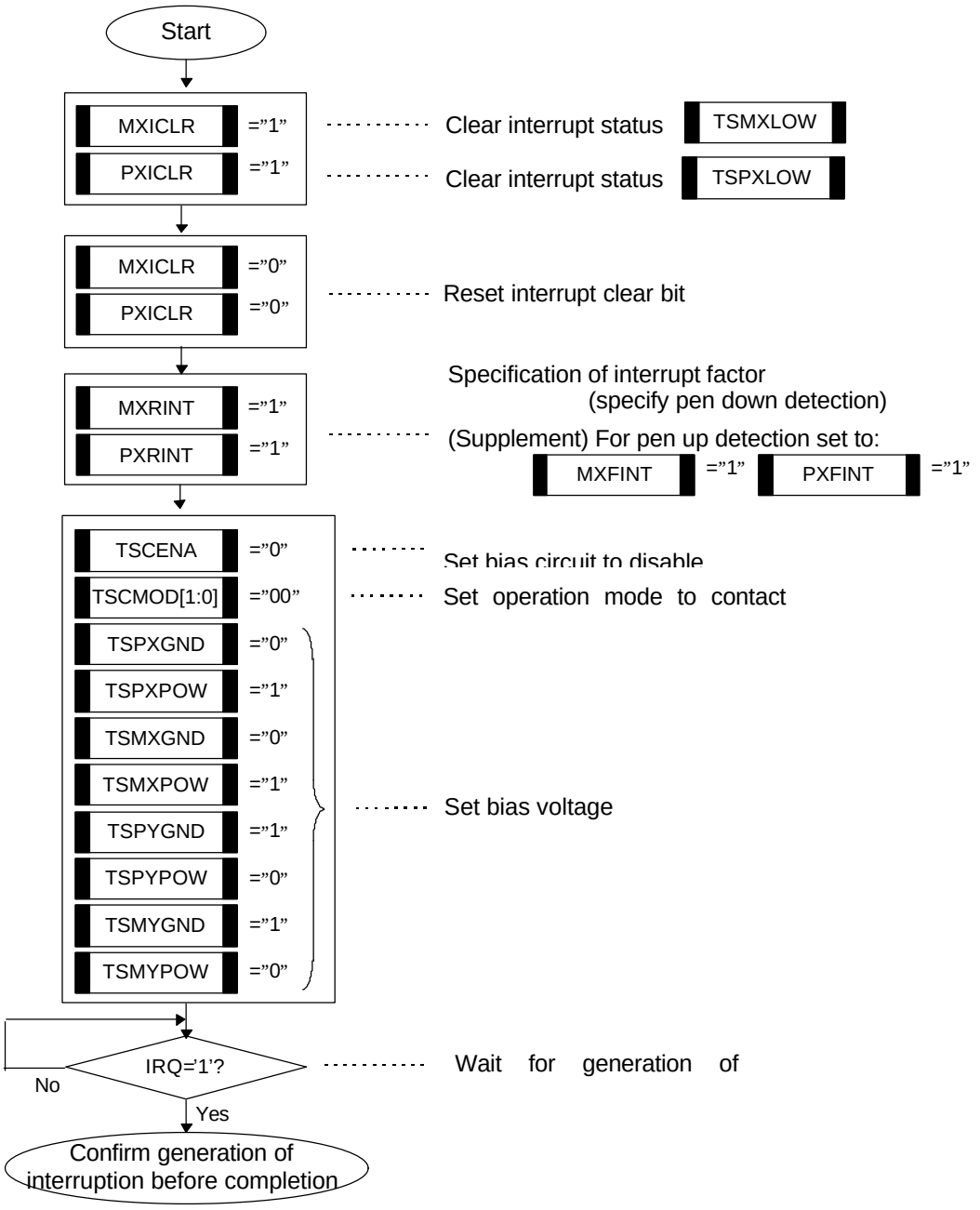


Figure 5.11.F Method of Controlling Contact Detection

5.11.6 Control Procedure for Position Measurement

Fig. 5.11.H shows the control procedure for X position measurement of the touch screen. With regard to control procedure, execute this procedure without fail.

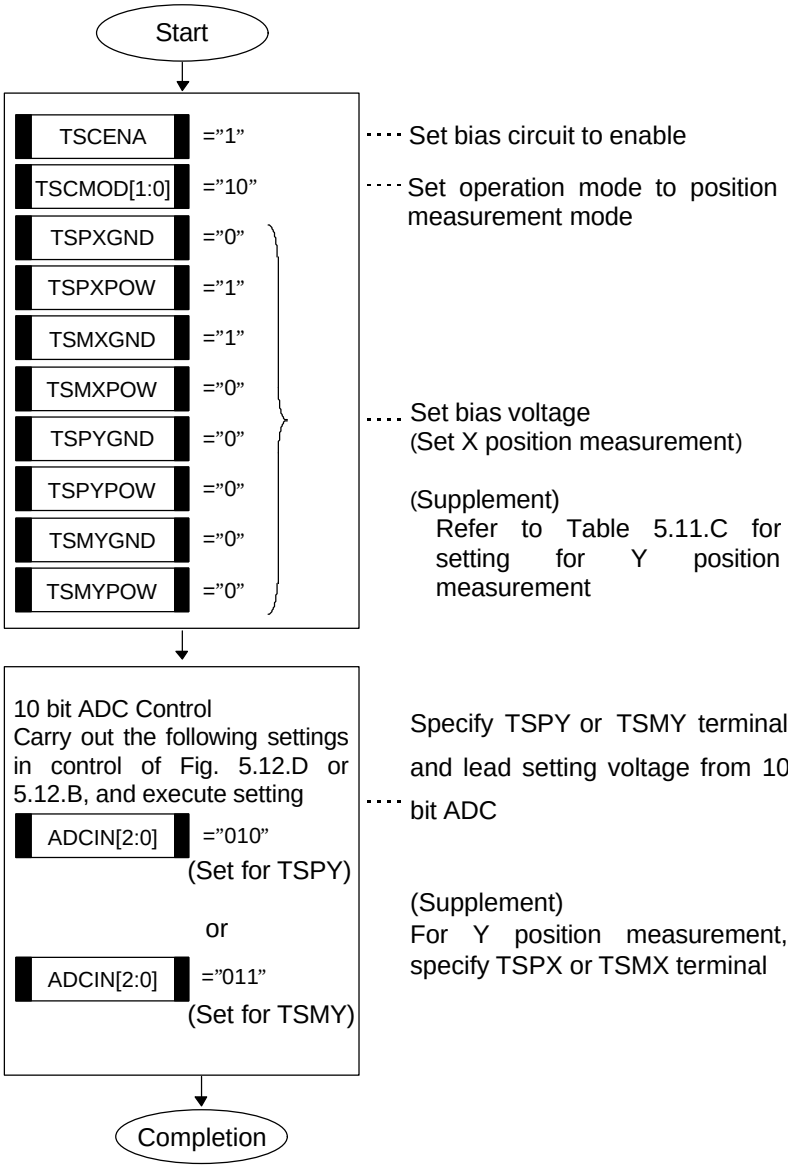


Figure 5.11.G X Position Measurement Control

5.12 10-bit AD Converter

The 10-bit ADC block consists mainly of an ADC, the input signal multiplexer and the sample-and-hold circuit, the control circuit, and the reference voltage generating circuit. This block is outlined in 5.12.1. Control procedures and timings detailed in 5.12.2.

5.12.1 Block Configuration

Figure 5.12.A shows a block configuration of the 10-bit ADC block.

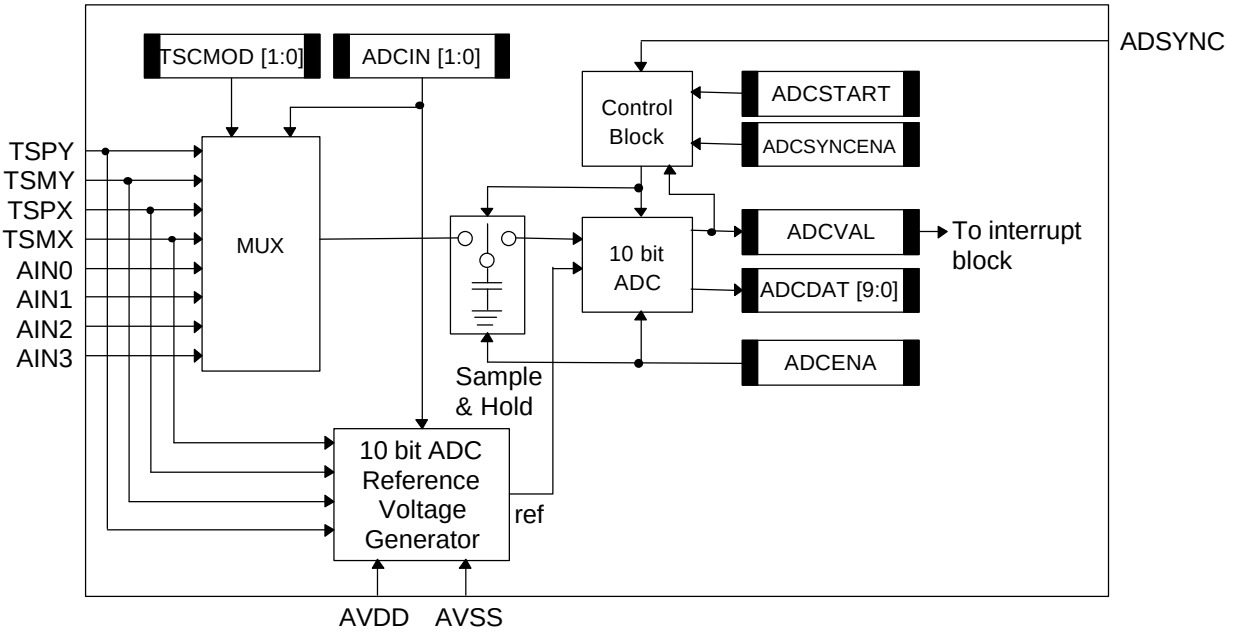
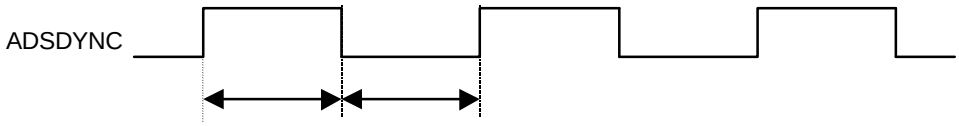


Figure 5.12.A Block diagram of 10-bit ADC system

Only one analog signal is selected for input to the ADC from touch-screen and general-purpose input signals. This selection is made using ADCIN [W:A:4-2]. If a touch-screen signal is selected, the position measurement mode must also be selected by TSCMOD [W:9:9-8].

The reference voltage supplied when a touch-screen signal is selected is the midpoint voltage of the voltage applied to the relevant plate. When a general-purpose input signal is selected, VDD/2 is supplied. The reference voltage thus supplied is automatically selected based on ADCIN setting code.

The sample-and-hold circuit synchronizes with the ADC and its operation is controlled by the control circuit. Before starting up the ADC, first enable it using ADCENA [W:A:15] and then set its operation mode using ADCSYNCENA [W:A:0]. There are two operation modes: asynchronous and synchronous. In asynchronous mode, the ADC conversion is started by a transition from 0 to 1 of ADCSTART [W:A:7]. Since ADCSTART can be set by the host processor asynchronously with the device operation, this mode is called the asynchronous mode. In synchronous mode, the ADC conversion is started according to the synchronizing pulse that is input from the ADSYNC pin. Even in synchronous mode, it is necessary that ADCSTART be set to 1. In case of the synchronous mode, input a signal whose high and low level period are more than 220ns as an input signal for ADSYNC. Especially when the duty ratio is different, take care to satisfy above specification. The condition of the ADSYNC input signal is shown in figure 5.12.B.



Both period High and low are equal to or more than 220ns.

Figure 5.12.B The condition which the ADSYNC signal needs

When conversion is completed, the ADC indicates the completion of conversion in ADCVAL [R:B:15]. The AD-converted data is presented to ADCDAT [R:B:14-5]. Since ADCVAL can be specified as an interrupt source, the host processor can easily be informed of the completion of conversion by this bit. For this specification, use ADCRINT [W:2:11] and ADCFINT [W:3:11].

Table 5.12.A 10 bit ADC control register (Address A)

BIT	W/R	SYMBOL	BIT MEANING	DEF.
15	W	ADCENA	This bit enables or disables the AD converter. The AD converter starts a sample-and-hold operation simultaneously when This bit goes to 1. Note 1 0 : Disabled. 1 : Enabled.	0
	R	ADCENA	This bit indicates setup status of whether the AD converter is enabled or disabled. 0: Disabled. 1: Enabled.	0
14 to 8	W	RESERVED	This is a spare bit. Set it to 0.	25h
	R	RESERVED	This is a spare bit. This indicates a 0.	25h
7	W	ADCSTART	This bit controls start of conversion. Conversion is started when this bit is set from 0 to 1 on asynchronous mode. On synchronous mode, the ADC starts the conversion at the first rising edge of ADSYNC pin after ADCSTART bit goes to 1.	0
	R	ADCSTART	This bit indicates the status of conversion start. 0: Conversion start is not under way. 1: Conversion start is under way.	0
6	W	RESERVED	This is a spare bit. Set it to 0.	0
	R	RESERVED	This is a spare bit. This indicates a 0.	0
5	W	EXREFENA	This bit selects the reference voltage. 0 : An internal reference voltage is used. 1 : An external reference voltage is used.	0
	R	EXREFENA	This bit indicates the selected reference voltage of the ADC. 0: The internal reference voltage is used. 1: An external reference voltage is used.	0
4 to 2	W	ADCIN[2:0]	These bit select the input signal of the 10-bit ADC. The relationship between ADCIN [2:0] and the selected pins is shown below. **ADCIN[2:0] / Input port / Comment** 0h / TSPX / Default 1h / TSMX 2h / TSPY 3h / TSMY 4h / AIN0 5h / AIN1 6h / AIN2 7h / AIN3	0h
	R	ADCIN[2:0]	These bits indicate the selected input signal of the 10-bit ADC. For details about code representation and the selected pins, refer to the write register described above.	0
1	W	RESERVED	This is a spare bit. Set it to 0.	0
	R	RESERVED	This is a spare bit. This indicates a 0.	0

0	W	ADCSYNCENA	This bit selects the AD converter's conversion mode between synchronous and asynchronous.Note 2 When the synchronous mode is selected, the ADC convert operation is synchronized to the pulses input from the ADSYNC pin. 0: Asynchronous mode. 1: Synchronous mode.	0
	R	ADCSYNCENA	This bit indicates the selected conversion mode of the AD converter. 0: Asynchronous mode. 1: Synchronous mode.	0

(Note 1) : If ADCENA is cleared to 0, the AD converter is reset and disabled. If this bit is cleared to 0 during conversion, ADCVAL [R:B:15] is set to 1 causing the output data to be updated. This data is invalid, so ignore it. In this case, if ADCSTART [W:A:7] is 1, be sure to clear it as something as ADCENA dearing.

(Note 2) : In asynchronous mode, conversion is started immediately after the sample-and-hold time that has been set times out. In synchronous mode, conversion is started synchronously with a high-going transition of ADSYNC (pin 5) after the sample-and-hold time that has been set times out.

Table 5.12.B 10 bit ADC Control Register (Address B)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15	W	RESERVED	This is a spare bit. Set it to 0.	0
	R	ADCVAL	This bit indicates the conversion status performed by the AD converter. 0 : Conversion in progress 1 : Conversion completed (The AD converter's output data (ADCDAT[9:0]) is updated.)	0
14 to 5	W	RESERVED	These are spare bits. Set them to 0.	0h
	R	ADCDAT[9:0]	These bits represent the output data of the AD converter.	0
4 to 0	W	RESERVED	These are spare bits. Set them to 0.	0h
	R	RESERVED	These are spare bits. They indicate a 0.	0

5.12.2 ADC Operation Timing

There are two ADC operation modes: asynchronous and synchronous. Typical control procedures in asynchronous and synchronous modes are shown in Figures 5.12.C and 5.12.E, respectively. Also, operation timing corresponding to these typical control procedures are shown in Figures 5.12.D and 5.12.F.

In both asynchronous and synchronous modes, we recommend using an interrupt for handshaking of the AD-converted data. Although it is possible to know the completion of the ADC conversion by polling ADCVAL, use of an interrupt helps to reduce the load on the host processor.

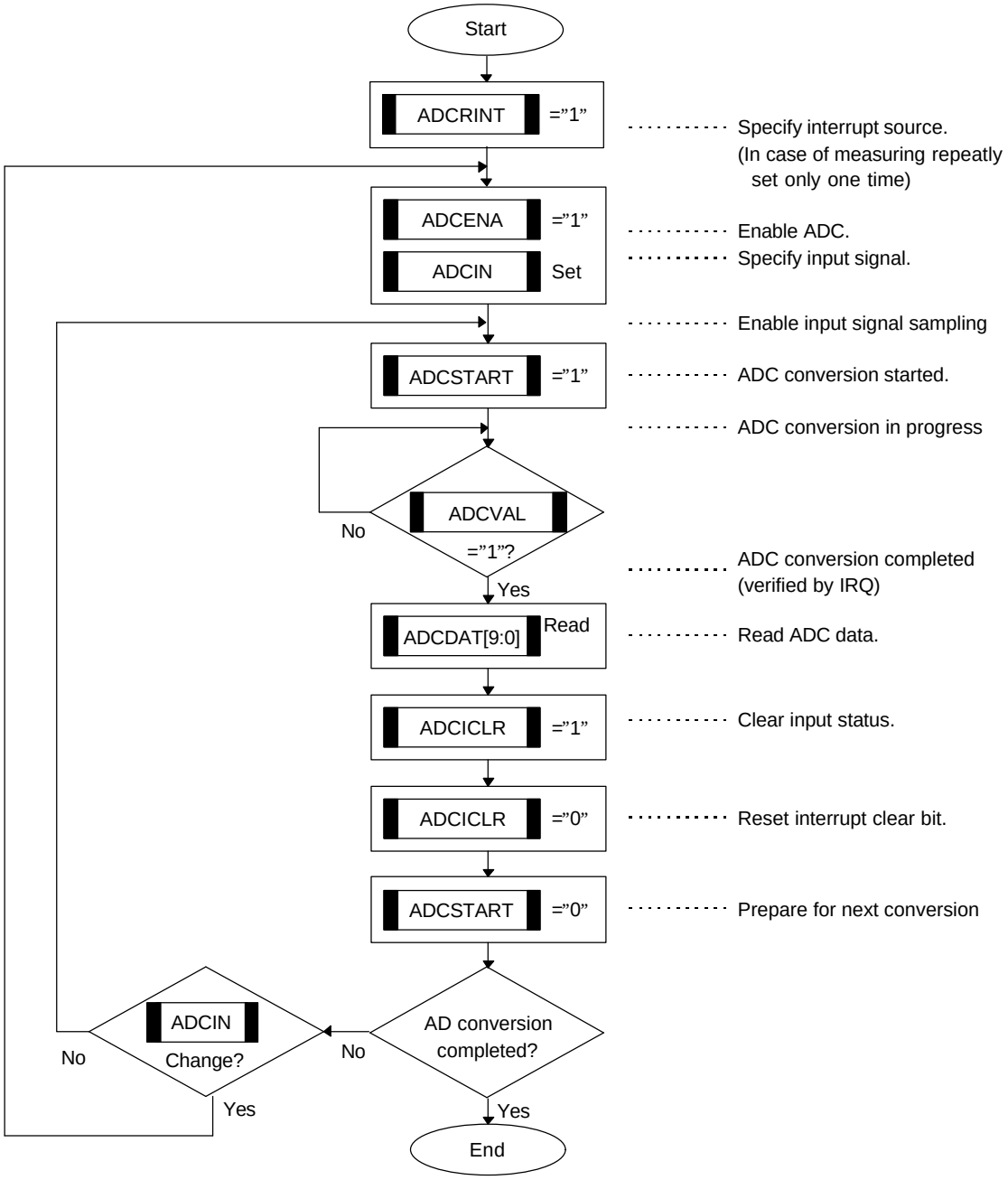


Figure 5.12.C Example of control procedure (in asynchronous mode)

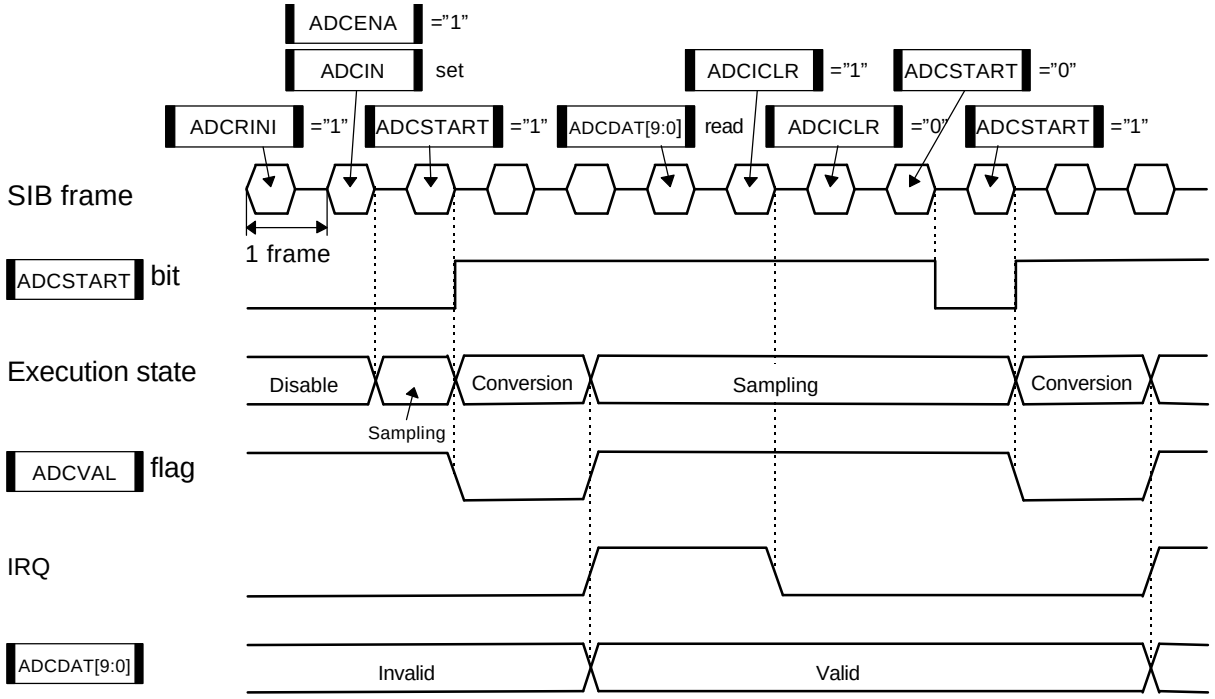


Figure 5.12.D Timing sequence (in asynchronous mode)

The following explains the control procedure in asynchronous mode.

First, specify the conversion status ADCVAL for an interrupt source using the ADCRINT bit. Then enable the ADC and set the pins whose voltage to be measured using the ADCENA bit and the ADCIN [2-0] bits. Make these settings in the same SIB frame. If the ADC operation mode is synchronous at this time, set ADCSYNCENA to 0 to change it for the asynchronous mode. When the ADC is enabled, the sample-and-hold circuit starts sampling the input signal. In asynchronous mode, the ADC conversion operation is started by a change of state from 0 to 1 of the ADCSTART bit. Simultaneously when the ADC starts converting, the sample-and-hold circuit goes to a hold operation. Since the minimum time required for sampling is one SIB frame period or less, ADCSTART can be set in any SIB frame once ADCENA and ADCIN [2-0] are set. When an interrupt from the IRQ pin is asserted, a host processor reads the converted data from the ADCDAT [9-0] bits. A host processor can check conversion end by polling statusthe the register. Conversion operation requires at least two SIB frame periods. Consequently, an interrupt request for the converted data occurs two SIB frames after ADCSTART is set. Read the ADCDAT bits beginning with the next frame after the interrupt request is generated. The data in the ADCDAT bits are retained until the next ADC conversion is performed. After reading the data, clear the interrupt status to prepare for the next conversion and set the ADCSTART bit to 0. The ADCSTART bit can be reset to 0 before reading the ADCDAT without causing any problem.

Before starting a next conversion, set the ADCSTART bit to 1 and perform conversion again.

To change the pins to be measured, change the settings of ADCIN and then set the ADCSTART bit to 1 to start conversion. The ADC does not need to be disabled before starting conversion. If a change of ADCIN settings and a setting of the ADCSTART bit (to start the ADC conversion) are made within the same SIB frame, there isn't sufficient time for sampling and you cannot obtain the correct conversion result.

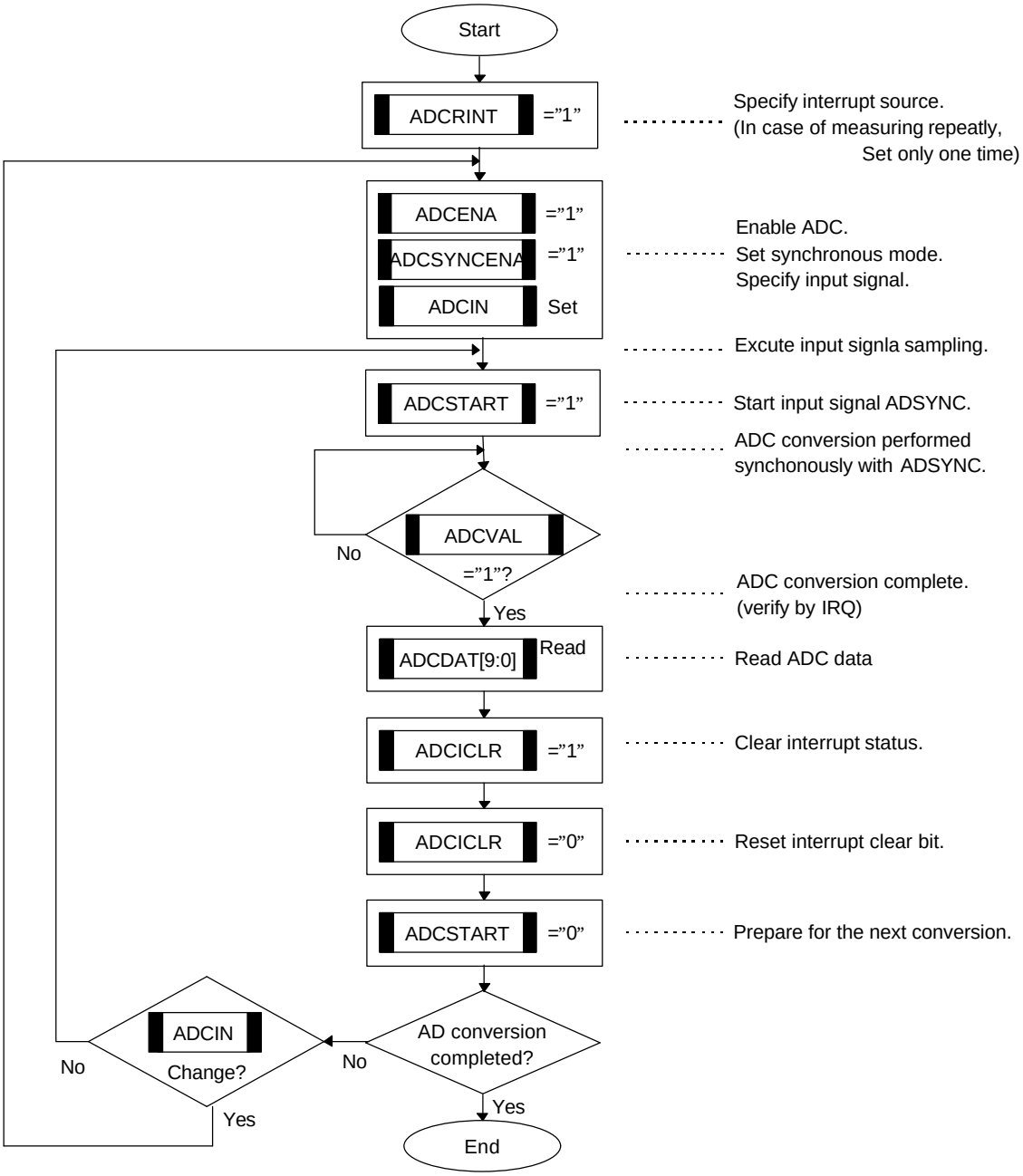


Figure 5.12.E Example of control procedure (in synchronous mode)

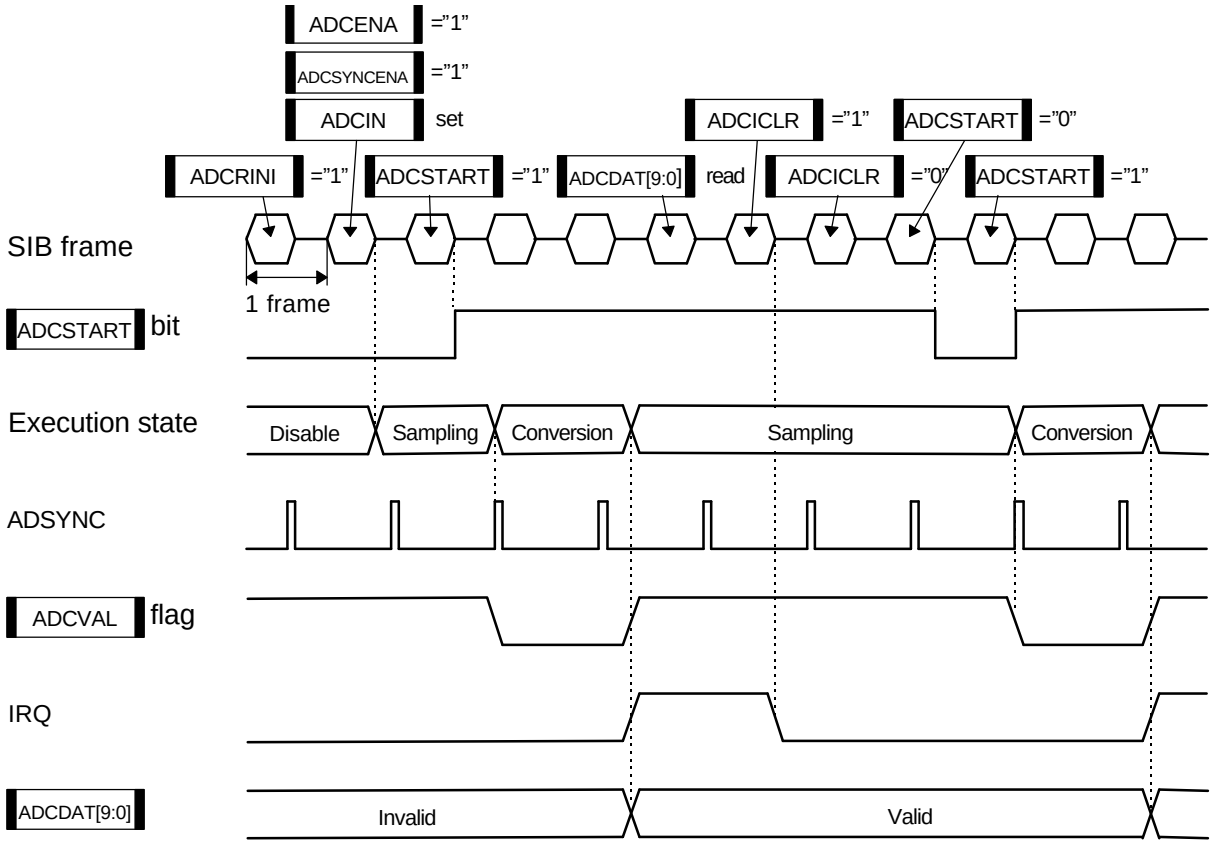


Figure 5.12.F Timing sequence (in synchronous mode)

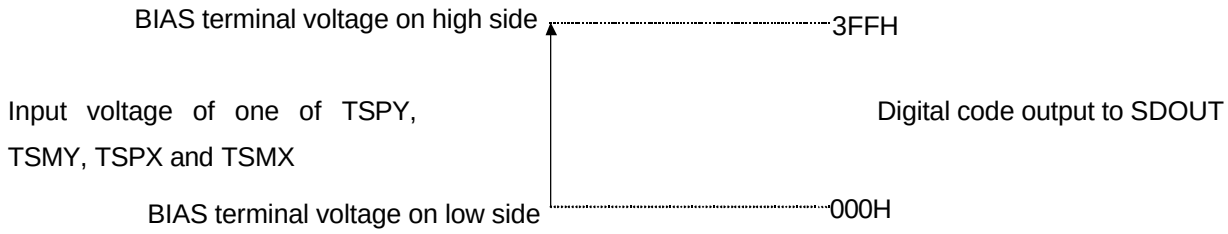
The control procedure in synchronous mode is almost the same as in asynchronous mode. The following explains the differences with the asynchronous mode.

Set the synchronous mode simultaneously when or in the prior SIB frame before enabling the ADC. To set the synchronous mode, set ADCSYNCENA to 1. Even in synchronous mode, it is necessary to set the ADCSTART bit to 1 to start conversion. Once this setting is made, the ADC starts converting synchronously with a rising edge of the first pulse input from the ADSYNC pin. The pulses input before ADCSTART is set to 1 are ignored and no conversion is performed. Also, the pulses input after conversion is started also are ignored. The procedure for handshaking of the converted data is entirely the same as in asynchronous mode. After reading the converted data, reset ADCSTART to 0 to prepare for the next data conversion as in asynchronous mode.

The synchronous mode is especially effective for reducing the effect of spike noise in the LCD driver. Generally, noise in the LCD driver gets mixed in the touch-screen due to capacitive coupling, etc. By entering the startup pulse to drive the LCD from ADSYNC, it is possible to avoid LCD drive timings when sampling the touch-screen voltage.

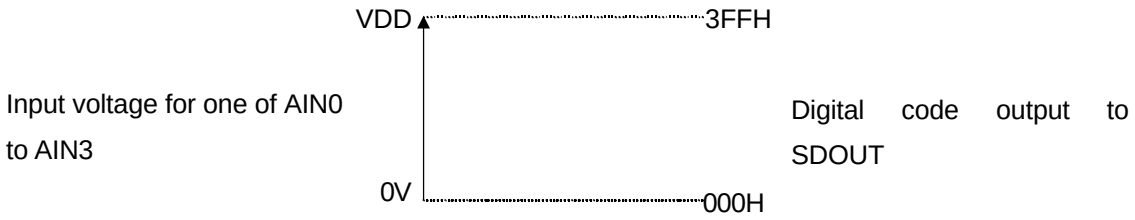
5.12.3 Relationship Between Analog Signal and Digital Code

Fig. 5.12.G and Fig. 5.12.H show the relationship between 10 bit ADC analog input and digital code. Fig. 5.12.G is the relational diagram for measuring the voltage of the TSPY, TSMY, TSPX, and TSMX terminals, while Fig. 5.12.H is therelational diagram for measuring the voltage of the four terminals from AIN0 to AIN3.



(Supplement 1) Digital code is integer expressions.
(Supplement 2) When measuring the voltage of the touch screen, the input range shall be the range of the BIAS voltage applied to the touch screen. BIAS voltage is determined by the resistance ratio between the output resistance of TC35143F and the resistance network of the touch screen, so the analog input range fluctuates.

Figure 5.12.G Relationship Between Touch Screen Input Voltage and Digital Code



(Supplement 1) Digital code is integer expressions.
(Supplement 2) When measuring AIN0 to AIN3, the analog input range is fixed.

Figure 5.12.H Relationship Between General-purpose InputVoltage and Digital Code

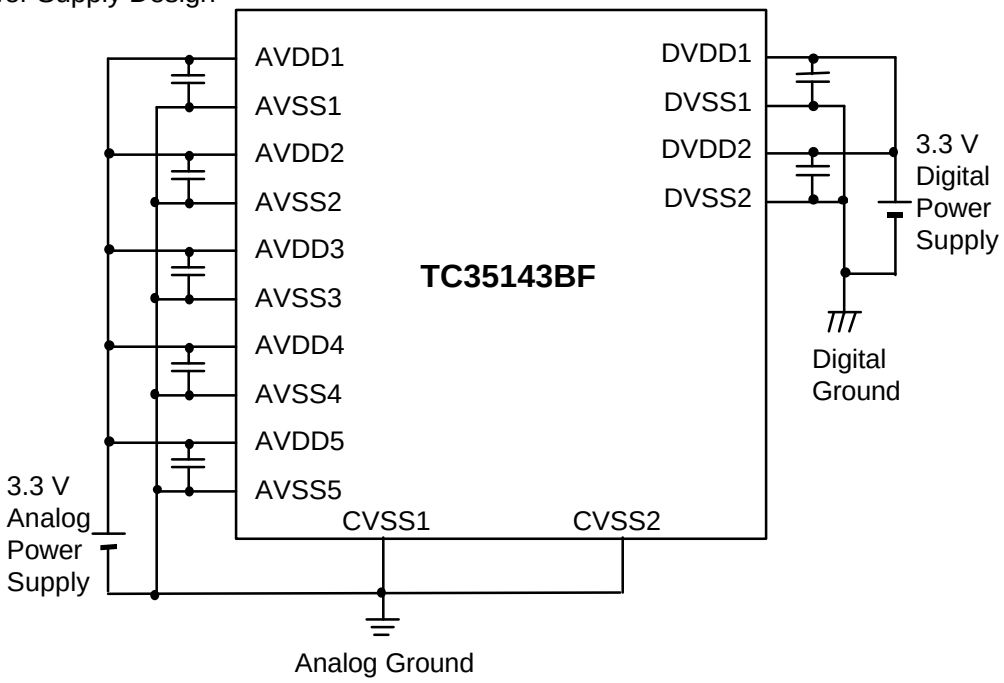
5.13 DATE Register

This register indicates the date (year/month) when the product was developed. This facility is useful for version management.

Table 5.13.A DATE Register (Address C)

BIT	R/W	SYMBOL	BIT MEANING	DEF.
15 to 0	W	RESERVED	This is a spare bit. Leave it to 0.	0
	R	DATE	Indicates the year and month when the product was developed in binary. This version indicated here is 9712h, meaning that the product was developed in December 1997. DATE[15:8] : Indicates the two low-order digits of a calendar year. DATE[7:0] : Indicates a month.	9712h

5.14 Power Supply Design



(Note) Analog Ground and Digital Ground should be connected to common ground at a single point.

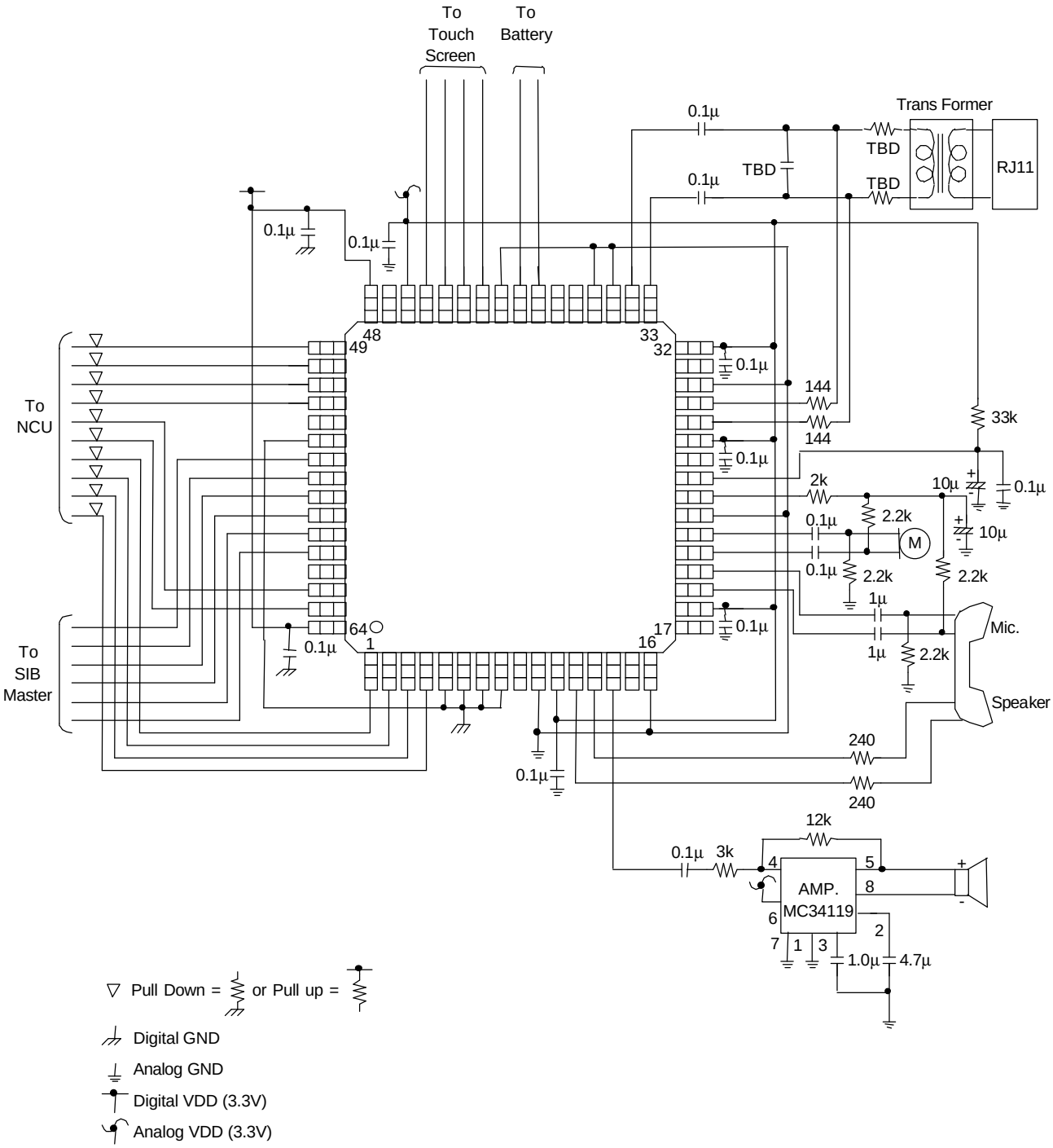
Figure 5.14.A Recommended power supply design

Figure 5.14.A shows a recommended power supply layout diagram. The TC35143BF contains five channels of analog and one channel of digital power supply circuits. For the analog unit, the five channels of power supply circuits are connected independently to five pairs of power supply pins. For the digital unit, two pairs of power supply pins are connected internally.

As an example method for connecting the power supply pins on the board, Toshiba recommends separating them into two power supplies, one for analog and one for digital, and connecting the analog and digital grounds to one common ground on the board as shown in Figure 5.14.A. For each of the two pairs of digital and five pairs of analog power supply pins, insert a bypass capacitor of about 0.1 μF between VDD and GND as close to the pins as possible.

For the analog input/output signals too, connect external devices as close to the input/output pins as possible using wiring patterns of at least 0.1 inch in width.

5.15 Example Circuit Drawing



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Item	Symabol	Rating	Unit
Power supply voltage	V_{DD}	V_{SS} – 0.5 to V_{SS}+4.0	V
Input voltage	V_{IN}	V_{SS} – 0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS} – 0.5 to V_{DD}+0.5	V
Input current	I_{IN}	10	mA
Output current	I_{OUT}	10	mA
Power dissipation	P_D	300	mW
Storage temperature	Tstg	-55 to +125	°C
Lead temperature(10 sec.max.)	T_L	260	°C

6.2 Recommended Operating Conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage	V_{IN}		0		V_{DD}	V
Serial clock (Master clock)	SCLK	V_{DD}=3.3 V±10 %		9.216		MHz
Master clock frequency deviation	SCLKΔf	V_{DD}=3.3 V±10 % fclk=9.216 MHz			100	ppm
Master clock duty rate	$SCLK_{Duty}$	V_{DD}=3.3 V±10 % fclk=9.216 MHz	45	50	55	%
Operating temperature	Topr		0		70	°C

$DV_{SS} = AV_{SS} = 0$ V

6.3 DC Characteristics

V_{DD} = 3.3 V±10 %, Ta = 25°C

Parameter	Symbol	Pin Name	Condition	MIN	TYP.	MAX	Unit
Current consumption when operating	I_{DDO}		V_{DD}=3.3 V All functional blocks operating		32		mA
Current consumption when idle	I_{DDS}		V_{DD}=3.3 V All functional blocks turned off, SCLK turned off		10		uA
Low level input voltage	V_{IL}	GPIO9 to GPIO0, SSYNC, SSYNC, SCLK, SDIN, -RST, ADSYNC	V_{DD}=3.0 V			0.3 V_{DD}	V
High level input voltage	V_{IH}	Same as V_{IL}	V_{DD}=3.6 V	0.7 V_{DD}			V
Low level input current (1)	$I_{IL}(1)$	SSYNC, SCLK, SDIN, -RST, ADSYNC	V_{IN}=V_{SS}	-1.0			uA
High level input current (1)	$I_{IH}(1)$	Same as $I_{IL}(1)$	V_{IN}=V_{DD}			1.0	uA
Low level input current (2)	$I_{IL}(2)$	VREF **1	V_{IN}=V_{SS}	-80			uA
High level input current (2)	$I_{IH}(2)$	Same as $I_{IL}(2)$	V_{IN}=V_{DD}			30	uA
Low level input current (3)	$I_{IL}(3)$	AIN0 to AIN3 **2	V_{IN}=V_{SS}	-10			uA
High level input current (3)	$I_{IH}(3)$	Same as $I_{IL}(3)$	V_{IN}=V_{DD}			10	uA
Low level input current (4)	$I_{IL}(4)$	AIN0 to AIN3 **3	V_{IN}=V_{SS}	-20			uA
High level input current (4)	$I_{IH}(4)$	Same as $I_{IL}(4)$	V_{IN}=V_{DD}			20	uA
Low level input current (during input state)	I_{DL}	GPIO9 to GPIO0	V_{IN}=V_{SS}	-1.0			uA
High level input current (during input state)	I_{DH}	Same as I_{DL}	V_{IN}=V_{DD}			1.0	uA
Low level output current (1)	$I_{OL}(1)$	GPIO9 to GPIO0	V_{OL}=0.4 V	1.8			mA
High level output current (1)	$I_{OH}(1)$	Same as $I_{OL}(1)$	V_{OH}=2.4 V			-1.8	mA
Low level output current (2)	$I_{OL}(2)$	SDOUT	V_{OL}=0.4 V	4			mA
High level output current (2)	$I_{OH}(2)$	Same as $I_{OL}(2)$	V_{OH}=2.4 V			-4	mA
Analog reference voltage	Vref	VREF	V_{DD}=3.3 V		1.35		V
Microphone bias voltage	Vmicb	MICBIAS	V_{DD}=3.3 V		2.0		V
Touch-screen bias voltage	Vfsc	TSMX, TSPX TSMY, TSPY	V_{DD}=3.3 V		1.9		V

* The digital input pins are CMOS-level input pins.

**1 : All functional blocks are turned off, with an external reference voltage used.

**2 : All functional blocks are turned off, with the 10-bit AD converter input path not selected.

**3 : All functional blocks are turned off, with the 10-bit AD converter input path selected.

6.4 AC Characteristics

6.4.1 Serial Interface Timing

SCLK=9.216 MHz, V_{DD} = 3.3V±10 %, Ta=25°C

Item	Symbol	Pin name	Condition	MIN.	TYP.	MAX.	Unit
Serial data output delay time	Tphl Tplh	SDOUT SCLK	C_L=80 pF		20		ns
Serial data data setup time	Tset	SDIN SCLK	C_{IN}=80 pF		20		ns
Serial data data hold time	Thold	SDIN SCLK	C_{IN}=80 pF		20		ns

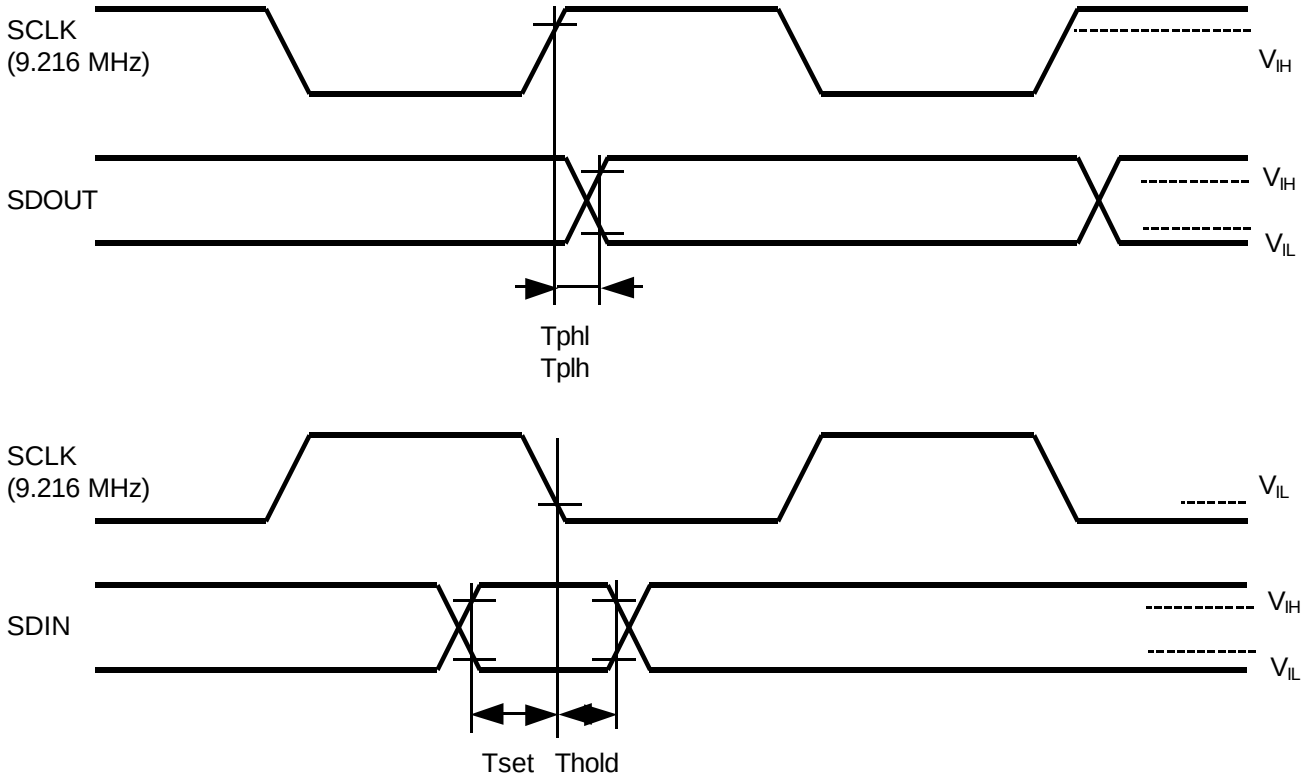
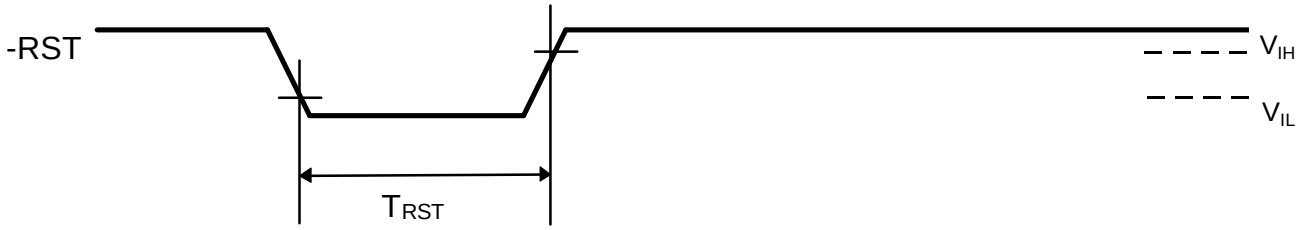


Figure 6.4.A

6.4.2 Reset Pulse Timing

V_{DD} = 3.3V±10 %, Ta=25°C

Item	Symbol	Pin name	Condition	MIN.	TYP.	MAX.	Unit
Minimum reset pulse width	T_{RST}	-RST	C_{IN}=80 pF	20			ns



6.4.3 Telecom Interface

Table 6.4.A Specification of Telecom Input

V_{DD}=3.3 V±10 %, Ta=25 °C

Item	Condition	Specification			
		min	typ.	max	Unit
S/N+D	S=+0dBm sine wave	70	80		dB
	S = -43dBm sine wave	32	37		dB
Resolution			16		bit
Full scale input	Differential(Gain=0dB)		4.00		Vpp
DC offset	Both inputs terminated		±10		mV
ADC gain variation		-1.5		1.5	dB
Cross talk	DAC output +2dBm	80	95		dB
Pass band ripple		-0.6		0.6	dB
Stop band rejection			60		dB
PSRR	200mVpp sine wave		50		dB
Input impedance			20		kΩ
Gain tracking error (1)	TAMP	-0.3		0.3	dB
Gain tracking error (2)	TGAIN	-0.3		0.3	dB

Table 6.4.B Specification of Telecom Output

V_{DD}=3.3 V±10 %, Ta=25 °C

Item	Condition	Specification			
		min	typ.	max	Unit
S/N+D	S = 0dBm sine wave	65	70		dB
200 to 3.6kHz	S = -43dBm sine wave	34	36		dB
Resolution			16		bit
Full scale output	Differential (ATT=0dB)		4.4		Vpp
Cross talk	+2dBm input to ADC	80	95		dB
DAC gain variation	4.4_{VP-P} output	-2.8		0.2	dB
Pass band ripple		-0.6		0.5	dB
Stop band rejection			60		dB
PSRR	200mV sine wave		40		dB
DC offset			±80		mV

Note) RL=600Ω differential

6.4.4 Voice Interface

Table 6.4.C Specification of Voice Input

V_{DD}=3.3 V±10 %, Ta=25 °C

Item	Condetion	Specification			
		min.	typ.	max.	Unit
Full scale input	Differential (Gain=0dB)		4.0		Vpp
DC offset	both inputs terminated VPGA1=0dB VPGA2=0dB		±10		mV
ADC Resolution			14		BIT
ADC Gain variation		-1.5		+1.5	dB
S/N+D	+2dBm sine wave VPGA1=0dB VPGA2=0dB	38			dB
	-43dBm sine wave VPGA1=0B VPGA2=0dB	24			dB
Idle channel noise	VPGA1=12dB VPGA2=0dB			-70	dBm0
Cross talk	DAC output +2dBm	80	95		dB
Pass band ripple		-0.6		0.6	dB
PSRR	200mVpp sine wave		40		dB
Input impedance			10		kΩ

Table 6.4.D Specification of Voice Output

V_{DD}=3.3 V±10 %, Ta=25 °C

Item	Condition	Specification			
		min.	typ.	max.	Unit
Full scale output for HSAMP	differential (ATT=0dB)		4.0		Vpp
Full scale output for SPAMP	differential (ATT=0dB)		4.0		Vpp
DAC DC offset	both inputs terminated		±80		mV
DAC resolution			14		BIT
DAC gain variation	4.0V_{P-P}output	-2.8		+0.2	dB
S/N+D	-2dBm sine wave HSATT=0dB SPATT=0dB	38			dB
	-43dBm sine wave HSATT=0dB SPATT=0dB	24			dB
Idle channel noise	0 digital code input			-72	dBm
Cross talk	DAC output +2dBm	80	95		dB
Pass band ripple		-0.6		0.6	dB
PSRR	200mVpp sin wave		40		dB
Load impedance	HSAMP	300			Ω
	SPAMP	2			KΩ
Attenuation tracking error(1)	HSAMP	-0.3		0.3	dB
	SPAMP	-0.3		0.3	dB
Attenuation trackign error(2)	DAATT	-0.3		0.3	dB

Note) VBO1 : R=300 Ω (differential)
VBO2 : R=2 KΩ (differential)

6.4.5 Touch Screen Interface

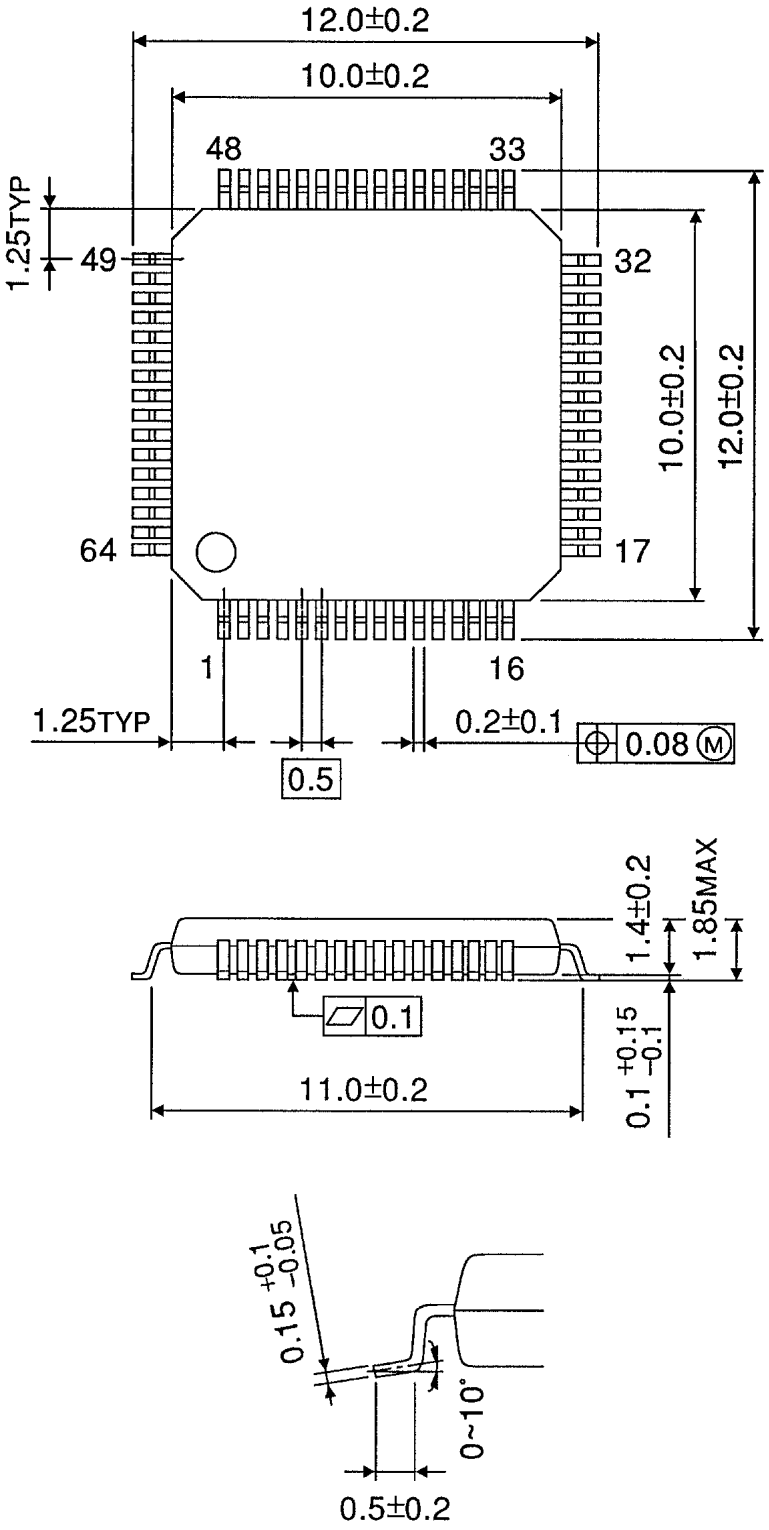
Table 6.4.E Specification of Touch Screen Interface

V_{DD}=3.3 V±10 %, Ta=25 °C

Item	Condition		Specification			
			Min.	Typ.	Max.	Unit
ADC resolution				10		bit
ADC linearity (AIN [3:0] input pins)	Chip surface temperature	10 bit ADC output code range				
	40°C > Ta ≥ 0°C	0 to 1023 LSB			±2	LSB
	60°C > Ta ≥ 40°C	0 to 31 LSB			+5	LSB
		32 to 991 LSB			±2	LSB
		992 to 1023 LSB			-5	LSB
	70°C ≥ Ta ≥ 40°C	0 to 31 LSB			+8	LSB
		32 to 991 LSB			±2	LSB
		992 to 1023 LSB			-8	LSB
ADC linearity (TCS input pins)					±2	LSB
ADC conversion time					20	us
ADC full scale input (TSC input pins)					TSC bias Voltage	V
ADC full scale input (AIN[3:0] pins)					V_{DD}	V
ADC tracking time			9			us
ADC input impedance				200		pF
ADC wake-up time					5	us
TSC bias voltage				1.9		V
TSC bias current				10		mA
Power / GND switch impedance				50		Ω
ADSYNC input	High level time period		220			ns
	Low level time period		220			ns

7. Outline Drawing

LQFP64-P-1010-0.50A



8. Reflow

8.1 Method of Solder Reflow

(1)Infrared Reflow

Regarding Near Infrared Reflow and V.P.S (Vapor phase solder), the reliability of device will be deteriorate remarkably. Therefore, we recommend Medium/Far Infrared Reflow with top/bottom heating.(refer to Figure.8.1.A) The soldering should be performed within 10 seconds at 240°C maximum on the surface of package. Figure 8.1.B shows recommended temperature profile. Near infrared Reflow give a heavy stress to device so that we forbid that.

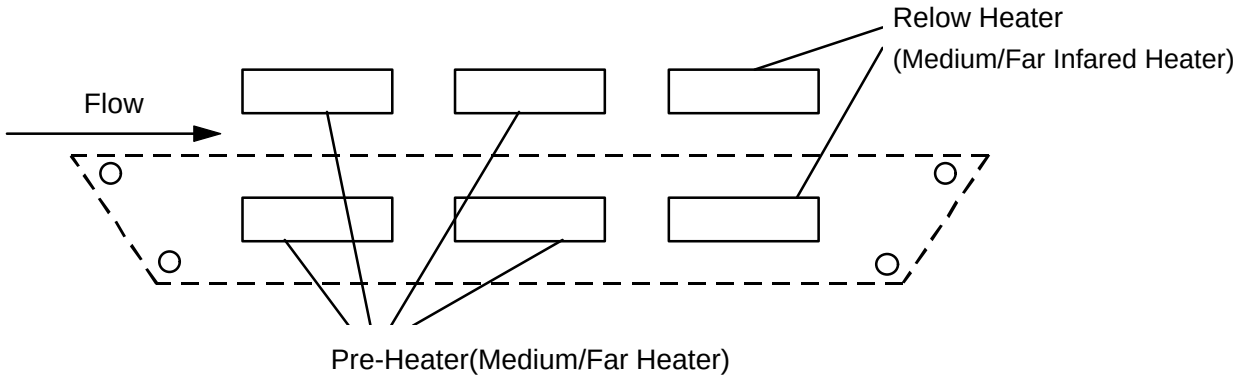


Figure 8.1.A Heating Mehtod

(2) Heating Air Reflow

The restraint and temperature profile is same as the case of Infrared Reflow. Figure.8.1.B shows recommended temperature profile.

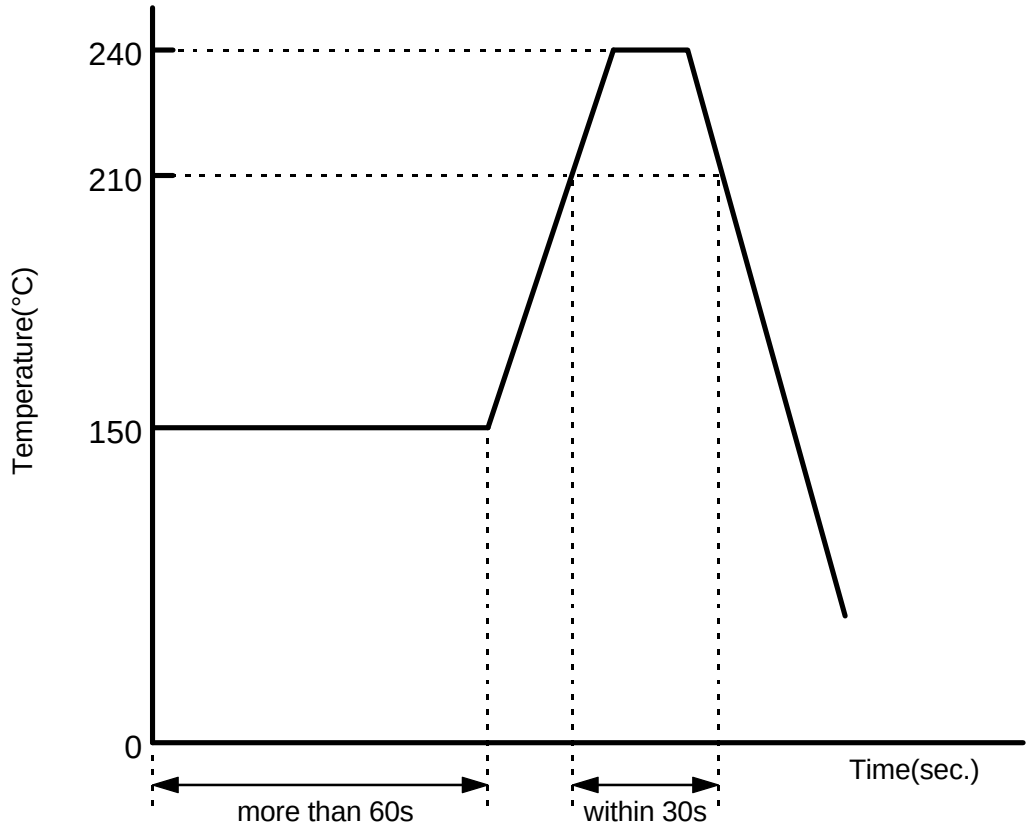


Figure 8.1.B

8.2 Dry Package

Dry packing is applied to TC35143BF. After the customer opens the bag, the parts must be mounted or soldered within 2 days under normal storage RH=60%, Ta=30°C.

If all the parts can not be soldered within the recommended period after opening the bag, pre-baking must be performed. The recommended pre-baking conditions are as follows :

Heat proof tray type 125°C/20hours baking with the original heat proof pack trays.