NIS3001

Integrated Driver and MOSFET Power Chip for Synchronous Buck Controllers

The NIS3001 is an integrated multi−chip solution for high power DC to DC synchronous buck converters. It contains two power MOSFETs that are controlled by an internal Driver. All three die are packaged in a power QFN package called PInPAK™. The 10.5 by 10.5 mm PInPAK™ package increases power density and simplifies PCB layout. The device can be used in single or multi−phase applications.

The NIS3001 implements the newest MOSFET technology. The control MOSFET is designed to provide improved switching performance and operates at a much lower temperature compared to discrete solutions. The synchronous MOSFET is designed to reduce conduction and switching losses at high frequencies. The integrated solution greatly reduces the parasitic inductance associated with conventional discrete buck converters and results in the highest power conversion efficiency.

The power density of the NIS3001 is optimized based on MOSFET die size and PInPAK design. The PInPAK layout allows for direct routing into each power terminal. This results in a better thermal solution for the system. In addition its thermal resistance is 50% lower than BGAs. In summary, the NIS3001 has an improved efficiency, reliability and scalability for multi−phase synchronous buck converters.

Features

- Matched MOSFETs for Optimal Efficiency
- 10.5 mm x 10.5 mm Power QFN Package, PInPAK
- 25 A DC Output Current
- 7.0 to 14 V Input Voltage Range
- Internal Thermal Shutdown
- Operating Frequency Range up to 1,000 kHz
- 0.7 V to 5.1 V Output Voltage Range
- Nominal Duty−Cycle 5% to 50%

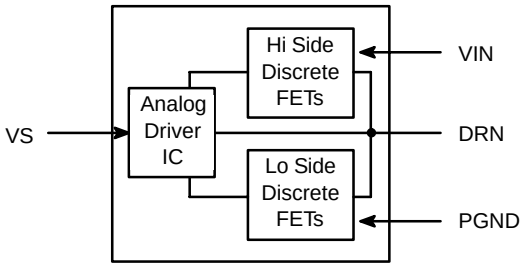
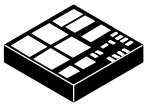


Figure 1.

ON Semiconductor®

http://onsemi.com

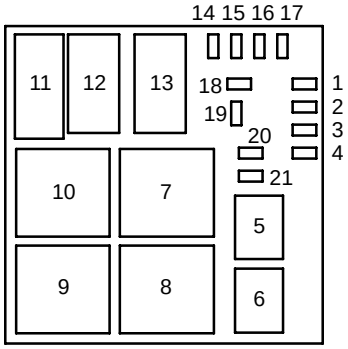


CASE 500
PInPAK
10.5x10.5 PLLP

MARKING DIAGRAM

NIS3001 = Specific Device Code
A = Assembly Site
WL = Wafer Lot
YY = Year
WW = Work Week

PINOUT DIAGRAM



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NIS3001QPT1	PInPAK	1500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

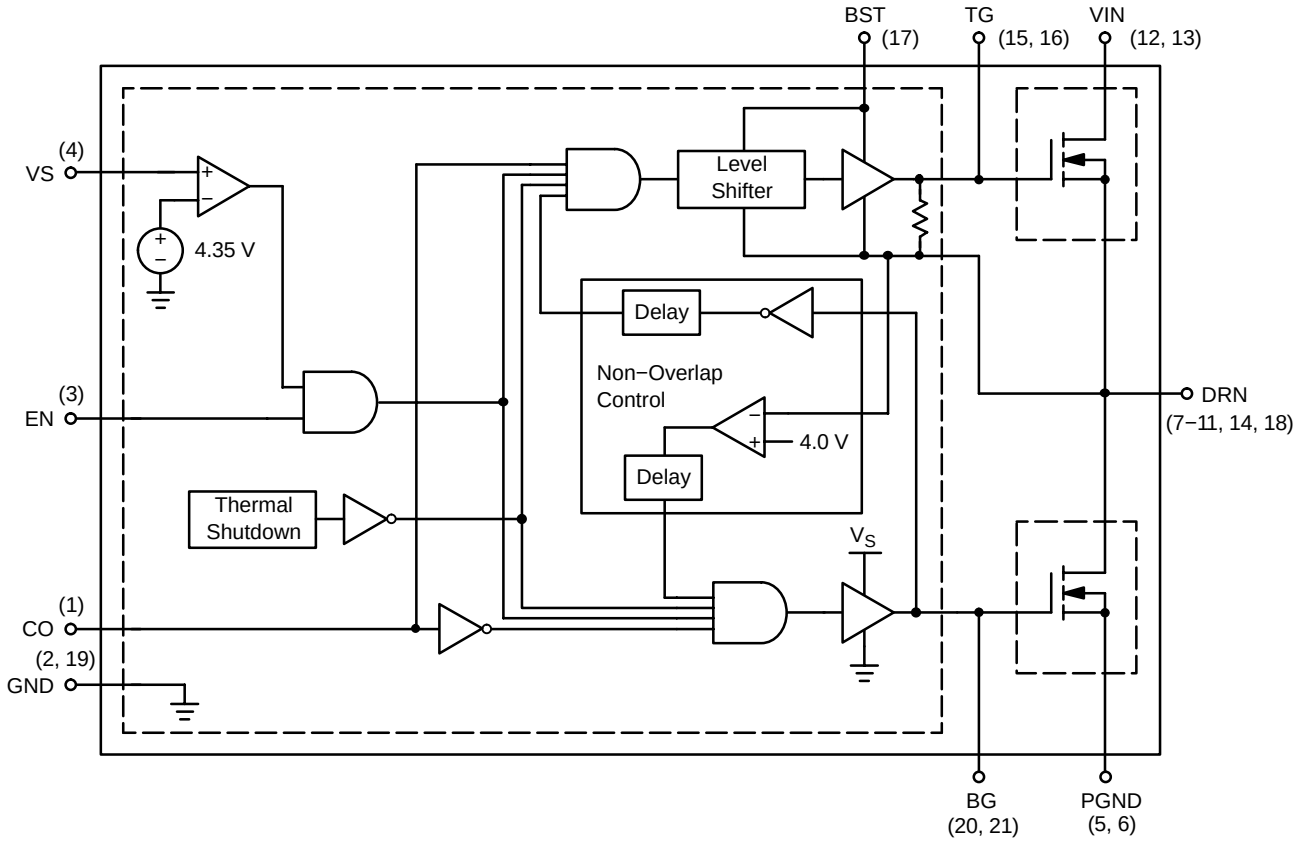


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTIONS

Pad #	Symbol	Description
1	CO	Logic level control input produces complementary output states.
2, 19	GND	Signal ground.
3	EN	Logic level enable input forces internal driver top gate and bottom gate low, and supply current to less than 10 μA when EN is low.
4	VS	Power supplied to the internal driver. A 1.0 μF ceramic capacitor should be connected from this pin to PGND.
5, 6	PGND	Power ground. High current return path for the lower internal.
7−11, 14, 18	DRN	Switching Node, connected to output inductor (10). Switching Node, connected to the boost capacitor (14). All pins connected internally.
12, 13	VIN	DC−DC converter input voltage.
15, 16	TG	High Side Driver Output (Top Gate, this pin is used to monitor the gate).
17	BST	Bootstrap supply voltage input. In conjunction with a Schottky diode to Vs, a 0.1 μF to 1.0 μF ceramic capacitor connected between BST and DRN (14).
20, 21	BG	Low Side Driver Output (Bottom Gate, this pin is used to monitor the gate).

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	125	°C
Output DC Current	25	A
Package Thermal Resistance: Junction to Ambient, $R_{\theta J-A}$ (4 layer PCB with vias, no air flow) Junction to Ambient, $R_{\theta J-A}$ (4 layer PCB with vias, 200lfm air flow) Junction to PCB, $R_{\theta J-PCB}$ (4 layer PCB with vias)	 26 13 8.0	°C/W
Storage Temperature Range, T_S	−65 to 150	°C
ESD Susceptibility (Human Body Model)	500	V
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C
JEDEC Moisture Sensitivity Level	3	MSL

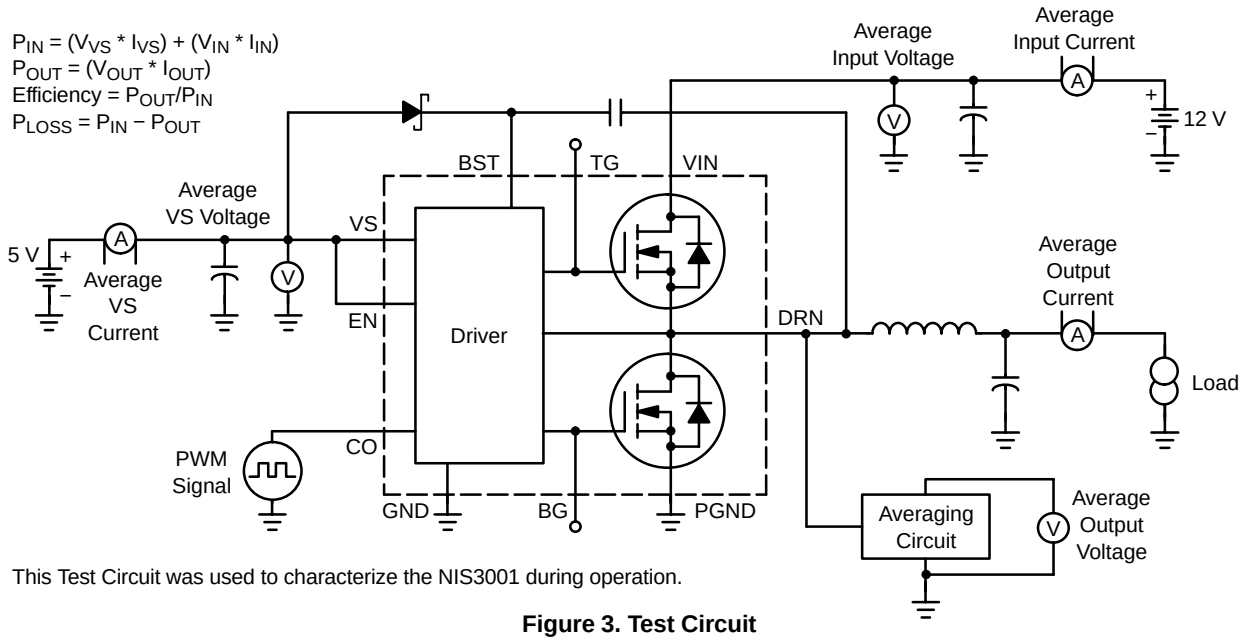
Pin Symbol	Pin Name	MAX	MIN	I_{SOURCE}	I_{SINK}
VS	Driver Supply Voltage	6.3 V	−0.3 V	NA	4.0 A Peak (< 100 μs) 250 mA DC
BST	Bootstrap Supply Voltage Input	25 V wrt/PGND 6.3 V wrt/DRN	−0.3 V wrt/DRN	NA	4.0 A Peak (< 100 μs) 250 mA DC
DRN	Switching Node (Bootstrap Supply Return)	25 V	−1.0 V DC −5.0 V for 20 ns −6.0 V for 20 ns	4.0 A Peak (< 100 μs) 250 mA DC	NA
TG	High Side Driver Output (Top Gate)	25 V wrt/PGND 6.3 V wrt/DRN	−0.3 V wrt/DRN	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
BG	Low Side Driver Output (Bottom Gate)	6.3 V	−0.3 V	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
CO	TG & BG Control Input	6.3 V	−0.3 V	1.0 mA	1.0 mA
EN	Enable Input	6.3 V	−0.3 V	1.0 mA	1.0 mA
PGND	Ground	0 V	0 V	4.0 A Peak (< 100 μs) 250 mA DC	NA
VIN	Input Supply Voltage	14 V	–	–	–

NOTE: All voltages are with respect to PGND except where noted.
1. 60 seconds maximum above 183°C.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS

(Test conditions unless otherwise noted; V_{IN} = 12 V, V_S = V_{BST} = V_{EN} = 5 V, F_{SW} = 500 kHz, V_{CO} = 4 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DC OPERATING SPECIFICATIONS					
Power Supply					
Power Loss V_{OUT} = 1.5 V, I_{OUT} = 4.5 A V_{OUT} = 1.5 V, I_{OUT} = 15 A	P_{LOSS}	 – –	 0.85 2.67	 – –	W
VS Operating Current (switching)	I_{VS}	–	19	–	mA
VS Quiescent Current, Shutdown, V_{EN} = 0 V	I_{VS}	–	10	–	μA
Bootstrap Operating Current (switching)	I_{BST}	–	7	10	mA
EN Input Characteristics					
Enable Input Bias Current	I_{EN}	–	1	–	μA
EN High Threshold, (Operating), V_{IN} = open	V_{EN}	2.0	–	–	V
EN Low Threshold, (Shutdown), V_{IN} = open	V_{EN}	–	–	0.8	V
Undervoltage Lockout					
Undervoltage Lockout, Turn on, (V_{CO} = V_{EN} = 4 V, V_{IN} = open)	UVLO	4.0	4.25	4.48	V
Undervoltage Lockout, Turn off, (V_{CO} = V_{EN} = 4 V, V_{IN} = open)	UVLO	3.7	4.0	4.3	V
Hysteresis for Undervoltage Lockout, (V_{CO} = V_{EN} = 4 V, V_{IN} = open)	V_{hyst}	–	275	–	mV
CO Input Characteristics					
CO Input Bias Current, (V_{IN} = open, V_{CO} = 4 v)	I_{CO}	–	3	–	nA
CO High Threshold, V_{IN} = open	V_{CO}	2.0	–	–	V
CO Low Threshold, V_{IN} = open	V_{CO}	–	–	0.8	V
Thermal Shutdown					
Overtemperature Trip Point		–	170	–	°C
Hysteresis		–	30	–	°C
AC OPERATING SPECIFICATIONS					
High−Side Driver					
Propagation Delay Time, TG Going High (Nonoverlap time); 50% between BG (going low) and TG (going high) V_{BST} − V_{DRN} = 5.0 V	$tpdh_{TG}$	–	45	–	ns
Propagation Delay Time, TG Going Low; 50% between CO (going low) and TG (going low) V_{BST} − V_{DRN} = 5.0 V	$tpdl_{TG}$	–	60	–	ns
Propagation Delay Time, BG Going High (Nonoverlap time); 50% between DRN (going low) and BG (going high)	$tpdh_{BG}$	–	43	–	ns
Propagation Delay Time, BG Going Low; 50% between CO (going high) and BG (going low)	$tpdl_{BG}$	–	8.0	–	ns
POWER MOSFET ON CHARACTERISTICS					
High−Side Driver					
Static Drain−to−Source On−Resistance (VGS = 5 V, ID = 20 A)	$R_{DS(on)}$	–	10.5	–	mΩ
Low−Side Driver					
Static Drain−to−Source On−Resistance (VGS = 5 V, ID = 20 A)	$R_{DS(on)}$	–	3.19	–	mΩ



This Test Circuit was used to characterize the NIS3001 during operation.

Figure 3. Test Circuit

TYPICAL PERFORMANCE CURVES

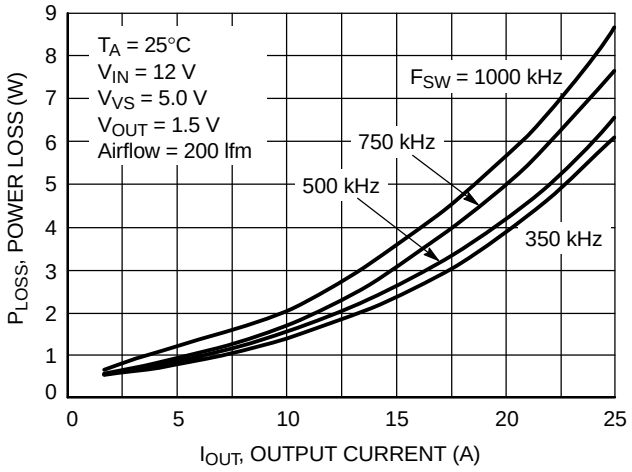


Figure 4. Power Loss versus Output Current

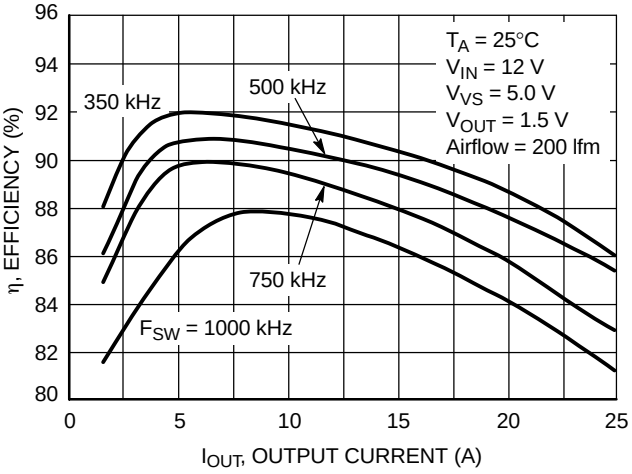


Figure 5. Efficiency versus Output Current

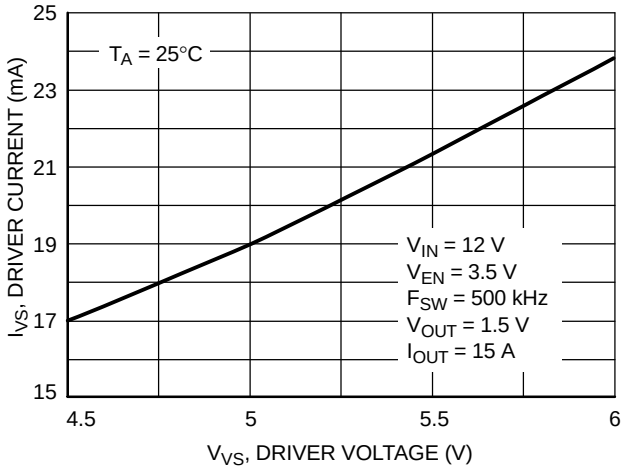


Figure 6. Driver Current versus Driver Voltage

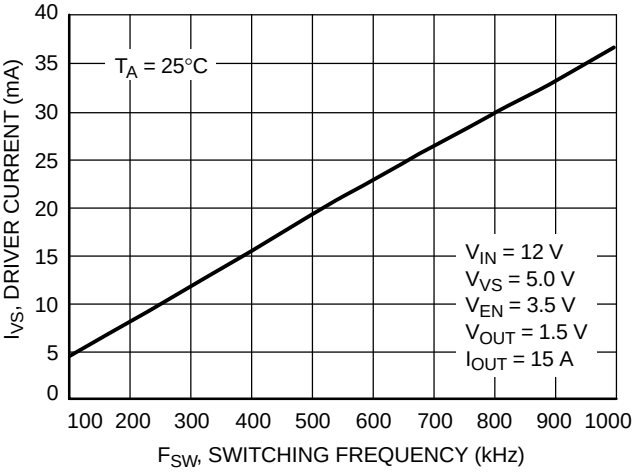


Figure 7. Driver Current versus Switching Frequency

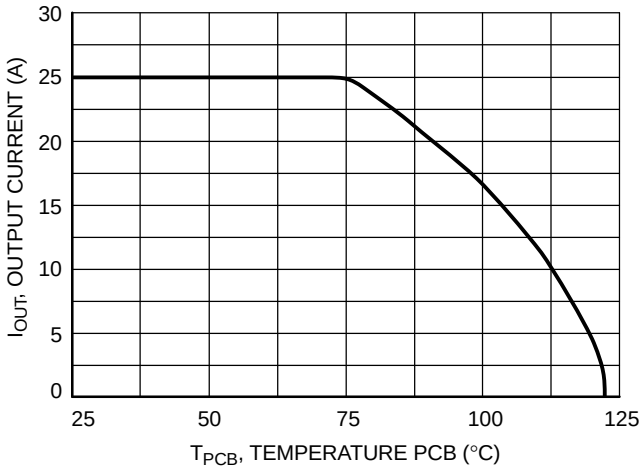


Figure 8. Safe Operating Area; Output Current versus Temperature PCB

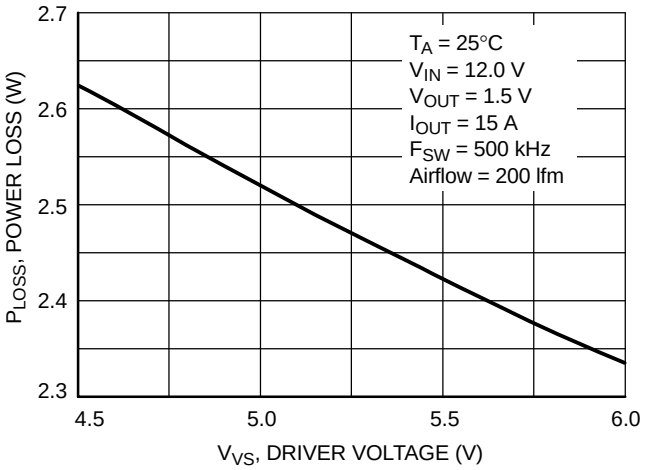


Figure 9. Power Loss versus Driver Voltage

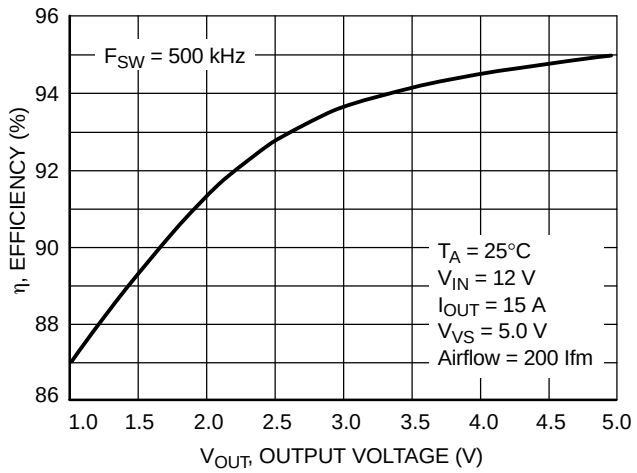


Figure 10. Efficiency versus Output Voltage

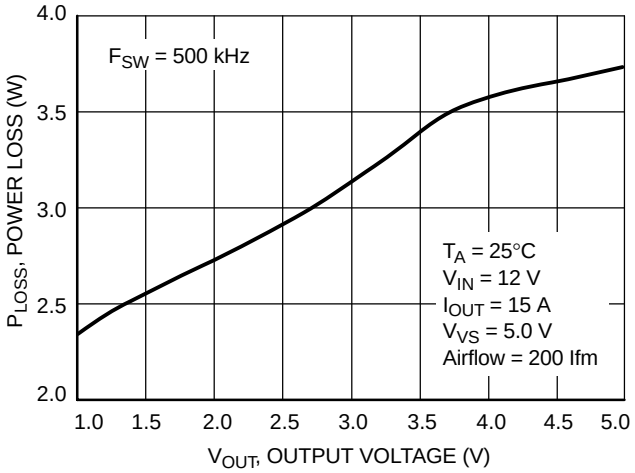


Figure 11. Power Loss versus Output Voltage

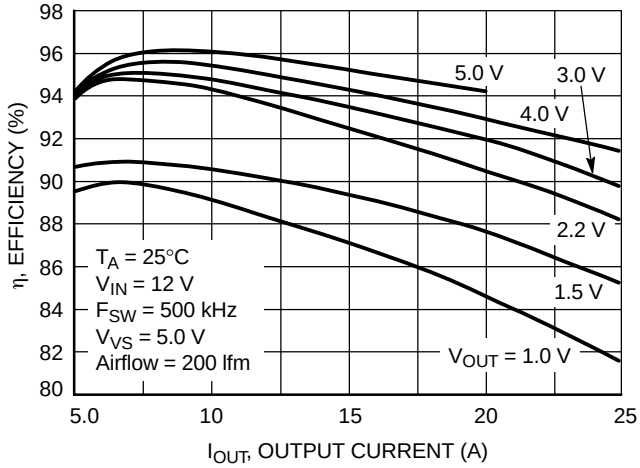


Figure 12. Efficiency versus Output Current at Different Output Voltages

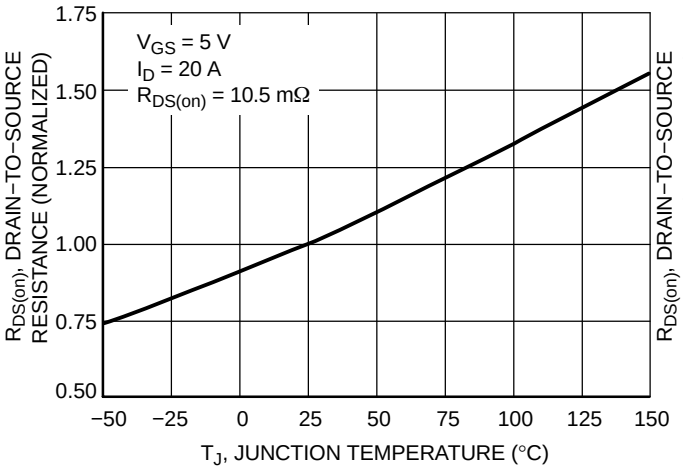


Figure 13. Top MOSFET On−Resistance Variation with Temperature

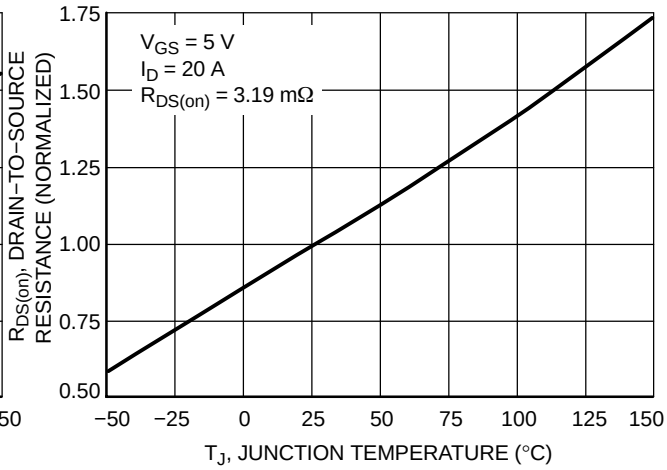


Figure 14. Bottom MOSFET On−Resistance Variation with Temperature

INTRODUCTION

The NIS3001 represents a significant improvement in high frequency power conversion, by combining a high performance driver with two power MOSFET devices for use in synchronous buck converters. All three die are assembled in a QFN package called a PInPAK.

This approach minimizes the parasitic elements in the power path by reducing the distance between the three devices. The leadless design also provides an excellent thermal path for the removal of heat which is generated during the power conversion process. All of these improvements result in a higher conversion efficiency when operation at high frequencies (350 kHz to 1000 kHz) is required. Operating at higher frequencies, reduces the number of electrolytic capacitors and the size of filter inductors required to meet load line and transient response requirements.

This device is designed to process power from a nominal 12 V source (ranging from 7 V to 14 V), while obtaining its internal bias power from a 5 V supply. The output voltage can range from 0.7 V to 5.1 V with a maximum duty cycle of 50%. It requires signal inputs from a synchronous buck controller, such as the NCP5316.

A minimum number of external components are required to create a complete power converter. Figure 15 is an example of a simplified solution.

Operational Description

Driver: The internal driver requires a nominal 5 volt bias voltage to operate. The bootstrap voltage is normally derived from this same source. The bootstrap circuit typically employs a schottky diode as part of the charge pump that provides the isolated supply voltage to the high side driver.

The driver uses several control functions to provide the correct gate drive signals. The control (CO) input accepts the drive signal from the synchronous converter PWM. The driver circuitry programs a delay between the top and bottom FETs, such that they will not conduct at the same time.

An enable pin (EN) allows the output of the driver to be shut down by a logic level signal. In this mode of operation, the bias current is reduced to a level of 10 μA. When the driver is disabled, the gates of both FETs are low and the drain (DRN) output of the NIS3001 is in a high impedance state.

To guarantee system integrity, the driver also incorporates an internal UVLO circuit. It is activated when the bias voltage reaches 4.25 volts, and will shut down the driver when if the bias voltage drops below 3.975 volts. In the UVLO shutdown condition, both FETs are off, and the DRN pin is in a high impedance state.

Power MOSFETs: The NIS3001 contains two power FETs which are directly connected to the internal driver chip. They have different on resistances and are designed for optimum performance for current VRM voltage and current requirements. The drain of the top FET is connected to the 12 volt input and the source is connected to the DRN pins. The drain of the bottom FET is also connected to the DRN pins, while its source is connected to the power ground pins.

Functional Pin Description

VS Pin: The VS pin connects to a nominal 5 volt supply and provides power to the driver chip. It is necessary to provide a bypass capacitor between 1.0 μF and 10.0 μF in close proximity to this pin and the ground (GND) pin. This capacitor allows a low impedance path for the high frequency currents that occur when the gate of the bottom FET switches. The voltage at this pin is monitored internally by the UVLO circuit which will disable the driver if there is not sufficient voltage available to assure proper operation of the driver.

VIN Pin: The VIN pin connects to the nominal 12 volt supply which provides power to the switching stage of the converter. It connects to the drain of the top FET, which is the controlled switch of the buck converter. This pin needs a combination of electrolytic and ceramic capacitors for bypass purposes.

Enable Pin: The EN pin accepts a logic level signal that can both source and sink current. There is no hysteresis on the signal switching levels for this pin, so care should be taken that the high and low logic levels of the driving signal should be above and below the switching points by several hundred millivolts.

In its high state, the driver is operational and will respond to inputs on the CO pin. In its low state, the driver is disabled. In this state, it enters a reduced power mode and turns off both FETs, thereby providing a high impedance output at the DRN pin.

A bypass capacitor is not normally required for the enable signal.

Control Pin: The CO pin accepts a logic signal from the PWM output of the controller chip. This signal is fed into the driver and controls the top and bottom FETs. When this pin is in a high state, the top FET is fully enhanced and the bottom FET is not conducting. When the signal is low, the bottom FET is fully enhanced and the top FET is not conducting.

During the switching transition, there is a non−overlap control circuit that is designed to provide optimum switching timing for the two FETs. This circuit eliminates the possibility of cross conduction, by monitoring the voltage on the DRN pin to time the turn−on of the bottom FET.

Bootstrap Pin: The BST pin connects to an external diode−capacitor circuit that acts as a charge pump to provide a floating, isolated voltage source for the high−side driver. A schottky diode is recommended, which charges the capacitor when the DRN pin is low. This diode is normally connected to the same source as the VS pin.

The capacitor (typically 0.2 to 1.0 μF) is connected from the BST to the DRN pin. The capacitor should be mounted as close as possible to the NIS3001 package. As there are

several DRN pins available, it is recommended that pin 14 be used because of its proximity to the BST pin.

Drain Pin: The DRN pin is also called the switch node. It is the connection between the source of the top FET and the drain of the bottom FET. This node is connected to one terminal of the output filter inductor. When the top FET is conducting, the DRN pin is essentially connected to the 12 volt source. When the bottom FET is conducting, this node is essentially connected to ground. When the driver is disabled, this node is in a high impedance state, and is essentially connected to neither.

Top Gate Pin: The TG pin is the internal connection of the output of the high−side driver and also the gate of the top FET. There is normally no connection to this pin. It can however, be used to drive an external FET which will operate in parallel with the top FET.

This pin may also be attached to the pcb for additional heat sinking or used to monitor the top gate waveform.

Bottom Gate Pin: The BG pin is the internal connection of the output of the lower driver and bottom FET gate. There is normally no connection to this pin, although it may be used for paralleling an additional FET, monitoring or heat sinking, similar to the TG pin.

Power Ground: The PGND pin is the power ground for the device. The source of the bottom FET is also connected to this pin. This pin is not internally connected to the GND pin and care should be taken when laying out the circuit to maintain proper isolation between these grounds.

Signal Ground: The GND pin is the ground pin for the driver, and is internally isolated from the PGND pin.

Layout Considerations

While the design of the NIS3001 reduces many of the parasitic elements when compared to a discrete solution, careful consideration to layout must still be observed. The following suggestions are offered:

a) Mount the bootstrap capacitor very close to the package. Use DRN pin 14 and BST pin 17 due to their proximity. The capacitor should be a high quality ceramic type.

b) Mount the VS pin bypass capacitor as close as possible to the package. This should be a high quality ceramic capacitor and is mounted between pins 4 and 2.

c) VIN requires a combination of bypass capacitors. These consist of both low ESR aluminum electrolytics and high quality ceramics. The ceramics should be SMT devices and mounted as close to the VIN and PGND pins as possible. The aluminum capacitors are generally located slightly farther away, but should be connected via power and ground planes to maintain the lowest possible impedance. The total amount of capacitance required is dependant on the system requirements.

d) Keep as much copper area as possible on all layers in the proximity of the device for best thermal performance. Especially, keep large copper areas connected to the large pads on the chip, and use thermal vias to transmit the heat to the bottom side of the board when possible.

e) All vias underneath the chip, whether thermal or not should be plugged with epoxy or some material other than solder. The amount of solder paste used for mounting is important to a good connection. Empty vias can siphon off solder during the mounting process and leave voids, while soldered vias may contribute solder and cause shorts below the chip.

f) Power and ground (PGND) busses should be distributed through power and ground planes. These should feed through vias to the appropriate pads for the 12 volts, switch node and ground connections. The impedances of the high current paths are critical for optimum efficiency.

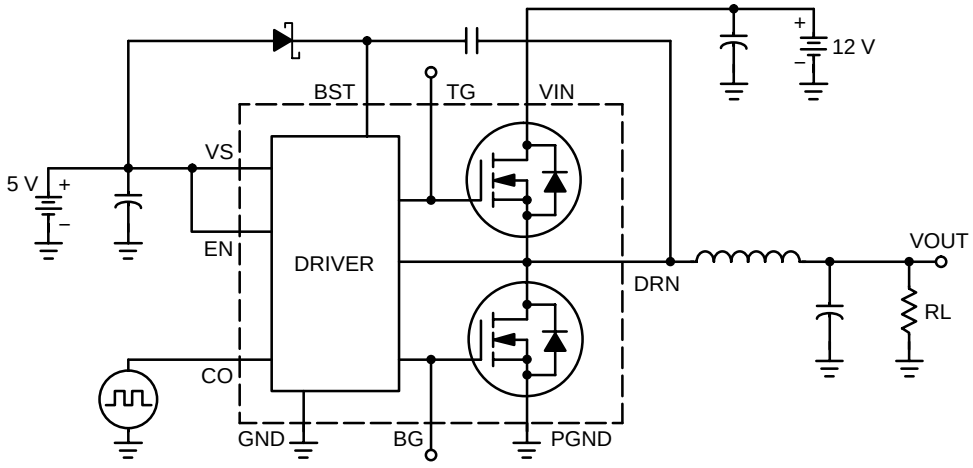


Figure 15.

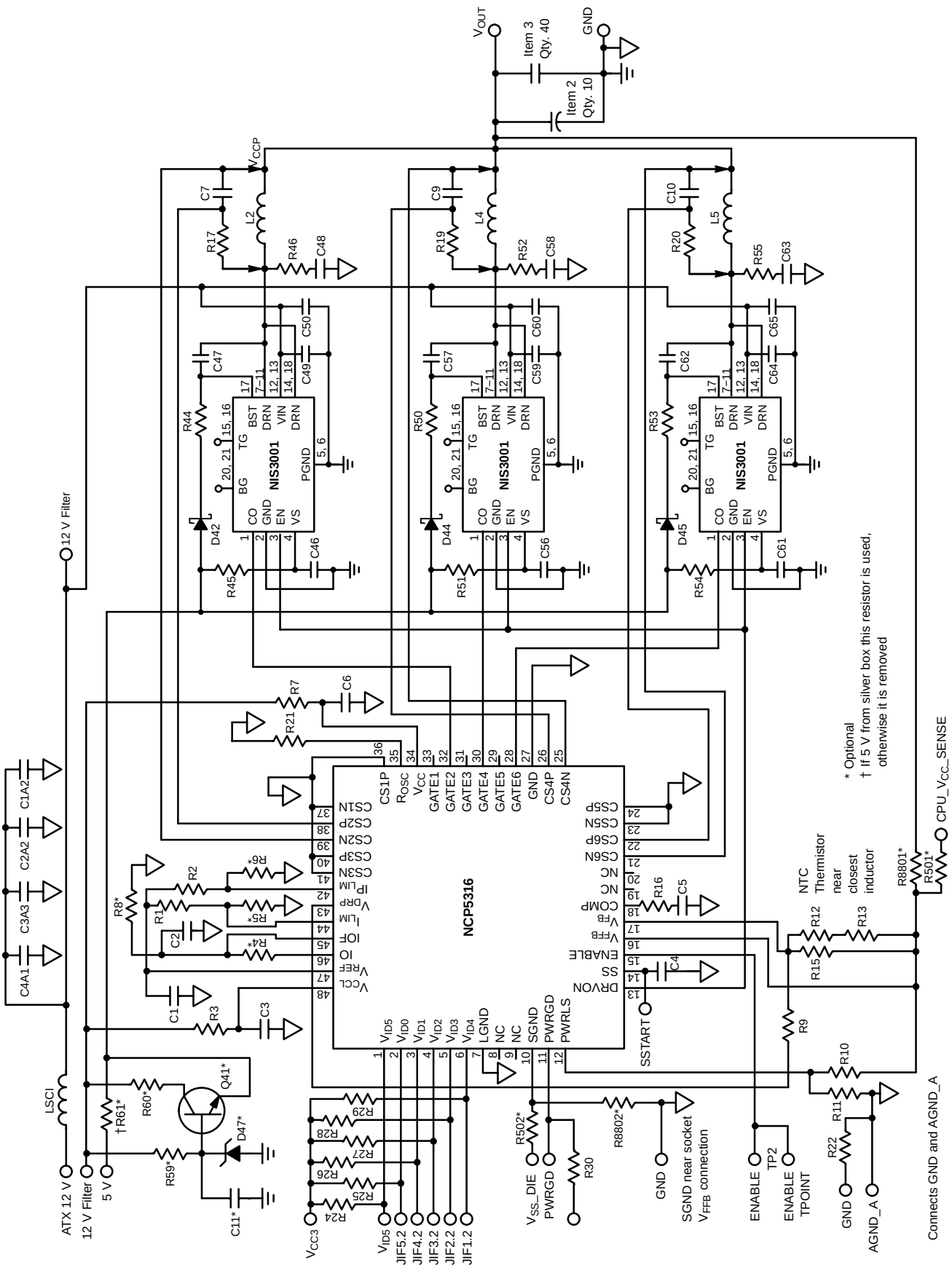


Figure 16. Application Diagram, Three−Phase Converter

3 Phase Voltage Regulator (VRD) Recommended Bill of Materials

Item	Quantity	Reference	Value	Size	Rating	Vendor	Part Number	Vendor	Part Number
1	10	C1,C2,C3,C4,C5,C6,C7, C9,C10	10nF	SM C0603	50V	muRata	GRM188R71H103KA01L	TDK	C1608X7R1H103K
2	10	C1B5,C1B6,C1B7,C2B12 C2B13,C2B14, C2B15,C3B9,C3B10, C3B11	560μF	Size E, 8 x 10.5mm 3.5mm, 0.60mm	4V	SANYO OS−CON SEPC Series	4SEPC560M(E13) ;+/−20% (M)		
3	40	C2D1,C2C1,C2D2,C2C2, C2D3,C2C3, C2D4,C2C4,C2D5,C2C5, C2D6,C2C6, C2D7,C2C7,C2D8,C2C8, C2D9,C2C9, C2D10,C2C10,C2D11, C2C11,C2D12, C2C12,C2C13,C2C14, C2C15,C2C16, C2C17,C2C18,C2C19, C2C20,C2C21, C2C22,C2C23,C2C24, C2C25,C2C26, C2C27,C2C28	10μF	SM 1206	6.3V	muRata	GRM31CR70J106KA01L	TDK	C3216X5R0J106M
4	6	C46,C47,C56,C57,C61, C62	1μF	SM C0805	16V	muRata	GRM21B71C105KA01L	TDK	C2012X7R1C105K
5	6	C49,C50,C59,C60,C64, C65	10μF	SM C1210	16V	muRata	GRM31CR61C106KC31L	TDK	C3225X7R1C106KT
6	3	C48,C58,C63	10nF	SMC0603	16V	muRata	GRM188R71H103KA01L	TDK	C1608X7R1H103K
7	4	C4A1,C3A3,C2A2,C1A2	1800μF	23X10 mm/5.5 mm	16V	Rubycon	16 MBZ 1800 M 10X23		
8	3	D42,D44,D45	Schottky	SOT−23	30V/ 0.2A	ON Semiconductor	BAT54LT1		
9	3	L2,L4,L5	280nH	18.0 x 8.12	30Adc	Coiltronics, Incorporated			
10	1	L5C1	275nH	10.16 x 8.12	16Adc	Coiltronics, Incorporated	CTX15−14771		
11	2	R2,R1	6.65K	R0805	“1%, 1/8 W”	VISHAY	CRCW08056651FRT1		
12	2	R3,R7	10 _	R0805	“10%, 1/8W”	VISHAY	CRCW0805100JT1		
13	1	R9	2.10K	R0805	“1 %, 1/8W”	VISHAY	CRCW08052101FRT1		
14	1	R10	15K	R0805	“10%, 1/8W”	VISHAY	CRCW0805153JT1		
15	1	R11	20 K	R0805	“10%, 1/8W”	VISHAY	CRCW0805203JT1		
16	1	R12	2.00 K	R0805	“10%, 1/8W”	VISHAY	CRCW0805202JT1		
17	1	R13	15K@ T=25°C	R0805	200mW	muRata NTC Thermistor	NCP21XW153J03RA	TDK	NTCG203NH153JT
18	1	R22	0_	R0805	“10%, 1/8W”	VISHAY	CRCW0805R00JT1		
19	1	R15	1K	R0805	“10%, 1/8 W”	VISHAY	CRCW0805102JT1		
20	2	R16,R61	0_	R0805	“10%, 1/8W”	VISHAY	CRCW0805R00JT1		
21	3	R17,R19,R20	18.2K	R0805	“1%, 1/8 W”	VISHAY	CRCW08051822FT1		
22	1	R21	63.4K	R0805	“1%, 1/8 W”	VISHAY	CRCW08056342FT1		
23	7	R24,R25,R26,R27,R28, R29,R30	1.5K	R0805	“10%, 1/8W”	VISHAY	CRCW0805152JT1		
24	6	R44,R45,R50,R51,R53, R54,	2.2_	R0805	“10%, 1/8W”	VISHAY	CRCW08052R2JT1		

R61 is used to connect the NIS3001 Vs pin to 5V supply only. If different voltage is required items 29 thru 33 are needed.

3 Phase Voltage Regulator (VRD) Recommended Bill of Materials

Item	Quantity	Reference	Value	Size	Rating	Vendor	Part Number	Vendor	Part Number
25	3	R46,R52,R55	2.2_	SMR0603	“10%, 1/10W”	VISHAY	CRCW06032R2JT1		
26	1	U1	4/5/6 Phase IC	LQFP−48 9 X 9 mm		ON Semiconductor	NCP5316		
27	1	PCB	4 layer 1 oz cCu ea	6.3 x 6.0 inches	FR4	CGI Circuits	ONS 7 Rev C		
28	3	U42, U44, U45	Inte-grated Module	10.5 X 10.5 mm	25 Arms	ON Semiconductor	NIS3001		
OPTIONAL PARTS									
29	1	C11	10nF	SM C0603	50V	muRata	GRM188R71H103KA01L		
30	1	R59	1K	R0805	“10%, 1/8W”	VISHAY	CRCW0805102JT1		
31	1	R60	2.2_	R0805	“10%, 1/8W”	VISHAY	CRCW08052R2JT1		
32	1	Q41	NPN Bipolar X−sistor	SOT−223	30V/ 3A	ON Semiconductor	MMJT9410T1		
33	1	D47	Zener Regulator	SOT−23	0.225W/ 6.8 V	ON Semiconductor	BZX84C6V8LT1		
34	2	R8801, R8802	N/A						
35	2	R501, R502	N/A						
36	4	R4, R5, R6, R8	N/A						

R61 is used to connect the NIS3001 Vs pin to 5V supply only. If different voltage is required items 29 thru 33 are needed.

APPLICATION INFORMATION

INTRODUCTION

Various ON Semiconductor components are packaged in an advanced Quad Flat−pack No−Lead Package (QFN) or commonly referred to as a Leadless Package. Because the QFN(Leadless) platform represent the latest in surface mount packaging technology, it is important that the design of the Printed Circuit Board (PCB), as well as the assembly process, follow the suggested guidelines outlined in this document.

NIS3001 Package Overview

The QFN platform offers a versatility, which allows either a single or multiple semiconductor devices to be connected together within a leadless package.

In this case the NIS3001 Package contains multiple semiconductor devices within one package. This package style was chosen due to its excellent thermal dissipation and reduced electrical parasitics.

When surface mounting this package onto a PCB, two critical issues must be considered:

1. Printed Circuit Board Design
2. Board Mounting Process.

This document will address both of these critical issues.

Printed Circuit Board Design Considerations

SMD and NSMD pad configurations

There are two different types of PCB pad configurations commonly used for surface mount leadless QFN style packages. These different I/O configurations are:

1. Non Solder masked Defined (NSMD)
2. Solder Masked Defined (SMD)

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 17. With the SMD Pads, the solder mask restricts the flow of solder paste on the top of the metallization which prevents the solder from flowing along the side of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

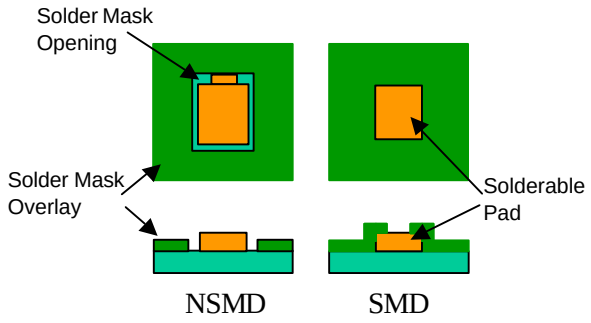


Figure 17. Comparison of NSMD versus SMD pads.

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is eliminated when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

NSMD Pad Configurations

When dimensionally possible, the solder mask should be located at least a ±0.076mm (0.003in) away from the edge of the solderable pad. This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad. The dimensions of the soldermask openings are shown in Figure 18 for a preferred non−soldermask configuration.

The dimensions of the PCB's solderable pads should match those of the pads on the package as shown in Figure 19. The 1:1 ratio between the package's pad configuration, and that of the PCB's, is desired for optimal placement accuracy and reliability. Please note that NIS3001 Footprint shows smaller exposed pad openings compared with the recommended PCB layout. Die attach pads on the footprint were divided into smaller exposed pads to help reduce the risk of solder voiding during reflow mounting to the package

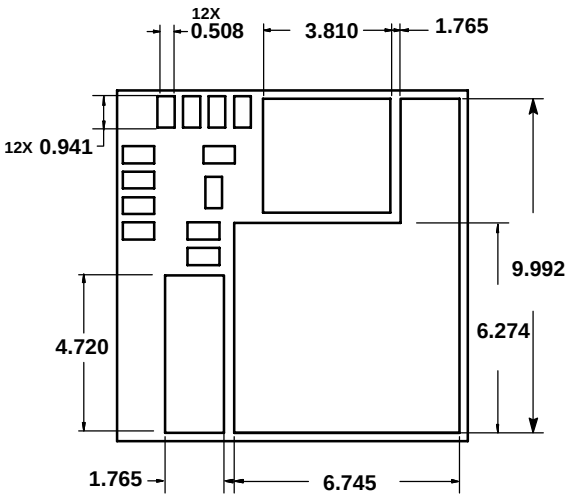


Figure 18. NSMD Openings for PCB Layout

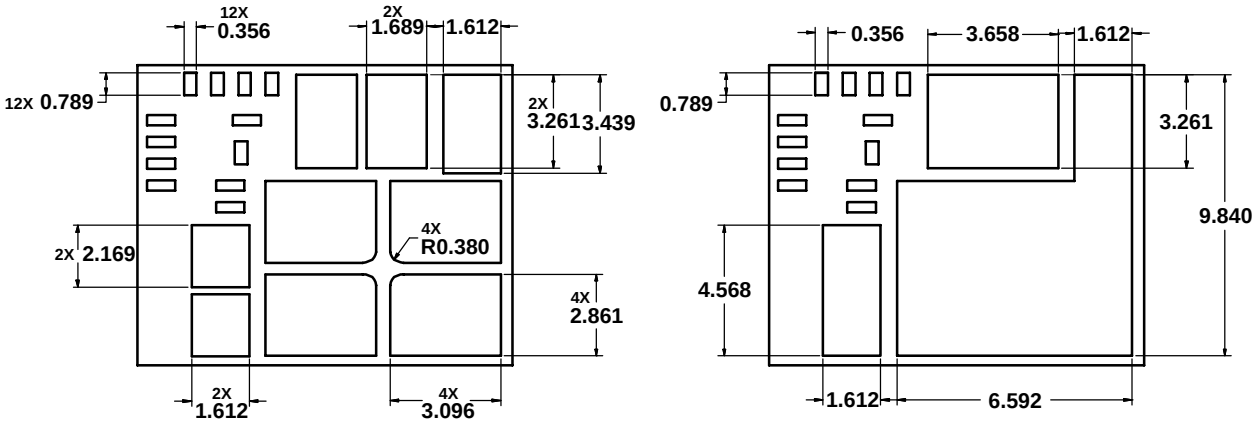


Figure 19. Recommended PCB Layout for NIS3001 footprint

Thermal/Electrical Vias

Vias are normally placed on the larger die attach pads to improve electrical and thermal performance. If vias are required on the larger die attach pads, our recommendation is to use filled−vias. Filled−vias will help prevent the solder from flowing down into the holes, thereby reducing the solder volume required for the solder joint of this die attach pad. Filled−vias are normally filled with some type of conductive epoxy.

If through−hole vias are used, we recommend that the via size be less than or equal to 0.25mm(10 mils). The number of vias placed over the die attach pad is also critical and should not exceed 25% of the total exposed area of the copper pattern. In other words, excessive through−hole vias will allow the solder to flow down into the via and thereby decrease the solder volume needed to have a sufficient solder joint. These vias can be plugged with solder mask material to avoid soldering wicking.

NIS3001 Board Mounting Process

The board mounting process is optimized by first defining and controlling the following processes:

1. Creating and maintaining a solderable metallization on the PCB contacts.
2. Choosing the proper solder paste.
3. Screening/stenciling the solder paste onto the PCB.
4. Placing the package onto the PCB.
5. Reflowing the solder paste.
6. Final solder joint inspection.

Recommendations for each of these processes are located below.

PCB Solderable metallization

There are two common plated solderable metallizations, which are used for PCB surface mount devices. In either case, it is imperative that the plating is uniform, conforming, and free of impurities to insure a consistent solderable system.

The first metallization consists of an Organic Solderability Preservative coating (OSP) over the copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering.

The second recommended solderable metallization consists of plated electroless nickel over the copper pad, followed by immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be at least 0.05 mm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment which may affect the reliability of the joint.

Solder Type

Solder paste such as Cookson Electronics' WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water−soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no−clean flux is preferred.

Solder Screening onto the PCB

Stencil screening the solder onto the PCB board is commonly used in the industry. The recommended stencil thickness to be used is 0.075 mm (0.003 in) and the sidewalls of the stencil openings should be tapered approximately 5 degrees to facilitate the release of the paste when the stencil is removed from the PCB. Note that a 0.127 mm (0.005 in) thick stencil may be used also, but will require smaller stencil openings to reduce the amount of solder applied to equal the amount of solder applied using the 0.075 mm thick stencil.

For a typical edge PCB terminal pad, the stencil opening should be the same size as the pad size on the package. However, in cases where the die pad is soldered to the PCB, the stencil opening must be divided into smaller openings

as shown in Figure 20. Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ±0.05 mm or better is recommended. The package will tend to center itself and correct for slight placement errors during the reflow process due to the surface tension of the solder.

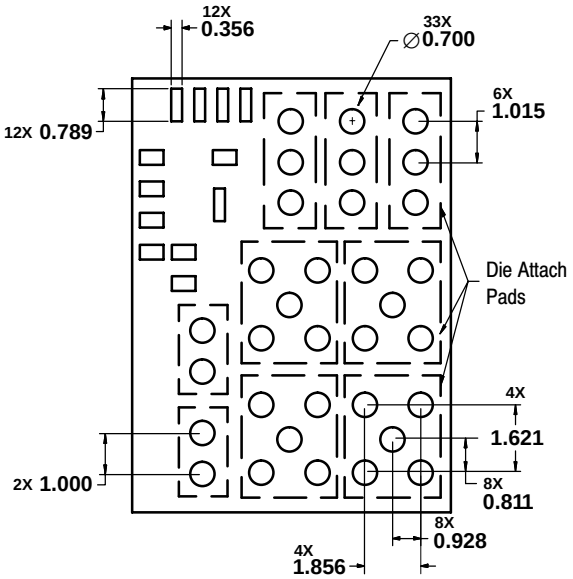


Figure 20. Solder stencil design illustrating smaller stencil openings over the larger exposed die pads.

Solder Reflow

Once the package is placed on the PC board along with the solder paste, a standard surface mount reflow process can be used to mount the part. Figure 21 is an example of a standard reflow profile. The exact profile will be determined, and is available, by the manufacture of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

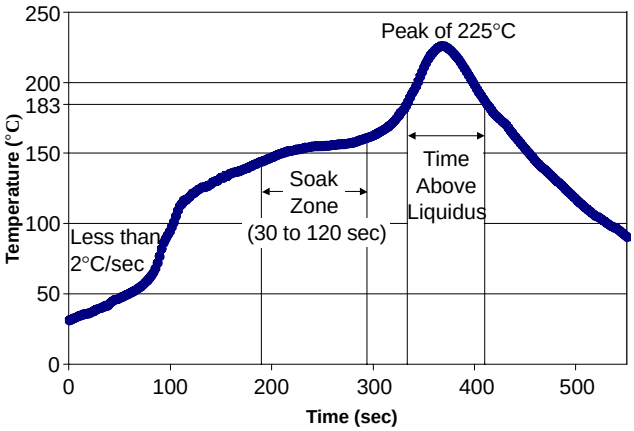


Figure 21. Typical reflow profile for eutectic tin/lead solder.

In general, the temperature of the part should be raised not more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 30 to 120 seconds. Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 30 to 100 seconds depending on the mass of the board. The peak temperature of the profile should be between 205 and 225°C for eutectic Sn/Pb solder.

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of an X−ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X−ray inspection system. The solder joints should have enough solder volume with the proper stand−off height so that an “Hour Glass” shaped connection is not formed as shown below in Figure 22. “Hour Glass” solder joints are a reliability concern and must be avoided.

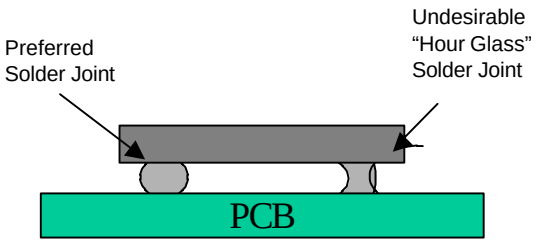


Figure 22. Side view of NIS3001 illustrating preferred and undesirable solder joints.

Rework Procedure

Due to the fact that the NIS3001 is a leadless device, the entire package must be removed from the PC board if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommend that the PC board be placed in an oven at 125°C for 4 to 8 hours prior to heating the parts to remove excess moisture from the packages. In order to control the region, which will be exposed to reflow temperatures, the board should be heated to a 100°C by conduction through the backside of the board in the location of the NIS3001 QFN Package. Typically, heating nozzles are then used to increase the temperature locally.

Once the NIS3001's solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PC board are cleaned. The cleaning of the pads is typically performed with a blade−style conductive tool with a de−soldering braid. A no clean flux is used during this process in order to simplify the procedure.

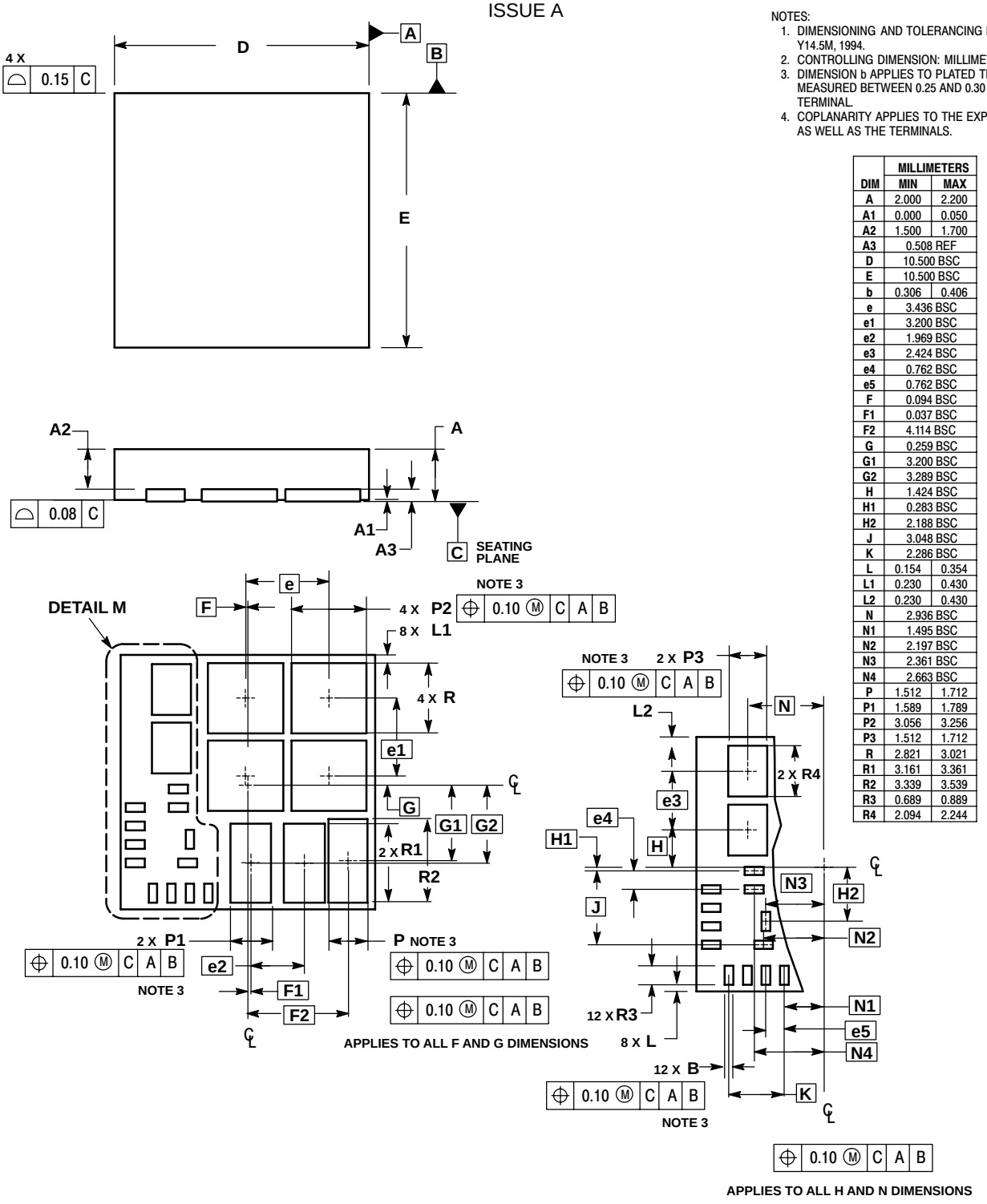
Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PC board configurations, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini−stencil for redressing the pad.

Due to the small pad configurations of the NIS3001, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the NIS3001 Package with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the packages will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second is either a concern or unacceptable for a specific application, than the localized reflow option would be the recommended procedure.

PACKAGE DIMENSIONS

PInPAK
10.5x10.5 QFN
CASE 500−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.200
A1	0.000	0.050
A2	1.500	1.700
A3	0.508 REF	
D	10.500 BSC	
E	10.500 BSC	
b	0.306	0.406
e	3.436 BSC	
e1	3.200 BSC	
e2	1.969 BSC	
e3	2.424 BSC	
e4	0.762 BSC	
e5	0.762 BSC	
F	0.094 BSC	
F1	0.037 BSC	
F2	4.114 BSC	
G	0.259 BSC	
G1	3.200 BSC	
G2	3.289 BSC	
H	1.424 BSC	
H1	0.283 BSC	
H2	2.188 BSC	
J	3.048 BSC	
K	2.286 BSC	
L	0.154	0.354
L1	0.230	0.430
L2	0.230	0.430
N	2.936 BSC	
N1	1.495 BSC	
N2	2.197 BSC	
N3	2.361 BSC	
N4	2.663 BSC	
P	1.512	1.712
P1	1.589	1.789
P2	3.056	3.256
P3	1.512	1.712
R	2.821	3.021
R1	3.161	3.361
R2	3.339	3.539
R3	0.689	0.889
R4	2.094	2.244

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