4 Megabit (512K x 8) SuperFlash MTP
SST27VF040

Preliminary Specifications

FEATURES:

- **2.7 to 3.6 Volt Read Operation**
- **Superior Reliability**
  - Endurance: Greater than 1000 Cycles
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Access Time**
  - 90 and 120 ns
- **Fast Programming Operation**
  - 10 µs Programming Pulse
  - Chip Programming Time of 7 seconds
- **Features Electrical Erase**
  - Does Not Require UV Source
  - Chip Erase Time: 100 ms
- **CMOS I/O Compatibility**
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **12V Power Supply for Programming/Erase**
- **Packages Available**
  - 32-Pin PLCC
  - 32-Pin Plastic DIP
  - 32-Pin TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST27VF040 is a 512K x 8 CMOS, many-time programmable (MTP) low cost flash, manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST27VF040 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The SST27VF040 has to be erased prior to programming. The SST27VF040 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance byte programming, the SST27VF040 uses a programming pulse of 10 µs. The entire memory can be programmed byte by byte in 7 seconds. Designed, manufactured, and tested for a wide spectrum of applications, the SST27VF040 is offered with a endurance of 1000 cycles. Data retention is rated at greater than 100 years.

The SST27VF040 is suited for applications that require infrequent writes and low power nonvolatile storage. The SST27VF040 will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST27VF040 is offered in 32-pin PLCC, 32-pin PDIP and 32-pin TSOP packages. See Figures 1 and 2 for pinouts.

Device Operation

The SST27VF040 is a low cost flash solution that can be used to replace existing UV-EPROM, OTP and mask ROM sockets. It is functionally (Read and Program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, the device also supports electrical erase operation via an external programmer. The SST27VF040 does not require a UV source to erase, and therefore the packages do not have windows.

Read

The Read operation of the SST27VF040 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of T_{OE} from the falling edge of OE#, assuming the CE# pin has been low and the addresses have been stable for at least T_{CE} - T_{OE}. When the CE# pin is high, the chip is deselected and a standby current of only 10 µA (typical) is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.

Programming operation

The SST27VF040 is programmed by using an external programmer. The programming mode is activated by asserting 12V (±5%) on V_{PP} pin and V_{IL} on CE#, pin. The device is programmed using a single pulse (CE# pin low) of 10 µs per byte. Using the MTP programming algorithm, the byte programming process continues byte by byte until the entire chip (512 KBytes) has been programmed.

Chip Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". Unlike traditional EPROMs, which use UV light to the chip erase, the SST27VF040 uses an electrical Chip Erase operation. This saves a significant amount of time (about 30 minutes for each Erase operation). The entire chip can be erased in 100 ms (CE# pin low). In order to activate erase mode, the 12V (±5%) is applied to V_{PP} and A_9 pins and V_{IH} on OE# pin. All other address and data pins are don't care. The falling edge of CE# will start the chip erase operation. Once the chip has been erased, all bytes must be verified for FF. Refer to Figure 8 for the flow chart.

The SST27VF040 can also be reprogrammed in the system. This requires the availability of 12V on V_{PP} to program and 12V on address pin A_9 to erase.

Product Identification Mode

The product identification mode identifies the device as the SST27VF040 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V_H (12V±5%) on address A_9 with $V_{PP} = V_{DD} = 2.7\text{-}3.6V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0. For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Byte	Data
Manufacturer's Code	0000 H	BF H
Device Code	0001 H	C7 H

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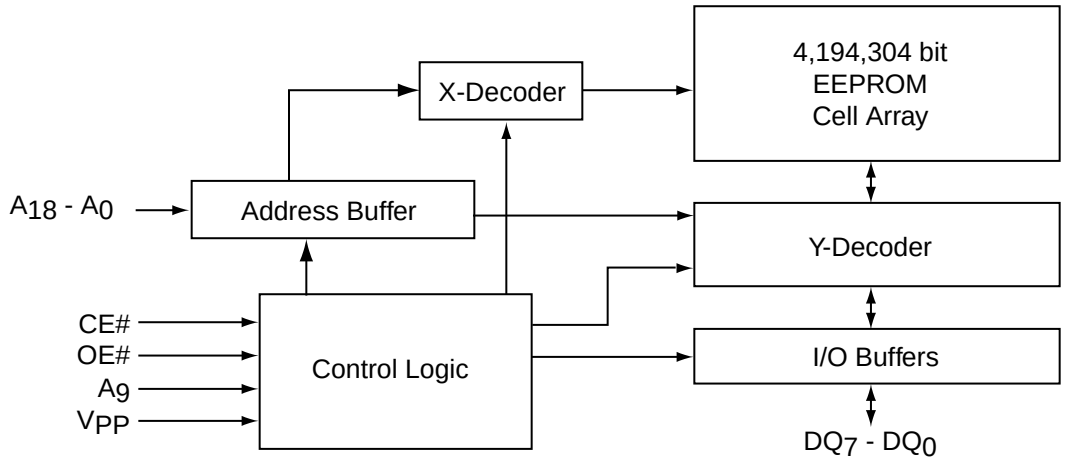
Design Consideration

The SST27VF040 should have a 0.1µF ceramic high frequency low inductance capacitor connected between V_{DD} and GND, as well as V_{PP} and GND. These capacitors should be placed as close as possible to the package terminals.

FUNCTIONAL BLOCK DIAGRAM OF THE SST27VF040



324 ILL B1.3

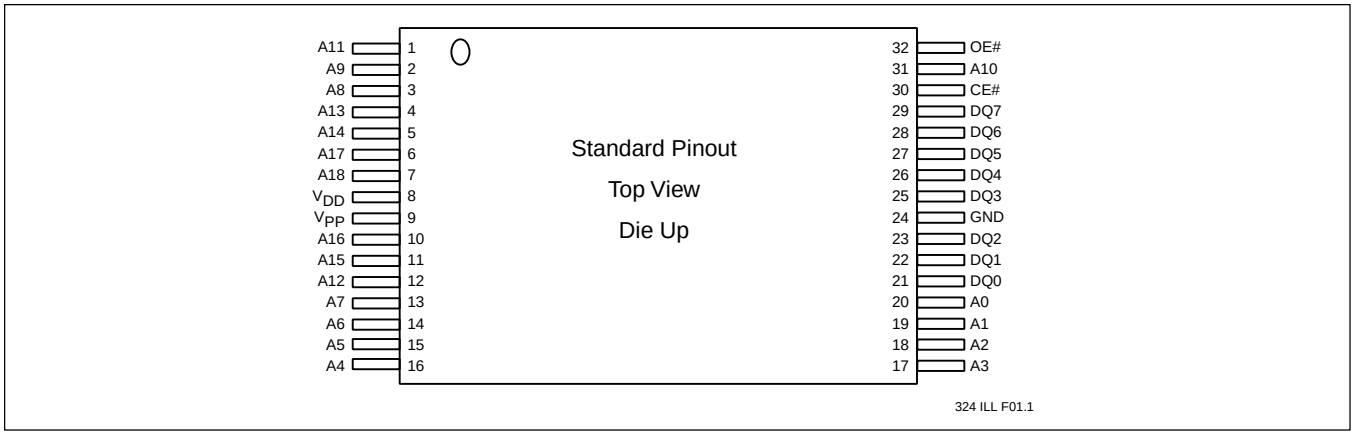


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGES

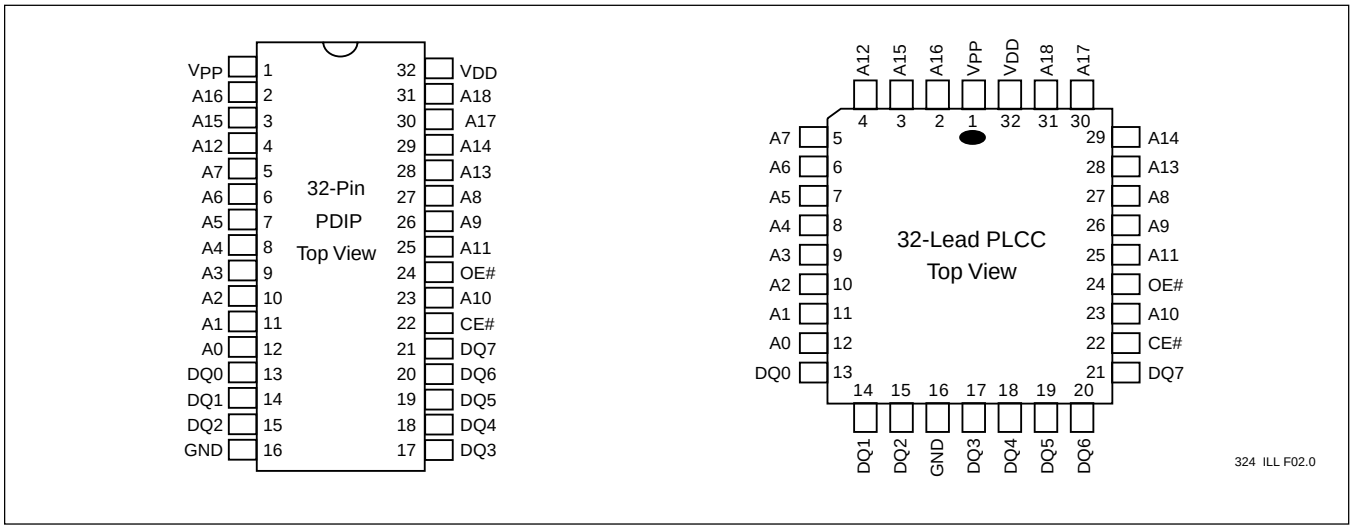


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLASTIC DIPS AND 32-LEAD PLCCS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{18}-A_0	Address Inputs	To provide memory addresses
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during program cycle, the outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low
OE#	Output Enable	To gate the data output buffers during read operation
V_{PP}	Power Supply for Program or Erase	High voltage pin during chip erase and programming operation 12-volt (±5%)
V_{DD}	Power Supply	To provide 3-volt supply (2.7 to 3.6V)
GND	Ground	

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	A_9	V_{PP}	DQ	Address
Read	V_{IL}	V_{IL}	A_{IN}	V_{DD} or GND	D_{OUT}	A_{IN}
Output Disable	X	V_{IH}	X	V_{DD} or GND	High Z	A_{IN}
Standby	V_{IH}	X	X	V_{DD} or GND	High Z	X
Chip Erase	V_{IL}	V_{IH}	V_H	V_{PPH}	High Z	X
Program	V_{IL}	V_{IH}	A_{IN}	V_{PPH}	D_{IN}	A_{IN}
Program/Erase Inhibit	V_{IH}	X	X	V_{PPH}	High Z	X
Product Identification	V_{IL}	V_{IL}	V_H	V_{DD} or GND	Manufacturer Code (BF) Device Code (C7)	A_{18}-A_1 = V_{IL}, A_0 = V_{IL} A_{18}-A_1 = V_{IL}, A_0 = V_{IH}

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Note: X = V_{IL} or V_{IH}
V_H = 12V±5%
V_{PPH} = 12V±5%

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{DD}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{DD}+ 1.0V
Voltage on A_9, and V_{PP} Pin to Ground Potential ..... -0.5V to 13.2V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current(1) ..... 50 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7 to 3.6V
Industrial	-40°C to +85°C	2.7 to 3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... C_L = 100 pF
See Figures 6 and 7

TABLE 4: READ MODE DC OPERATING CHARACTERISTICS
V_{DD} = 2.7 to 3.6V, T_A = 0°C to 70°C (Commercial) or -40°C to +85°C (Industrial)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	V_{DD} Read Current		12	mA	CE# = OE# = V_{IL}, all I/Os open, Address Input = V_{IL}/V_{IH}, at f = $1/T_{RC}$ Min, V_{DD} = V_{DD} Max
I_{PPR}	V_{PP} Read Current		100	µA	CE# = OE# = V_{IL}, all I/Os open, Address Input = V_{IL}/V_{IH}, at f = $1/T_{RC}$ Min, V_{DD} = V_{DD} Max, V_{PP} = V_{DD}
I_{SB}	Standby V_{DD} Current		15	µA	CE# = V_{IHC} V_{DD} = V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Max
V_{IH}	Input High Voltage	2.0	V_{DD}+0.5	V	V_{DD} = V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100µA, V_{DD} = V_{DD} Min
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, A_9 = V_H Max.

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TABLE 5: PROGRAM/ERASE DC OPERATING CHARACTERISTICS
V_{DD} = 2.7 to 3.6V, V_{PP} = V_{PPH}, T_A = 25°C ± 5°C

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CP}	V_{DD} Erase or Program Current		30	mA	CE# = V_{IL}, V_{PP} = 12V±5%, V_{DD} = V_{DD} Max
I_{PP}	V_{PP} Erase or Program Current		1	mA	CE# = V_{IL}, V_{PP} = 12V±5%, V_{DD} = V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_H	Supervoltage for A_9	11.4	12.6	V	CE# = OE# = V_{IL}
I_H	Supervoltage Current for A_9		200	µA	CE# = OE# = V_{IL}, A_9 = V_H Max
V_{PPH}	High Voltage for V_{PP} Pin	11.4	12.6	V	

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$	Power-up to Read Operation	100	µs
$P_{PU-WRITE}$	Power-up to Write Operation	100	µs

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TABLE 7: CAPACITANCE (T_A = 25 °C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1000	Cycles	MIL-STD-883, Method 1033
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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Note: [1] This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS

V_{DD} = 2.7 to 3.6V, T_A = 0°C to 70°C (Commercial) or -40°C to +85°C (Industrial)

		SST27VF040-90		SST27VF040-120		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read Cycle Time	90		120		ns
T_{CE}	Chip Enable Access Time		90		120	ns
T_{AA}	Address Access Time		90		120	ns
T_{OE}	Output Enable Access Time		45		55	ns
T_{CLZ}	CE# Low to Active Output	0		0		ns
T_{OLZ}	OE# Low to Active Output	0		0		ns
T_{CHZ}	CE# High to High-Z Output		30		30	ns
T_{OHZ}	OE# High to High-Z Output		30		30	ns
T_{OH}	Output Hold from Address Change	0		0		ns

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TABLE 10: PROGRAMMING/ERASE CYCLE TIMING PARAMETERS

V_{DD} = 2.7 to 3.6V, V_{PP} = 12V ± 5%, T_A = 25°C ± 5°C

Symbol	**Parameter**	**Min**	**Max**	**Units**
T_{PC}	Program Cycle Time	12		µs
T_{AS}	Address Setup Time	1		µs
T_{AH}	Address Hold Time	1		µs
T_{DS}	Data Setup Time	1		µs
T_{DH}	Data Hold Time	1		µs
T_{PRT}	V_{PP} Pulse Rise Time	1		µs
T_{VPS}	V_{PP} Setup Time	1		µs
T_{VPH}	V_{PP} Hold Time	1		µs
T_{PWP}	CE# Program Pulse Width	10	15	µs
T_{PWE}	CE# Erase Pulse Width	100	500	ms
T_{VR}	A_9 Recovery Time for Erase	1		µs
T_{ART}	A_9 Rise Time to 12V during Erase	1		µs
T_{A9S}	A_9 Setup Time during Erase	1		µs
T_{A9H}	A_9 Hold Time during Erase	1		µs

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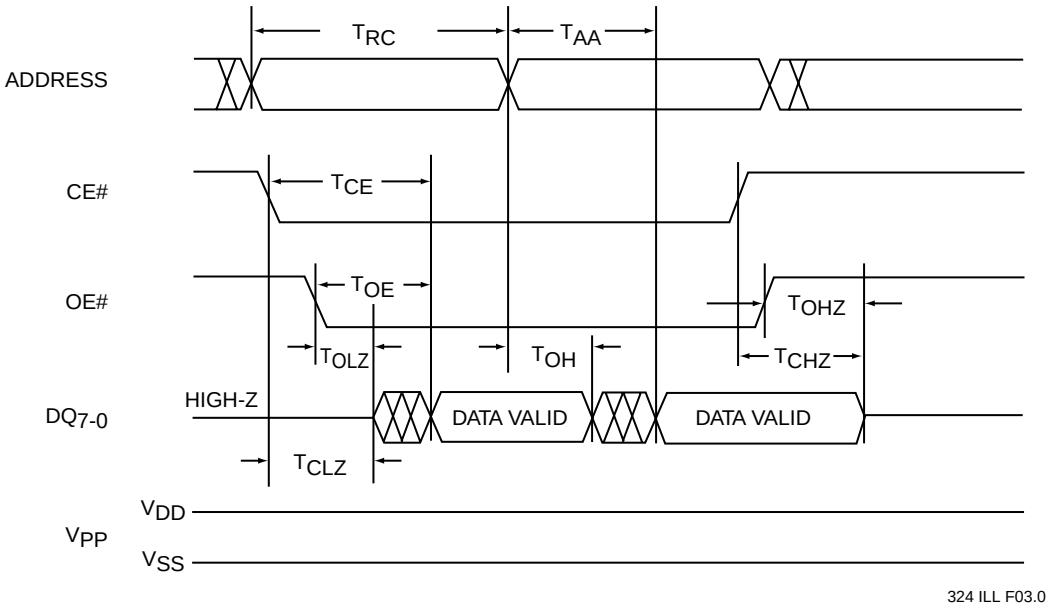


FIGURE 3: READ CYCLE TIMING DIAGRAM

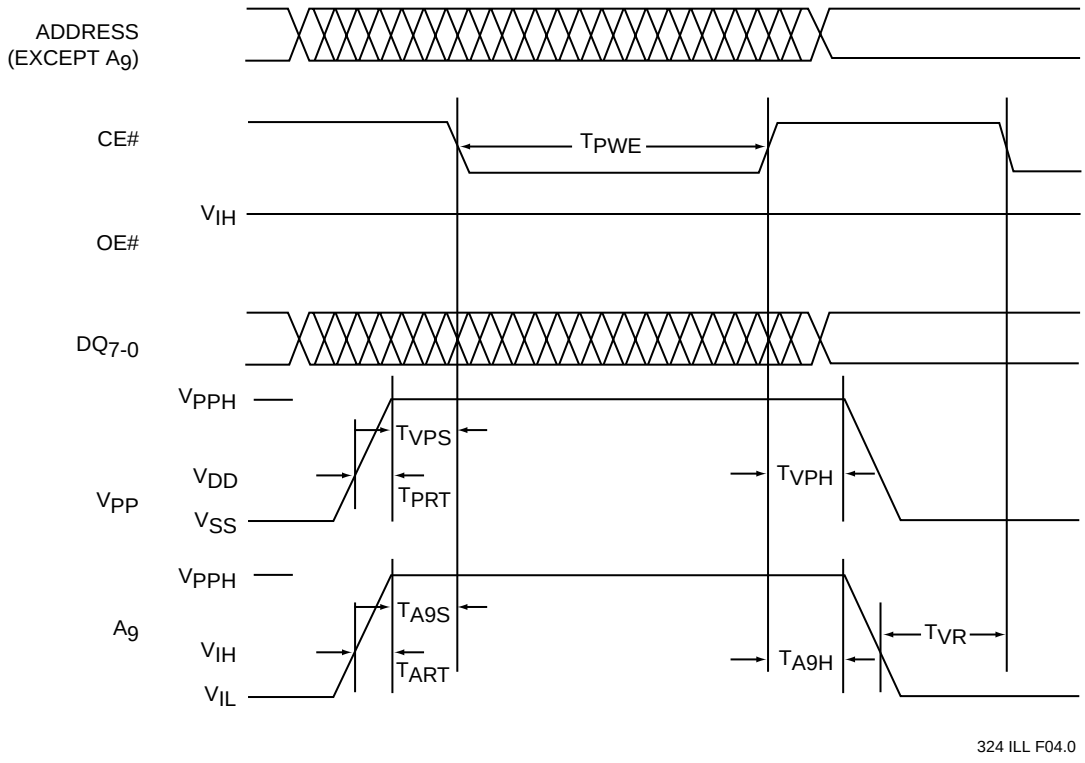


FIGURE 4: ERASE TIMING DIAGRAM

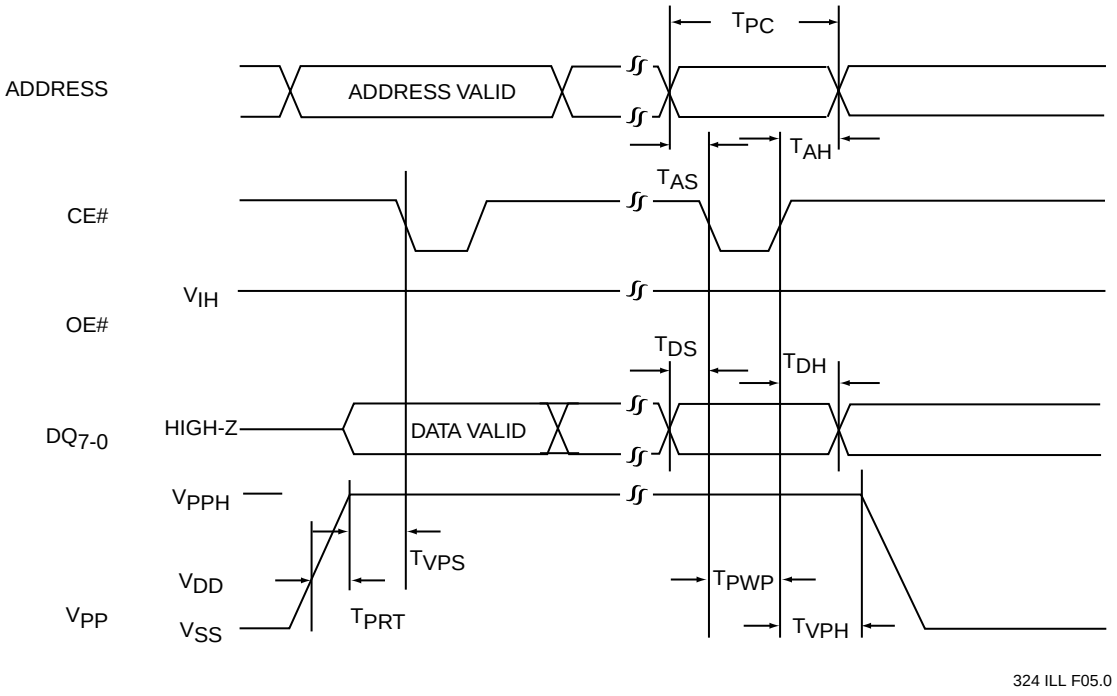
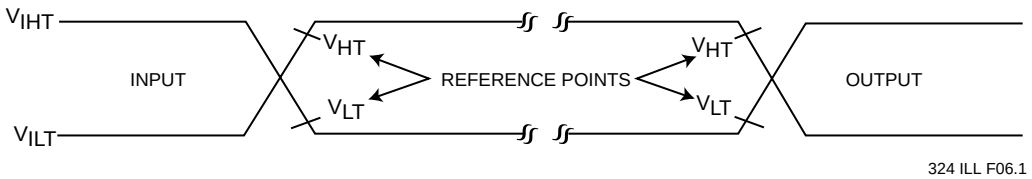


FIGURE 5: PROGRAM TIMING DIAGRAM



AC test inputs are driven at V_{IHT} (V_{DD}*0.9) for a logic "1" and V_{ILT} (V_{DD}*0.1) for a logic "0".
Measurement reference points for inputs and outputs are at V_{HT} (V_{DD}*0.7) and V_{LT} (V_{DD}*0.3)
Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT}–V_{HIGH} Test
V_{LT}–V_{LOW} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 6: AC INPUT/OUTPUT REFERENCE WAVEFORMS

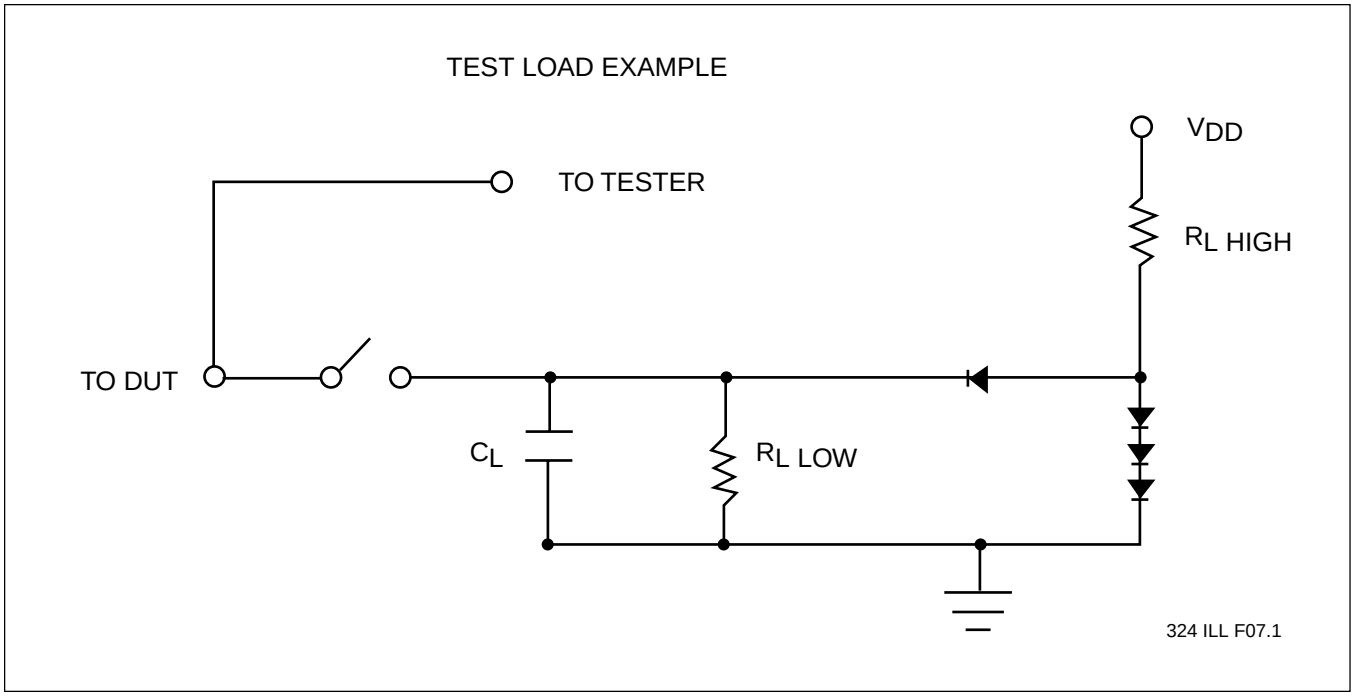


FIGURE 7: A TEST LOAD EXAMPLE

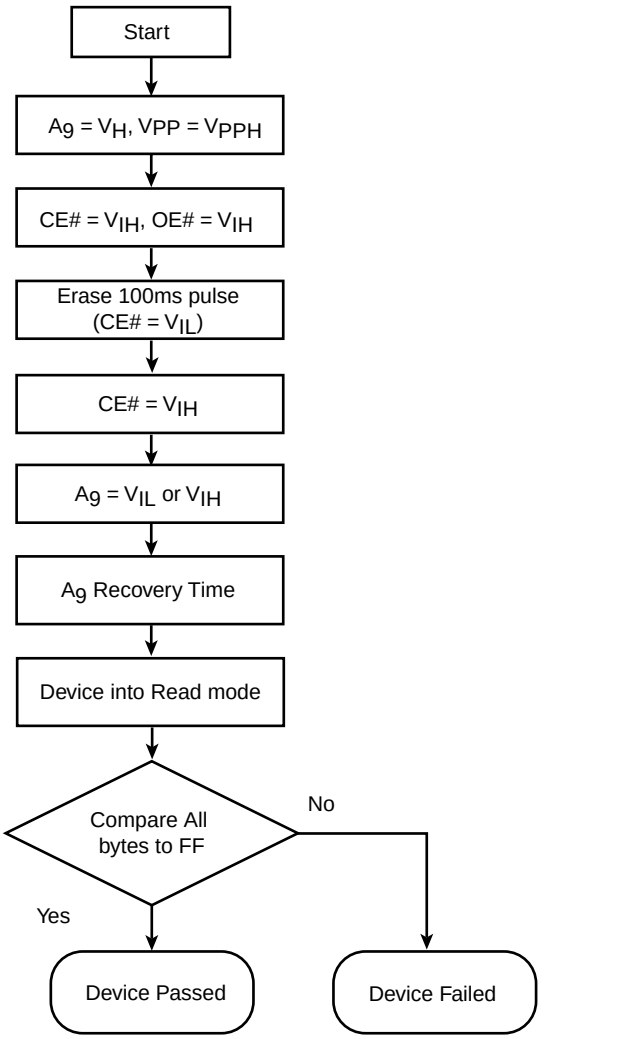


FIGURE 8: ERASE ALGORITHM

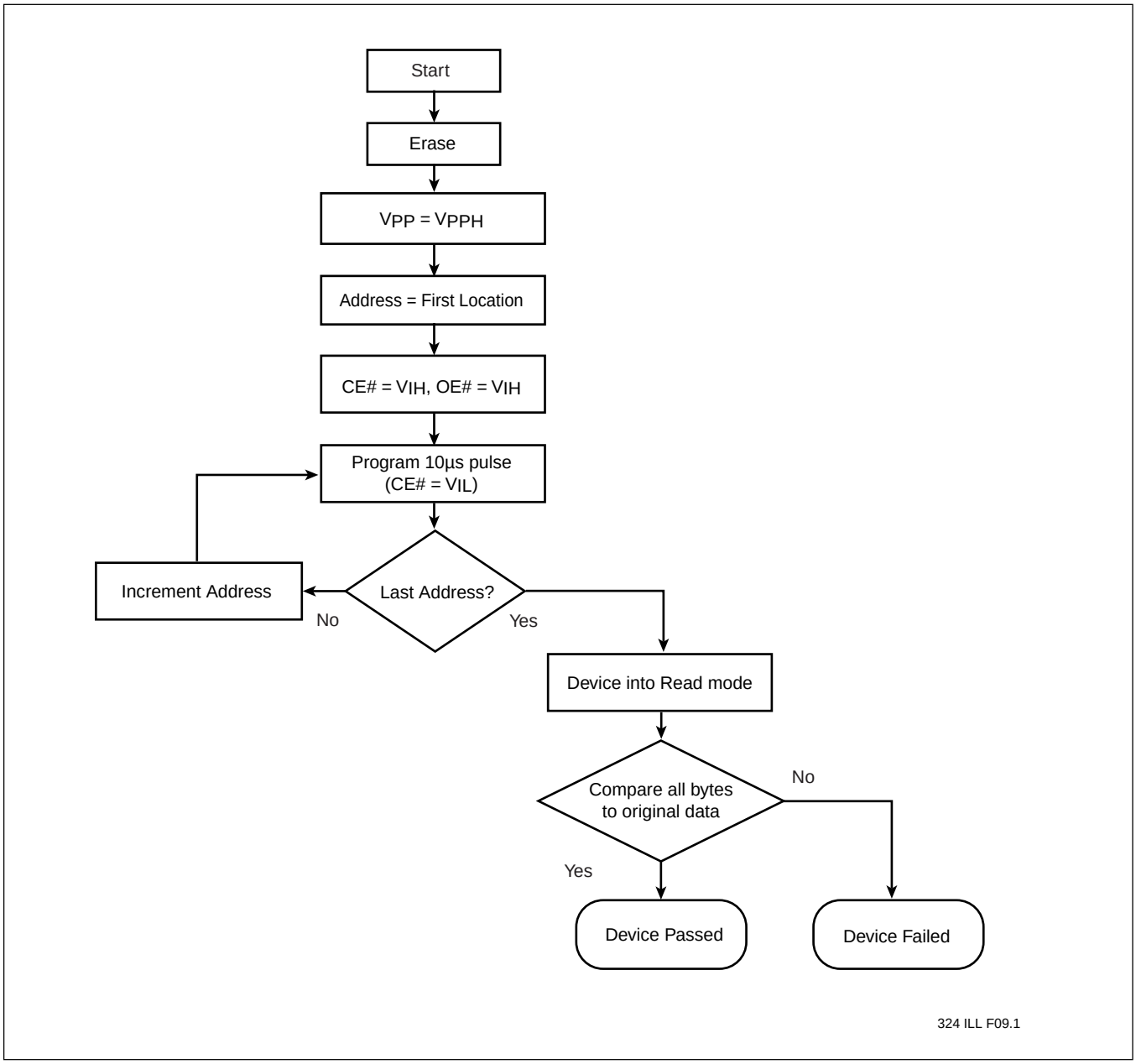
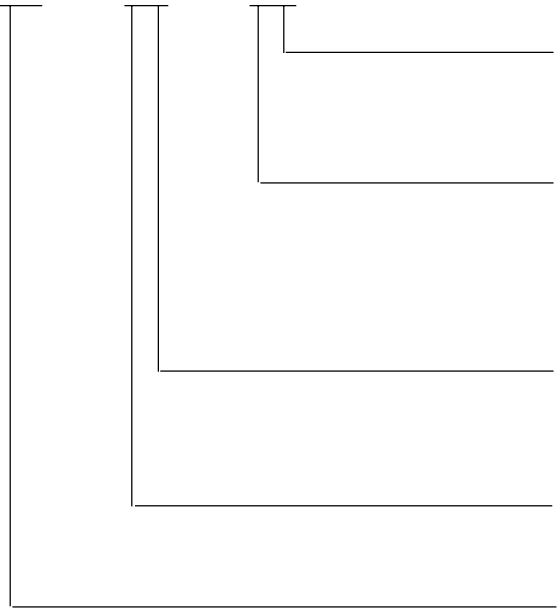


FIGURE 9: PROGRAMMING ALGORITHM

PRODUCT ORDERING INFORMATION

Device	Speed	Suffix1	Suffix2
SST27VF040 -	XXX -	XX -	XX



Package Modifier
H = 32 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
W = TSOP 8x14 mm
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles

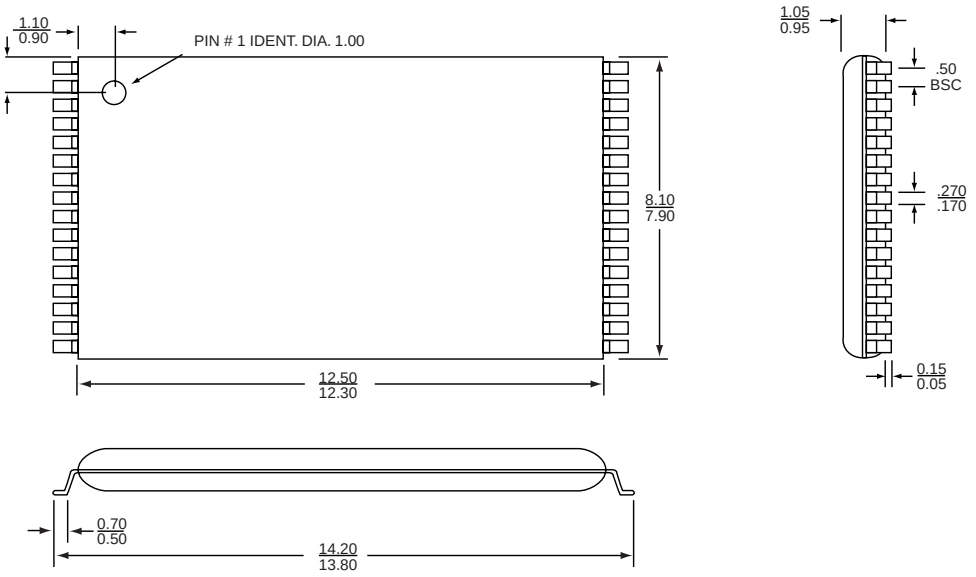
Read Access Speed
90 = 90 ns
120 = 120 ns

Valid combinations

SST27VF040-90-3C-WH	SST27VF040-90-3C-NH	SST27VF040-90-3C-PH
SST27VF040-90-3I-WH	SST27VF040-90-3I-NH	
SST27VF040-120-3C-WH	SST27VF040-120-3C-NH	SST27VF040-120-3C-PH
SST27VF040-120-3I-WH	SST27VF040-120-3I-NH	

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

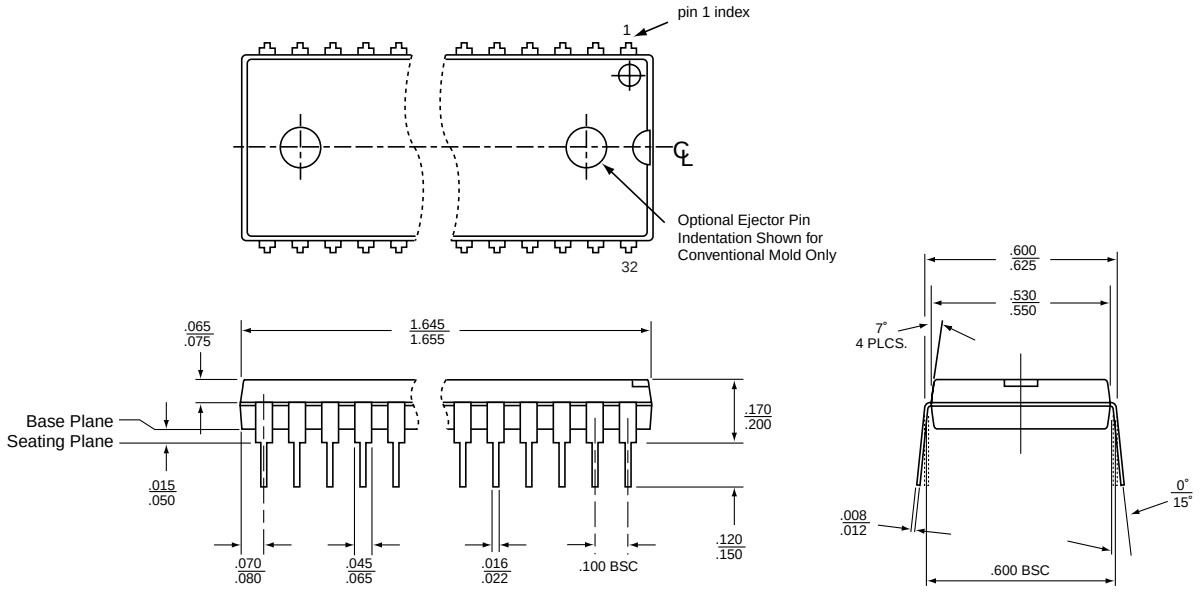
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32.TSOP-WH-ILL.0

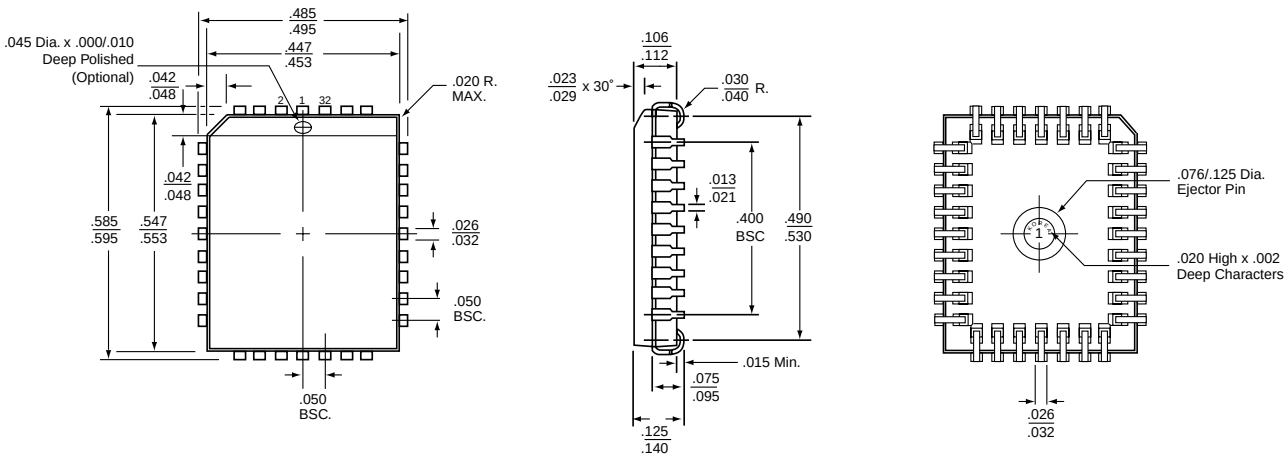
32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: WH



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32.pdipPH-ILL.0

32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32.PLCC.NH-ILL.0

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH