Micro Linear

T-52-33-11

ML4401, ML4411

Servo Demodulator

GENERAL DESCRIPTION

The ML4401 provides all of the analog circuitry necessary for the demodulation of di-bit servo signal information in Winchester disk drives. It interfaces to the servo head preamp and provides quadrature position signal outputs for the servo controller circuitry.

The ML4401 includes a high-performance 592-type input amplifier and differential AGC circuit. External logic is designed to meet the needs of the particular servo system utilizing the VCO and Charge Pump to create a PLL time base for Peak Detector gating. The SYNC output provides servo channel timing information for the logic.

The ML4401 has an ECL type output for the VCO, whereas the ML4411's VCO output is TTL.

The ML4401, ML4411, when combined with the ML4402, ML4406/07/08 Servo Driver, the ML4403, ML4413 Servo Controller and the ML4404, ML4414, ML4424 Trajectory Generator, provides a flexible closed-loop servo control system.

FEATURES

- Combines all analog di-bit demodulation circuitry
- Logic track-type switching can be used to minimize demodulator offset
- Exponential AGC characteristics makes AGC settling independent of input step size
- External loop compensation of analog blocks
- External digital circuitry allows flexible pattern format
- On-chip band gap voltage reference eliminates external referencing
- Operates from 12 V power supply
- Compatible with Micro Linear's ML4403, ML4413 Servo Controller, ML4402, ML4406/07/08 Servo Driver and ML4404, ML4414, ML4424 Trajectory Generator

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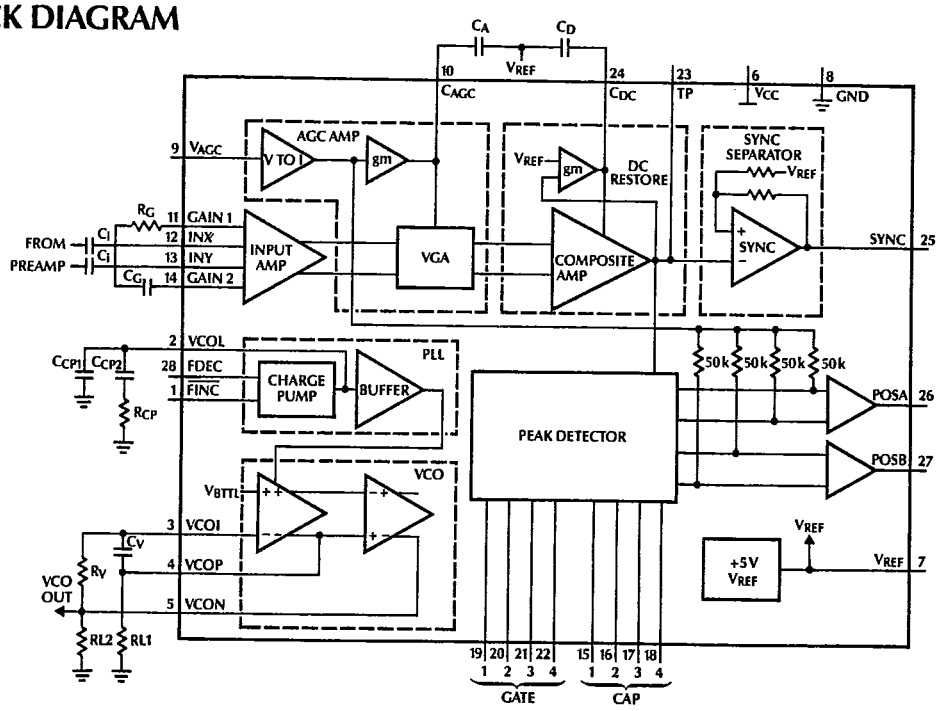
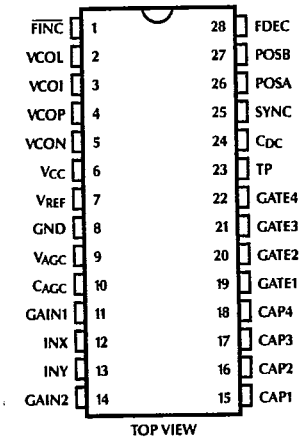
BLOCK DIAGRAM



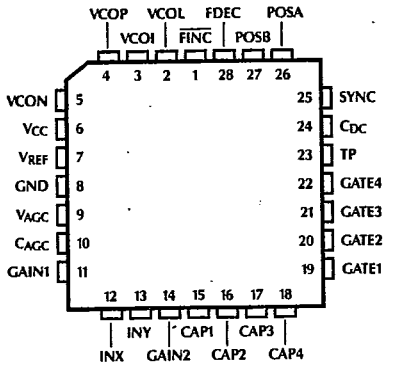
PIN CONNECTIONS

ML4401 28-Pin DIP



TOP VIEW

ML4401 28-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN #	NAME	FUNCTION
1	$\overline{\text{FINC}}$	Charge pump frequency increment input (TTL).
2	VCOL	PLL loop compensation terminal.
3	VCOI	VCO high impedance input.
4	VCOP	VCO positive output, for capacitive feedback to VCOI.
5	VCON	VCO negative output, drives resistance feedback to VCOI, also provides ECL output on ML4401 and TTL output on ML4411.
6	V_{CC}	+12V supply.
7	V_{REF}	Voltage reference output (+5V).
8	GND	Ground.
9	V_{AGC}	AGC gain reference voltage input.
10	C_{AGC}	External capacitor terminal to set AGC response.
11	GAIN1	Input amplifier gain adjusting RC terminal 1.
12	INX	X input into input amplifier.
13	INY	Y input into input amplifier.
14	GAIN2	Input amplifier gain adjusting RC terminal 2.
15	CAP1	Peak detector 1 capacitor terminal.
16	CAP2	Peak detector 2 capacitor terminal.
17	CAP3	Peak detector 3 capacitor terminal.
18	CAP4	Peak detector 4 capacitor terminal.
19	GATE1	Peak detector 1 gate input (TTL) high enabled, low disabled.
20	GATE2	Peak detector 2 gate input (TTL) high enabled, low disabled.
21	GATE3	Peak detector 3 gate input (TTL) high enabled, low disabled.
22	GATE4	Peak detector 4 gate input (TTL) high enabled, low disabled.
23	TP	Composite test point, normally left unconnected.
24	C_{DC}	External capacitor terminal to set DC restore response.
25	SYNC	SYNC pulse output (TTL).
26	POSA	Position output A.
27	POSB	Position output B.
28	FDEC	Charge pump frequency decrement input (TTL).

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Power Supply Voltage, V_{CC} 14V
Input Voltages:
- GAIN1, GAIN2 ..... −0.3 to 8V
- C_{AGC} ..... −0.3 to 7.0V
- V_{AGC} ..... −0.3 to 5.3V
- CAP1, CAP2, CAP3, CAP4 ..... −0.3 to 10V
- GATE1, GATE2, GATE3, GATE4, VCOP ..... −0.3 to 7.5V
- INX, INY, VCON, VCOI, $\overline{\text{FINC}}$, FDEC, C_{DC} ..... −0.3 to V_{CC} +0.3V

Θ_{JA} for 28-Pin Plastic DIP ..... ≈60°C/Watt
Θ_{JA} for 28-Pin PLCC ..... 60°C/Watt
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_{JMAX}) ..... 150°C
Lead Temperature (Soldering, 10sec) ..... 260°C

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
Supply Voltage (V_{CC}) ..... $12V_{DC} \pm 10\%$
Input Coupling Capacitance (Ci) 0.01μF
Input Amp Gain Capacitance (C_G) 0.047μF
Input Amp Gain Resistance (R_G) 1kΩ
AGC Response Compensation Capacitance (C_A) 0.082μF
Composite DC Restore Capacitance (C_D) 0.01μF
PLL Compensation Components:
- C_{CP1} 0.1μF
- C_{CP2} 1μF
- R_{CP} 910Ω

PLL Gain Components:
- R_V 1000Ω
- RL1, RL2 ..... 1000Ω

Peak Detector Capacitance (CAP1 thru CAP4) 270pF
SYNC Output Pull-Up Resistor (to 5V) 1000Ω
On track Base-to-Peak Voltage at pin TP 1.75V
V_{GA} Gain Control Voltage (at pin C_{AGC}) 0.65V

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of $T_A = 0$ to 70° C, $V_{CC} = 10.8$ to 13.2V, $V_{VAGC} = 5.0$V, and external components as recommended above, unless otherwise specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
Power Supply						
I_{CC}	Supply Current	$V_{CC} = 12$V		81	110	mA
TTL Inputs $\overline{\text{FINC}}$, FDEC, GATE1, GATE2, GATE3, GATE4						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IH} = 2.4$V	−1		30	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0.4$V	−20		1	μA
SYNC Output (TTL Open Collector) See Note 3						
V_{OL}	Low Level Output Voltage	$I_{OL} = 1.6$mA	0	0.3	0.5	V
V_{THR}	Positive going input threshold			$V_{REF}+0.9$		V
V_{THF}	Negative going input threshold			V_{REF}		V
$t_{PD} \pm$	Propagation Delay Rising, Falling	RL = 2k, $C_L = 15$pF		50		ns
VCOP Output ML4401 ($T_A = 25°C$)						
V_{OH}	High Level Output Voltage	RL = 1kΩ	4.0	4.3	4.6	V
V_{OL}	Low Level Output Voltage	RL = 1kΩ	2.9	3.2	3.5	V
VCOP Output ML4411						
V_{OH}	High Level Output Voltage	$I_{OH} = 50\mu$A	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 1.6$mA	0		0.5	V
VCO and Charge Pump Section						
I_{BIAS}	V_{COI} Input Bias Current		0	25	50	μA
I_{CH}, I_{DIS}	V_{COL} Charge and Discharge Current		495	660	825	μA
I_{CH}/I_{DIS}	V_{COL} Charge/Discharge Ratio		0.95	1.00	1.05	μA/μA
I_{OFF}	V_{COL} OFF State Current	$\overline{\text{FINC}} = 2.0$ FDEC = 0.8	0	25	50	nA

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of T_A = 0 to 70° C, V_{CC} = 10.8 to 13.2 V, V_{AGC} = 5.0 V, and external components as recommended above, unless specified (See Note 1.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 2	MAX	UNITS
VCO and Charge Pump Section (Continued)						
F_{MAX}	MAX VCO Frequency to Maintain + and − 5% Control Range Note 4		30			MHz
F_{VCO}	VCO Frequency Range Note 4	T_A = 25° C, V_{CC} = 12 C_V = 100 pF, R_V = 604 kΩ	9.7	10.0	10.3	MHz
K_{VCO}	VCO Voltage to Frequency Factor			2		%/V
Input AMP, AGC AMP, and DC Restore						
R_{IN}	INX, INY Differential Input Resistance		7	10	14	kΩ
$I_{GAIN1, 2}$	GAIN1, GAIN2 Bias Current		0.66	1.0	1.20	mA
I_{BIAS}	V_{AGC} Input Bias Current		0	5	20	μA
G_{MAGC}	AGC Transconductance at C_{AGC}			370		μMHOS
R_{AGC}	Control Range of AGC Loop to Regulate Composite Amplitude to within 2% of Nominal			7/1		V/V
BW	Bandwidth from INX, INY to Composite Note 4		10	15		MHz
GMDCR	DC Restore Transconductance			200		μMHOS
Peak Detectors						
I_{CH}	Charge Current		5			mA
I_{DIS}	Discharge Current	T_A = 25° C	25	45	60	μA
T_{CDIS}	Tempco of I_{DIS}			−0.17		μA/° C
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25° C	4.85	5.10	5.35	V
TC	Tempco			50		ppm/° C
R_{OUT}	Load Regulation			2		mV/mA
PSRR	Line Regulation			10		mV/V
I_{SINK}	Maximum SINK Current		0.8			mA
Output Amplifiers (POSA, POSB)						
V_{OS}	Input Offset	V_{CAP}1-4 = 6 V	−10	0	10	mV
A_V	Gain		1.20	1.25	1.30	V/V
A_{VA}/A_{VB}	Gain Tracking		−3	0	+3	%
V_{OUT}	Output Voltage Range		1.0		9.5	V
I_{SRC}	Output Source Current		5			mA
I_{SNK}	Output Sink Current		2			mA
SR	Slew Rate			2.5		V/μs
BW	3 dB Gain Bandwidth			3		MHz

Note 1: 0° C to 70° C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Typicals are parametric norm at 25° C.

Note 3: Pin 25 is an open collector output which should not exceed 7 volts in the high state.

Note 4: This parameter is guaranteed but not 100% tested and is not used in outgoing quality level calculations.

APPLICATION HINTS

Using a nominal on-track servo signal, amplitude adjustment should be made as follows:

1. Set composite signal amplitude, measured at pin TP, by adjusting voltage at pin V_{AGC} (approximately 4.7 volts). The composite signal should be set to 1.75 volts base to peak of an on-track position pulse (an off-track position pulse will be about 3.5 volts maximum).
2. Adjust Rg so that the VGA is in mid-range. This is determined by measuring the voltage at pin C_{AGC}; it should be approximately 0.9 volts. C_{AGC} voltage will vary approximately ±0.5 volts over the AGC range.

FUNCTIONAL DESCRIPTION

Input Amplifier

The input amplifier is equivalent to a wide-band 592 type video amplifier and provides amplification and buffering to the AGC circuitry. The Inputs INX and INY, which must be AC coupled, accept the composite analog signal from the servo head differential preamplifier. Internal input termination resistors eliminate the need for external bias resistors. Prefiltering of the signal is normaly desired to eliminate unwanted components. External components R_G and C_G determine the input amplifier's low frequency cutoff and gain as follows:

$$FC = \frac{1}{2\pi\ (R_G + 60\Omega)\ C_G} \qquad A_V = \frac{1700}{R_G + 60\Omega}$$

Where: C_G = External series capacitance between pins GAIN1 and GAIN2

R_G = External series resistance between pins GAIN1 and GAIN2

Automatic Gain Control (AGC)

The purpose of the AGC loop is to maintain a constant peak output voltage level at outputs POSA and POSB. This peak level is established by the reference voltage applied to pin V_{AGC}.

$$V_{P\text{-}P\ (Composite)} = K1 \times V_{AGC} + K2$$

Where: K1 = 0.65

K2 = 0.41V

In this closed-loop system, the peak detector output voltages are fed back and combined with the V_{AGC} voltage to provide a gain control current. The current controls the variable gain amplifier (VGA) and is compensated at pin C_{AGC} to provide control of AGC bandwidth. The bandwidth of the entire AGC loop is determined by:

$$BW = \frac{K\ V_{VAGC}}{2\pi\ C_A}$$

Where: $K = 4.3 \times 10^{-4}$

V_{VAGC} = External reference voltage at pin V_{AGC}

C_A = External capacitance at pin C_{AGC}

Optimum system stability is achieved by deriving V_{VAGC} from the V_{REF} output using a resistive divider.

Composite Amplifier

The input amplifier and AGC circuit of the ML4401 operate in a differential signal mode to provide good common mode and power supply rejection. The composite amplifier converts the differential signal into a buffered single-ended signal for the peak detector circuitry. The DC base line of the composite signal is equal to V_{REF}. The bandwidth of the DC restore function is controlled by capacitor C_D at pin C_{DC} with the following relationship:

$$BW = \frac{gm}{2\pi\ C_D}$$

Where: gm = 1/5 kΩ

C_D = External capacitance at pin C_{DC}

The composite signal is available at pin TP and is normally left unconnected. For short circuit protection a 425Ω resistor is connected in series with pin TP internally.

Synchronization Pulse Separator

The SYNC pulse separator is a threshold comparator with hysteresis which passes pulses from the composite amplifier above a set threshold. It provides a buffered open collector TTL output. The SYNC output, when gated through an external one-shot, is used to control the external gate timing and PLL logic.

Peak Detector

The peak detector circuit captures the peak signal amplitude of the di-bit pulses. The gates are controlled by inputs GATE1 through GATE4. Timing is established by the external logic circuitry. The external peak detector capacitors are connected from pins CAP1 through CAP4 to ground. The peak detector discharge rate (set by CAP1-CAP4) determines the maximum track crossing rate during an access operation. The performance of this block can be enhanced by using the velocity output of the ML4403, ML4413 to create a velocity proportional discharge. The peak detector outputs are fed into internal differential amplifiers that calculate the track error signals and provide buffered outputs POSA and POSB as follows:

POSA = 1.25 (CAP1 − CAP2) + V_{REF}

POSB = 1.25 (CAP3 − CAP4) + V_{REF}

Voltage Controlled Oscillator and Charge Pump

The VCO and external phase compare logic provide a time base for peak detector gate sychronization. Inputs $\overline{FINC}$ and FDEC provide increment and decrement signals to the charge pump for changing the oscillator frequency. The $\overline{FINC}$ and FDEC inputs gate the charge pump for the duration of the pulse width. The RC timing network formed by C_V and R_V at pins VCOI, VCON, and VCOP control the oscillators center frequency. (See Typical Performance Characteristics)

R_V should be greater than 330Ω. Too low of a value will result in excessive power dissipation. RL1, RL2 and R_V should be approximately equal, although the values of RL1 and RL2 do not require accuracy.

The VCO output should only be taken from pin VCON. Charge pump capacitor C_{CP1} is connected from pin VCOL to ground. Components R_{CP} and C_{CP2} are also connected in series from pin VCOL to ground to provide VCO loop compensation.

Internal Voltage Reference

V_{REF} is an internal band-gap voltage reference. It is buffered and available at pin V_{REF} and is used by the ML4402, ML4403, ML4404 and other chips requiring a 5 volt reference.

External Logic

The external logic provided by the user typically has a complexity of about 150 to 300 equivalent gates. Complexity and architecture depends on the users di-bit pattern and control function.

Note: Stray capacitance should be considered in applying the above relationships when low capacitor values are used. Stray capacitance of the integrated circuit terminal is typically about 2 to 3 pF.

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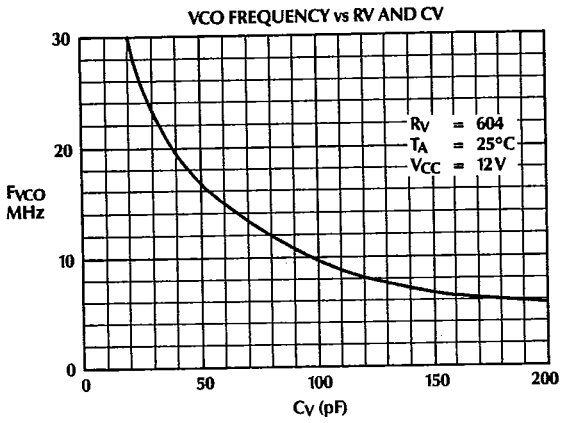
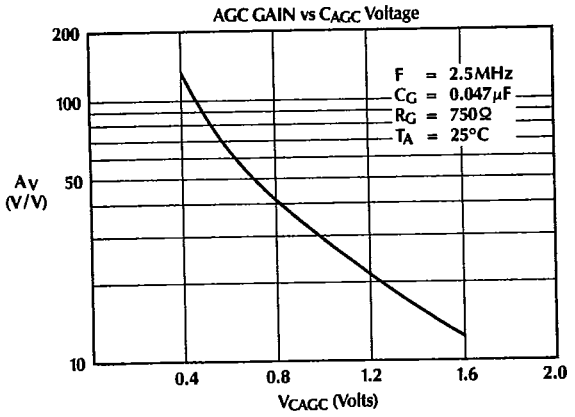
TYPICAL PERFORMANCE CHARACTERISTICS





T-52-33-11

ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	PIN COUNT	TEMPERATURE RANGE	COMMENTS
ML4401CP	Plastic DIP	28 PINS	0°C to +70°C	ECL Output
ML4401CQ	Molded PCC	28 PINS	0°C to +70°C	ECL Output
ML4411CP	Plastic DIP	28 PINS	0°C to +70°C	TTL Output
ML4411CQ	Molded PCC	28 PINS	0°C to +70°C	TTL Output

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