

Z86C91

CMOS Z8® ROMLESS MICROCONTROLLER

FEATURES

- 8-Bit CMOS ROMless Microcontroller
- 40-Pin DIP, 44-Pin PLCC, or 44-Pin QFP Package
- 4.5V to 5.5V Operating Range
- Low Power Consumption: 275 mW (max) @ 20 MHz
- Fast Instruction Pointer: 1.0 μ s @ 12 MHz
- Two Standby Modes: STOP and HALT
- 24 Input/Output Lines
- Full-Duplex UART
- All Digital Inputs are TTL Levels
- Auto Latches
- 256 Byte Register File
 - 236 Bytes of General-Purpose RAM
 - 16 Bytes Control and Status Register
 - 4 Bytes for Ports
- Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.
- Six Vectored, Priority Interrupts from Eight Different Sources
- Clock Speeds: 12, 16, and 20 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.

GENERAL DESCRIPTION

The Z86C91 microcontroller (MCU) is a member of the ROMless Z8 single-chip microcontroller family with 236 bytes of RAM. The Z86C91 is offered in a 40-pin DIP, 44-pin PLCC or a 44-pin QFP and is manufactured in CMOS technology. The ROMless Z86C91 device offers the use of external memory, making this Z8 microcontroller well-suited for applications where code flexibility is required.

Zilog's low-cost and low-power consumption Z86C91 microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C91 architecture is characterized by Zilog's 8-bit microcontroller core with a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features.

For applications demanding powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists

of eight lines, and is configurable under software control to provided timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory. Three basic address spaces are available to support this configuration: Program Memory, Data Memory, and 236 general-purpose registers.

To unburden the system from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C91 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART (Figure 1).

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|--------------|-----------------|----------------------|
| Power Ground | V_{CC} GND | V_{DD} V_{SS} |

GENERAL DESCRIPTION (Continued)

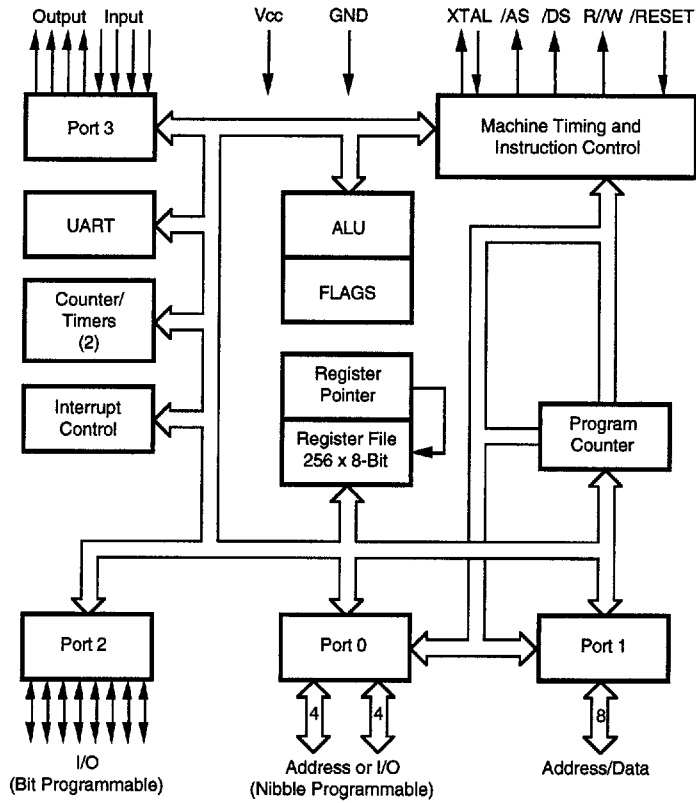
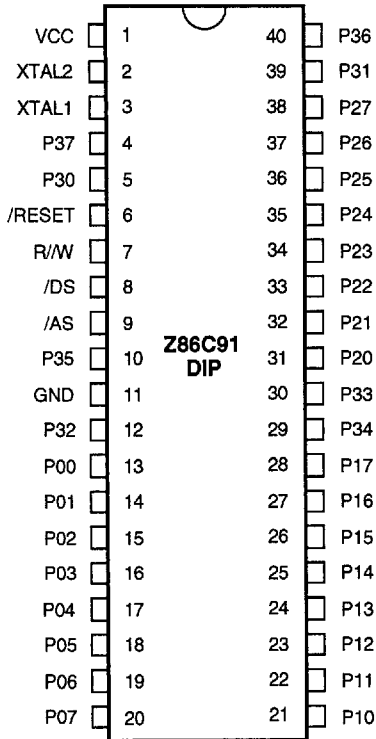
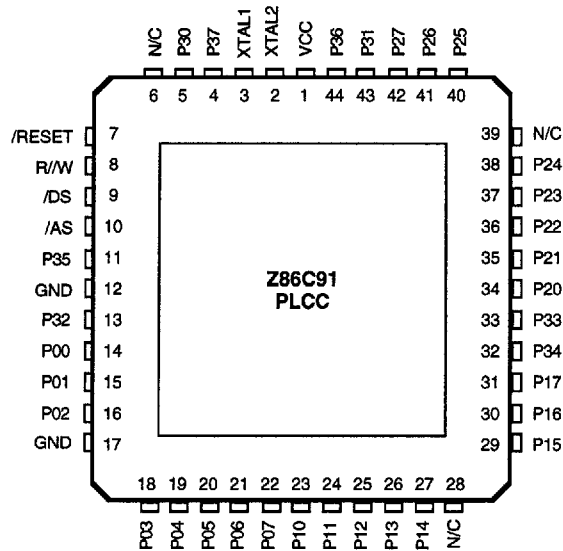


Figure 1. Z86C91 Functional Block Diagram

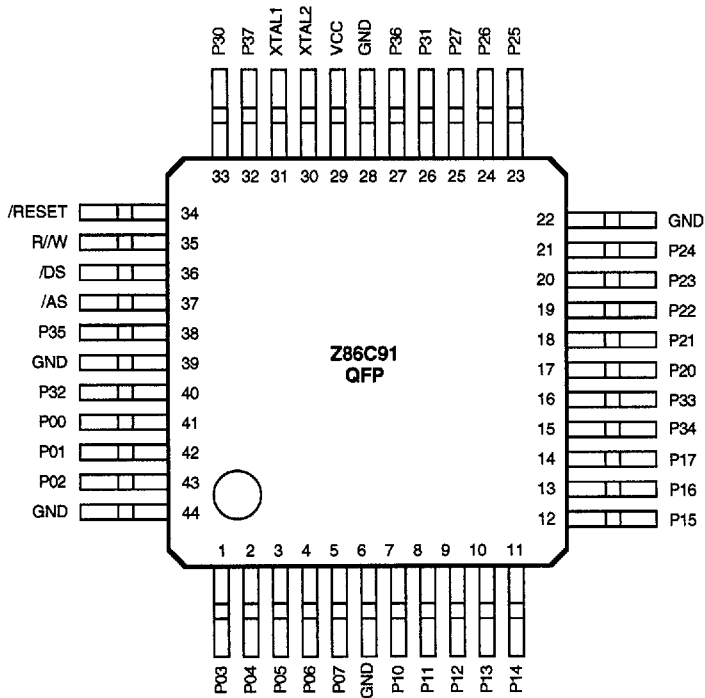
PIN DESCRIPTION

Table 1. 40-Pin DIP Pin Identification

| Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------------------|-----------|
| 1 | V _{CC} | Power Supply | Input |
| 2 | XTAL2 | Crystal, Oscillator Clock | Output |
| 3 | XTAL1 | Crystal, Oscillator Clock | Input |
| 4 | P37 | Port 3, Pin 7 | Output |
| 5 | P30 | Port 3, Pin 0 | Input |
| 6 | /RESET | Reset | Input |
| 7 | R/W | Read/Write | Output |
| 8 | /DS | Data Strobe | Output |
| 9 | /AS | Address Strobe | Output |
| 10 | P35 | Port 3, Pin 5 | Output |
| 11 | GND | Ground | Input |
| 12 | P32 | Port 3, Pin 2 | Input |
| 13-20 | P00-P07 | Port 0, Pins 0,1,2,3,4,5,6,7 | In/Output |
| 21-28 | P10-P17 | Port 1, Pins 0,1,2,3,4,5,6,7 | In/Output |
| 29 | P34 | Port 3, Pin 4 | Output |
| 30 | P33 | Port 3, Pin 3 | Input |
| 31-38 | P20-P27 | Port 2, Pins 0,1,2,3,4,5,6,7 | In/Output |
| 39 | P31 | Port 3, Pin 1 | Input |
| 40 | P36 | Port 3, Pin 6 | Output |

Figure 2. 40-Pin DIP Pin Assignments
11

PIN DESCRIPTION (Continued)

Figure 3. 44-Pin PLCC Pin Assignments
Table 2. 44-Pin PLCC Pin Identification

| Pin # | Symbol | Function | Direction | Pin # | Symbol | Function | Direction |
|-------|-----------------|---------------------------|-----------|-------|---------|------------------------|-----------|
| 1 | V _{CC} | Power Supply | Input | 14-16 | P00-P02 | Port 0, Pins 0,1,2 | In/Output |
| 2 | XTAL2 | Crystal, Oscillator Clock | Output | 17 | GND | Ground | Input |
| 3 | XTAL1 | Crystal, Oscillator Clock | Input | 18-22 | P03-P07 | Port 0, Pins 3,4,5,6,7 | In/Output |
| 4 | P37 | Port 3, Pin 7 | Output | 23-27 | P10-P14 | Port 1, Pins 0,1,2,3,4 | In/Output |
| 5 | P30 | Port 3, Pin 0 | Input | 28 | N/C | Not Connected | Input |
| 6 | N/C | Not Connected | Input | 29-31 | P15-P17 | Port 1, Pins 5,6,7 | In/Output |
| 7 | /RESET | Reset | Input | 32 | P34 | Port 3, Pin 4 | Output |
| 8 | R/W | Read/Write | Output | 33 | P33 | Port 3, Pin 3 | Input |
| 9 | /DS | Data Strobe | Output | 34-38 | P20-P24 | Port 2, Pins 0,1,2,3,4 | In/Output |
| 10 | /AS | Address Strobe | Output | 39 | N/C | Not Connected | Input |
| 11 | P35 | Port 3, Pin 5 | Output | 40-42 | P25-P27 | Port 2, Pins 5,6,7 | In/Output |
| 12 | GND | Ground | Input | 43 | P31 | Port 3, Pin 1 | Input |
| 13 | P32 | Port 3, Pin 2 | Input | 44 | P36 | Port 3, Pin 6 | Output |


Figure 4. 44-Pin QFP Pin Assignments
Table 3. 44-Pin QFP Pin Identification

| Pin # | Symbol | Function | Direction | Pin # | Symbol | Function | Direction |
|-------|-----------------|------------------------------|-----------|-------|---------|---------------------------|-----------|
| 1-5 | P03-P07 | Port 0, Pins 3,4,5,6,7 | In/Output | 31 | XTAL1 | Crystal, Oscillator Clock | Input |
| 6 | GND | Ground | Input | 32 | P37 | Port 3, Pin 7 | Output |
| 7-14 | P10-P17 | Port 1, Pins 0,1,2,3,4,5,6,7 | In/Output | 33 | P30 | Port 3, Pin 0 | Input |
| 15 | P34 | Port 3, Pin 4 | Output | 34 | /RESET | Reset | Input |
| 16 | P33 | Port 3, Pin 3 | Input | 35 | R/W | Read/Write | Output |
| 17-21 | P20-P24 | Port 2, Pins 0,1,2,3,4 | In/Output | 36 | /DS | Data Strobe | Output |
| 22 | GND | Ground | Input | 37 | /AS | Address Strobe | Output |
| 23-25 | P25-P27 | Port 2, Pins 5,6,7 | In/Output | 38 | P35 | Port 3, Pin 5 | Output |
| 26 | P31 | Port 3, Pin 1 | Input | 39 | GND | Ground | input |
| 27 | P36 | Port 3, Pin 6 | Output | 40 | P32 | Port 3, Pin 2 | Input |
| 28 | GND | Ground | Input | 41-43 | P00-P02 | Port 0, Pins 0,1,2 | In/Output |
| 29 | V _{cc} | Power Supply | Input | 44 | GND | Ground | Input |
| 30 | XTAL2 | Crystal, Oscillator Clock | Output | | | | |

PIN FUNCTIONS

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external program. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C91 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is

held active Low while /AS cycles at a rate of TpC2. When /RESET is deactivated program, execution begins at location 000C (HEX). Power-up reset time is held Low for 50 ms, or until V_{cc} is stable, whichever is longer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 provides Address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

After a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 5).

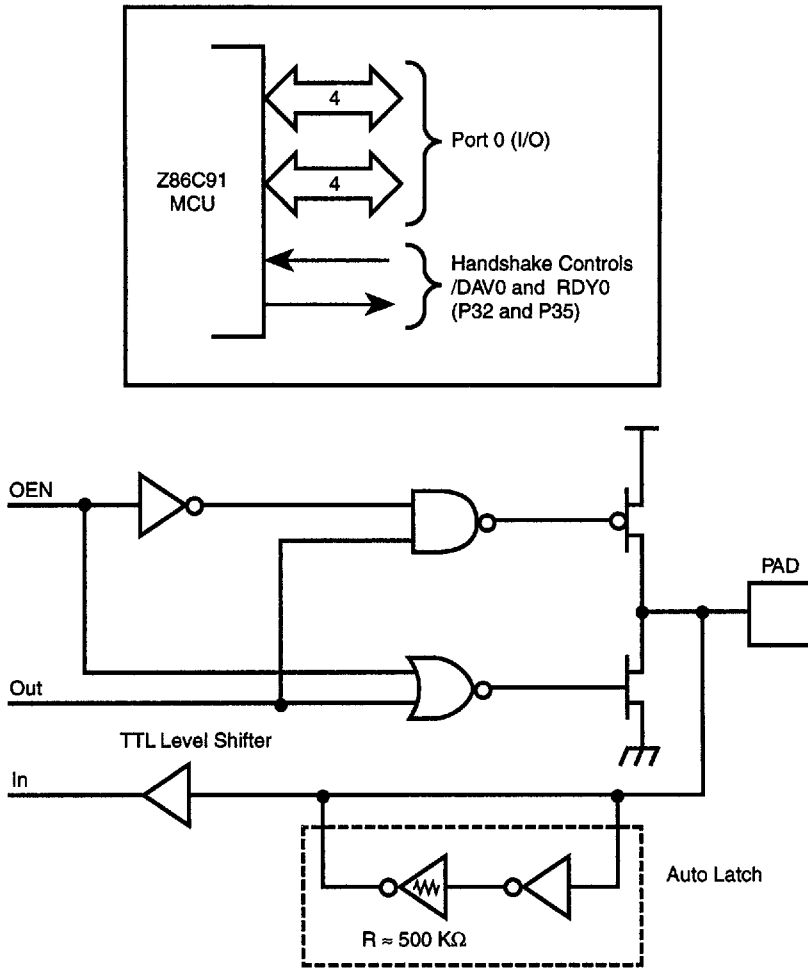


Figure 5. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports for interfacing external memory.

Port 1 can be placed in a high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 6).

If more than 256 external locations are required, Port 0 must output the additional lines.

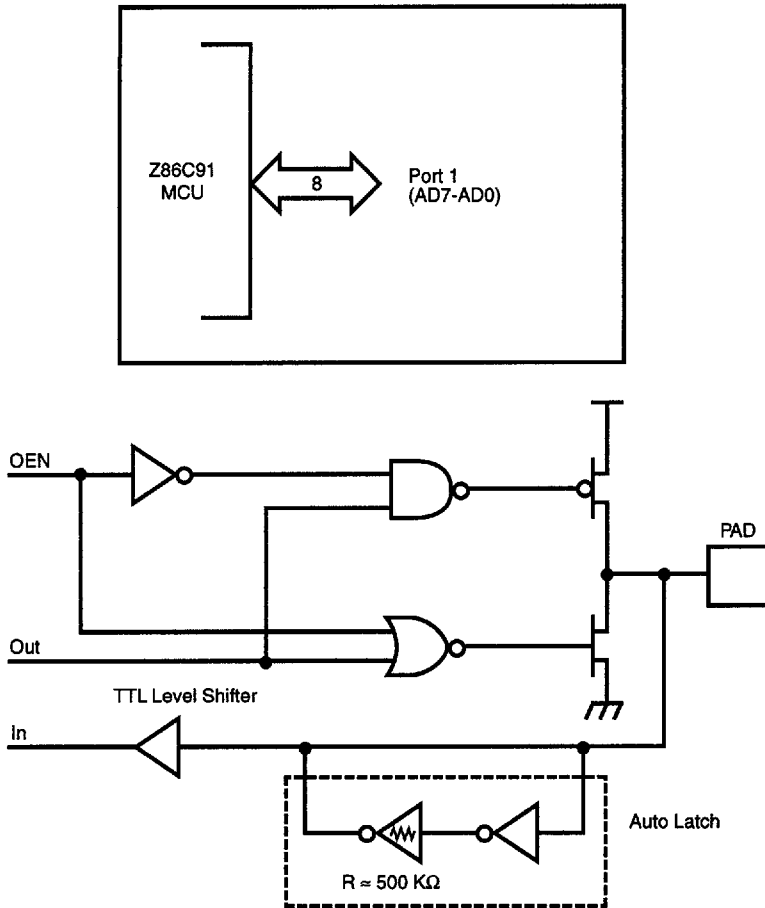


Figure 6. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bidirectional, TTL compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port

2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7).

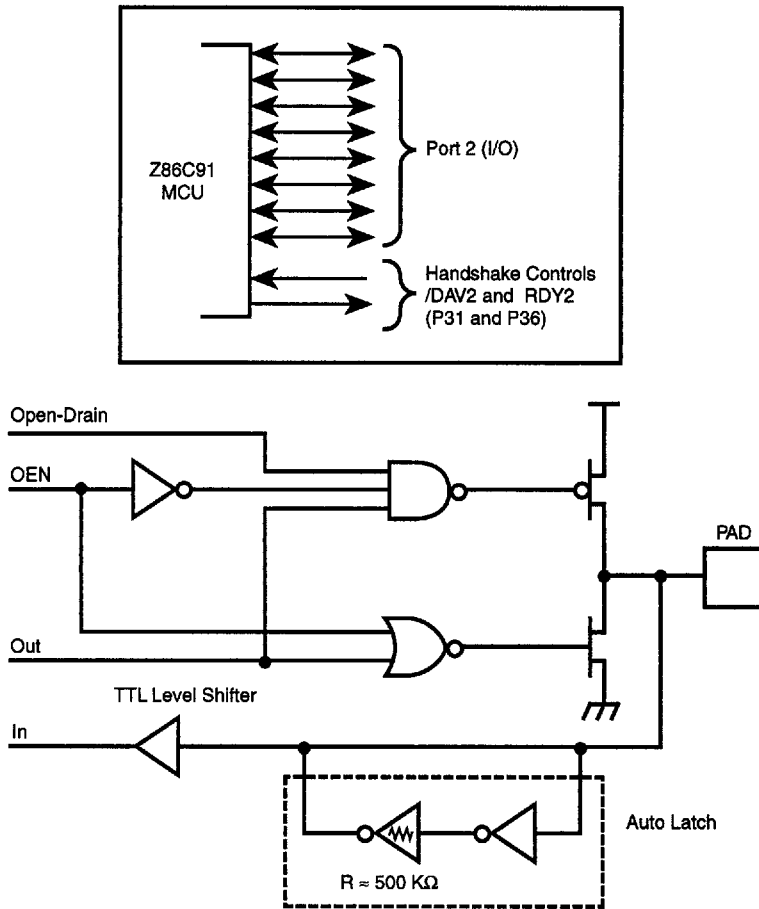


Figure 7. Port 2 Configuration

PIN FUNCTION (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, TTL compatible four fixed input and four fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four fixed (P37-P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 8). Port 3 inputs only are designed with Auto Latches.

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM) (Table 4.)

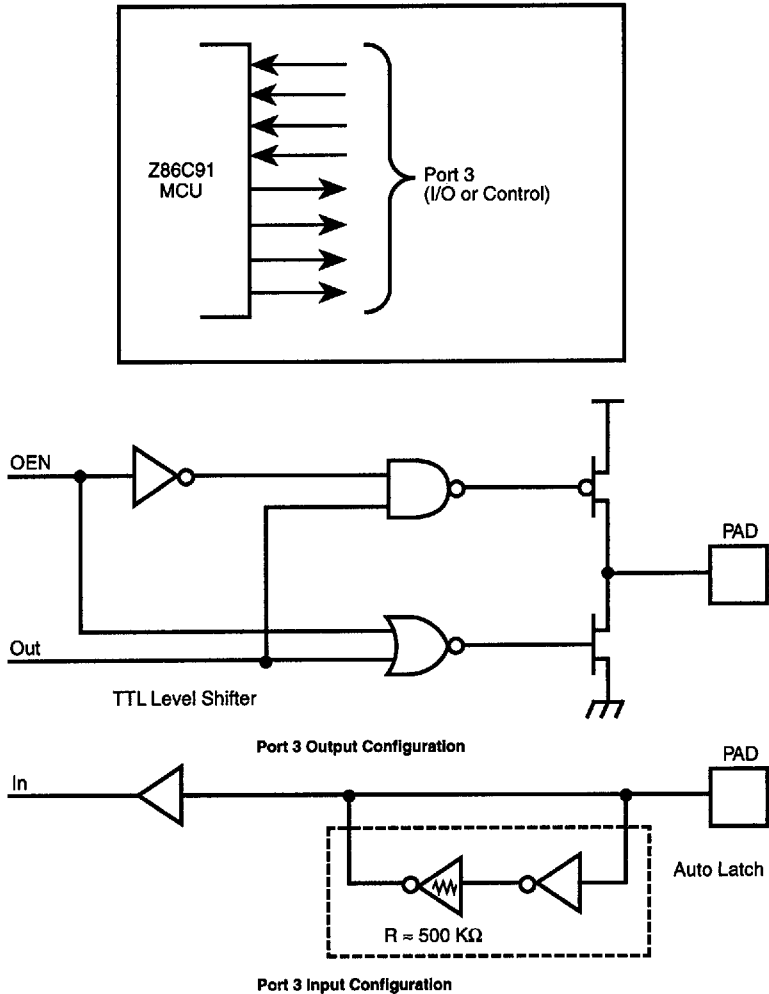


Figure 8. Port 3 Configuration

Table 4. Port 3 Pin Assignments

| Pin | I/O | CTC1 | Int. | P0 HS | P1 HS | P2 HS | UART | Ext |
|-----|-----|------------------|------|-------|-------|-------|------------|-----|
| P30 | IN | | IRQ3 | | | | Serial In | |
| P31 | IN | T _{IN} | IRQ2 | | | D/R | | |
| P32 | IN | | | IRQ0 | D/R | | | |
| P33 | IN | | IRQ1 | | D/R | | | |
| P34 | OUT | | | | R/D | | | DM |
| P35 | OUT | | | R/D | | | | |
| P36 | OUT | T _{OUT} | | | | R/D | | |
| P37 | OUT | | | | | | Serial Out | |
| T0 | | | IRQ4 | | | | | |
| T1 | | | IRQ5 | | | | | |

Notes:

HS = HANDSHAKE SIGNALS
D = Data Available
R = Ready

UART OPERATION

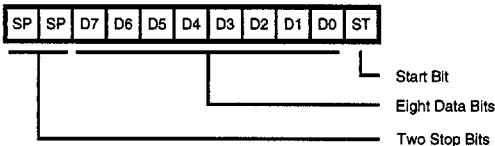
Port 3 lines P30 and P37, are programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

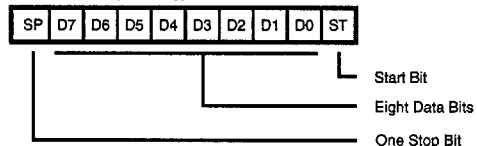
The Z86C91 automatically adds a start bit and two stop bits to transmitted data (Figure 9). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

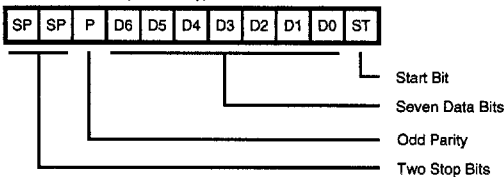
Transmitted Data (No Parity)



Received Data (No Parity)



Transmitted Data (With Parity)



Received Data (With Parity)

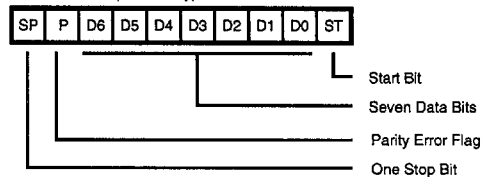


Figure 9. Serial Data Formats

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C91 can address up to 64 Kbytes of external program memory (Figure 10). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location 000CH after a reset.

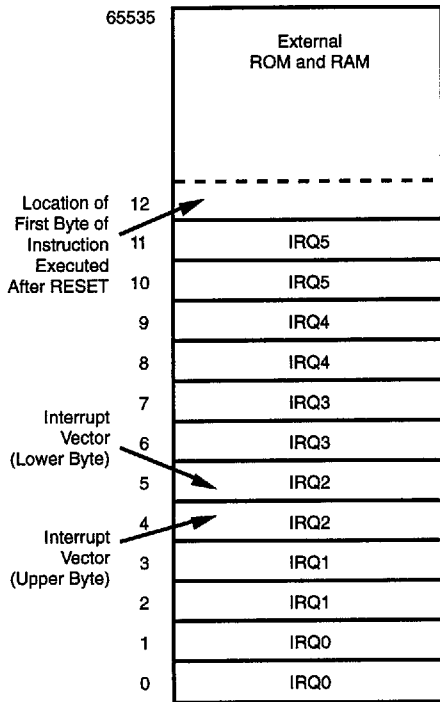


Figure 10. Program Memory Configuration

Data Memory (/DM). The Z86C91 addresses up to 64 Kbytes of external data memory space. External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on P34, is used to distinguish between data and program memory space (Figure 11). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

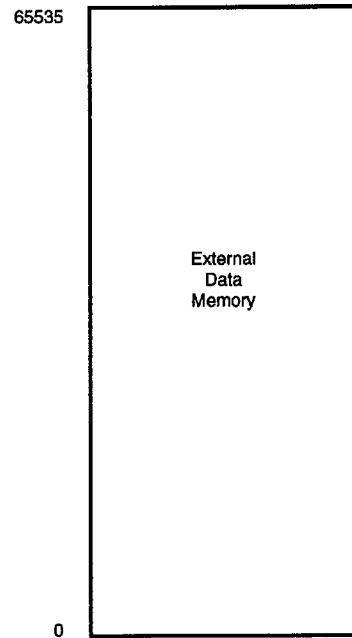


Figure 11. Data Memory Configuration

Register File. The Register File consists of three I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 12). The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 13). In the 4-bit mode, the Register File is divided into 16 working

register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group. For the reset and power-up conditions of the Register File see Figure 14.

Note: Register Bank E0-EF is only accessed through working register and indirect addressing modes.

| LOCATION | | IDENTIFIERS | |
|----------|-----------------------------|-------------|----|
| R255 | Stack Pointer (Bits 7-0) | SPL | |
| R254 | Stack Pointer (Bits 15-8) | SPH | |
| R253 | Register Pointer | RP | |
| R252 | Program Control Flags | FLAGS | |
| R251 | Interrupt Mask Register | IMR | |
| R250 | Interrupt Request Register | IRQ | |
| R249 | Interrupt Priority Register | IPR | |
| R248 | Ports 0-1 Mode | P01M | |
| R247 | Port 3 Mode | P3M | |
| R246 | Port 2 Mode | P2M | |
| R245 | T0 Prescaler | PRE0 | |
| R244 | Timer/Counter0 | T0 | |
| R243 | T1 Prescaler | PRE1 | |
| R242 | Timer/Counter1 | T1 | |
| R241 | Timer Mode | TMR | |
| R240 | Serial I/O | SIO | |
| R239 | General-Purpose Registers | | |
| R4 | | | |
| R3 | | Port 3 | P3 |
| R2 | | Port 2 | P2 |
| R1 | Port 1 | P1 | |
| R0 | Port 0 | P0 | |

Figure 12. Register File

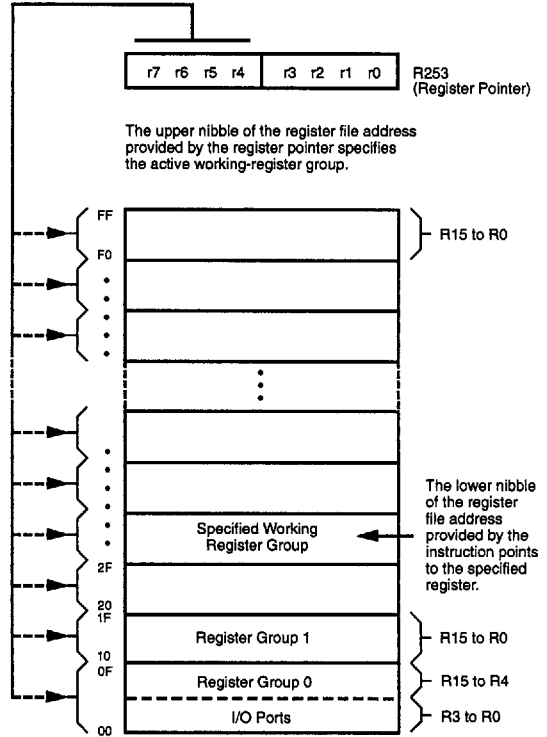


Figure 13. Register Pointer

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 15).

The 6-bit prescalers divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single

pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1 or sub the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1

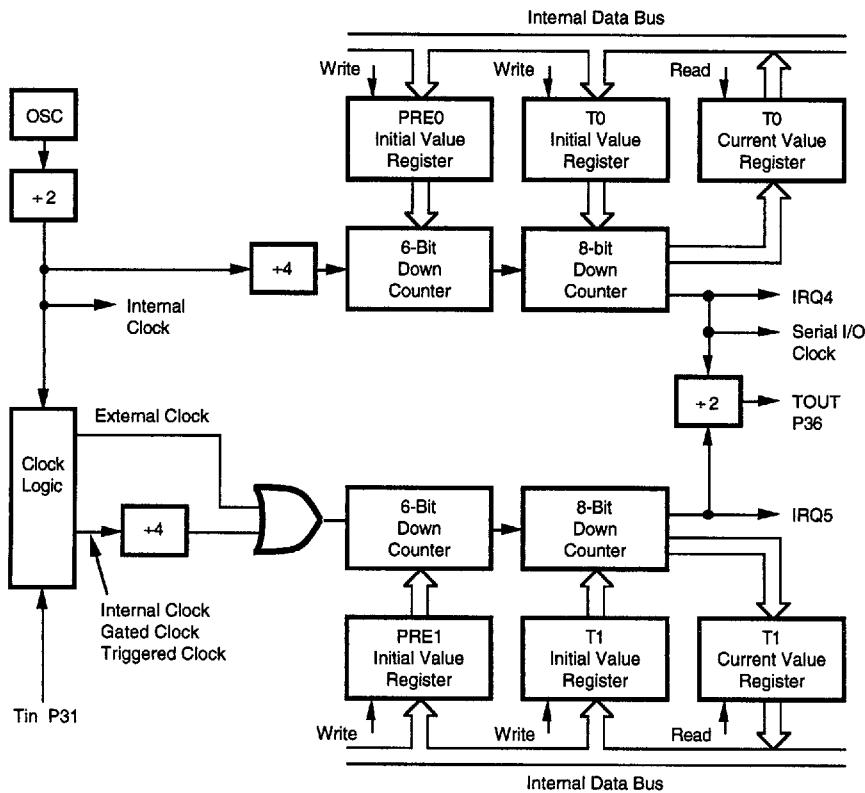


Figure 15. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86C91 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follow: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one in Serial In, and two in the counter/timers (Figure 16). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register (Refer to Table 4).

All Z86C91 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, save the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

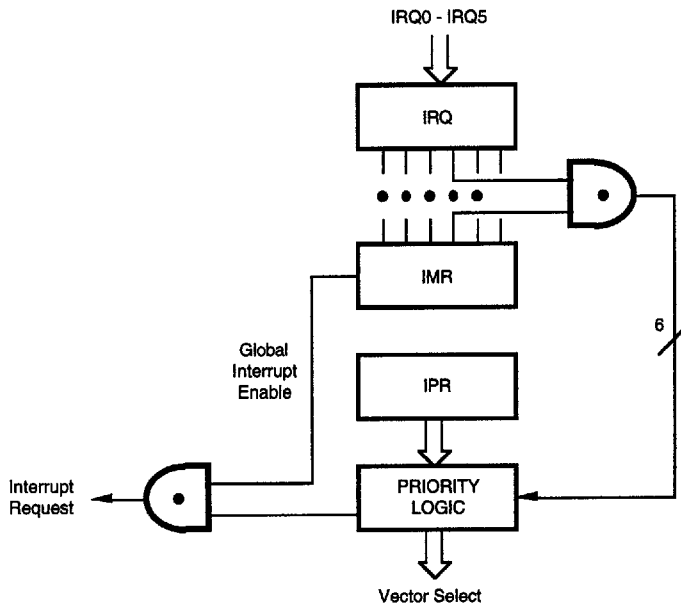


Figure 16. Interrupt Block Diagram

Clock. The Z86C91 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended

capacitors ($10\text{ pF} < CL < 300\text{ pF}$) from each pin 11 ground instead of just the system ground. This prevents noise injection into the clock inputs (Figure 17).

Note: Actual capacitor values specified by the crystal manufacturer.

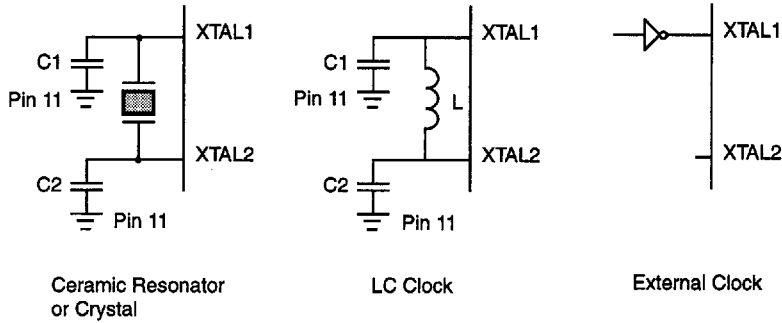


Figure 17. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to $5\text{ }\mu\text{A}$ (typical) or less. The STOP mode is terminated by a reset, which cause the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF NOP ; clear the pipeline
6F STOP ; enter STOP mode
or
FF NOP ; clear the pipeline
7F HALT ; enter HALT mode
```

ABSOLUTE MAXIMUM RATINGS

| Symbol | Description | Min | Max | Units |
|-----------|-------------------|------|------|-------|
| V_{CC} | Supply Voltage* | -0.3 | +7.0 | V |
| T_{STG} | Storage Temp | -65 | +150 | °C |
| T_A | Oper Ambient Temp | | † | °C |

Notes:

* Voltages on all pins with respect to GND.

† See Ordering Information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).

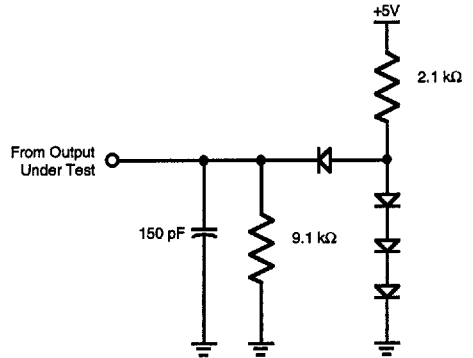


Figure 18. Test Load Diagram

DC CHARACTERISTICS

| Sym | Parameter | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | | $T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$ | | Typical @ 25°C | Units | Conditions |
|-----------|--------------------------|---|--------------|--|--------------|---------------------------------|---------------|---|
| | | Min | Max | Min | Max | | | |
| | Max Input Voltage | | 7 | | 7 | | V | $I_{IN} < 250 \mu\text{A}$ |
| V_{CH} | Clock Input High Voltage | 3.8 | $V_{CC}+0.3$ | 3.8 | $V_{CC}+0.3$ | | V | Driven by External Clock Generator |
| V_{CL} | Clock Input Low Voltage | -0.3 | 0.8 | -0.3 | 0.8 | | V | Driven by External Clock Generator |
| V_{IH} | Input High Voltage | 2 | $V_{CC}+0.3$ | 2.0 | $V_{CC}+0.3$ | | V | |
| V_{IL} | Input Low Voltage | -0.3 | 0.8 | -0.3 | 0.8 | | V | |
| V_{OH} | Output High Voltage | 2.4 | | 2.4 | | | V | $I_{OH} = -2.0 \text{ mA}$ |
| V_{OH} | Output High Voltage | $V_{CC} - 100 \text{ mV}$ | | $V_{CC} - 100 \text{ mV}$ | | | V | $I_{OH} = -100 \mu\text{A}$ |
| V_{OL} | Output Low Voltage | | 0.4 | | 0.4 | | V | $I_{OL} = +2.0 \text{ mA}$ |
| V_{RH} | Reset Input High Voltage | 3.8 | $V_{CC}+0.3$ | 3.8 | $V_{CC}+0.3$ | | V | |
| V_{RL} | Reset Input Low Voltage | -0.3 | 0.8 | -0.3 | 0.8 | | V | |
| I_{IL} | Input Leakage | -2 | 2 | -2 | 2 | | μA | $V_{IN} = 0\text{V}, V_{CC}$ |
| I_{OL} | Output Leakage | -2 | 2 | -2 | 2 | | μA | $V_{IN} = 0\text{V}, V_{CC}$ |
| I_{IR} | Reset Input Current | | -80 | | -80 | | μA | $V_{RL} = 0\text{V}$ |
| I_{CC} | Supply Current | | 30 | | 30 | 20 | mA | @ 12 MHz [1] |
| | | | 35 | | 35 | 24 | mA | @ 16 MHz [1] |
| | | | 50 | | 50 | | mA | @ 20 MHz [1] |
| I_{CC1} | Standby Current | | 6.5 | | 6.5 | 4 | mA | HALT mode $V_{IN} = 0\text{V}, V_{CC}$ @ 12 MHz [1] |
| | | | 7 | | 7 | 4.5 | mA | HALT mode $V_{IN} = 0\text{V}, V_{CC}$ @ 16 MHz [1] |
| | | | 8.5 | | 8.5 | | mA | HALT mode $V_{IN} = 0\text{V}, V_{CC}$ @ 20 MHz [1] |
| I_{CC2} | Standby Current | | 10 | | 20 | 1 | μA | STOP mode $V_{IN} = 0\text{V}, V_{CC}$ [1] |
| I_{ALL} | Auto Latch Low Current | -10 | 10 | -14 | 14 | 5 | μA | |

Note:

 [1] All inputs driven to either 0V or V_{CC} , outputs floating.

AC CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagram

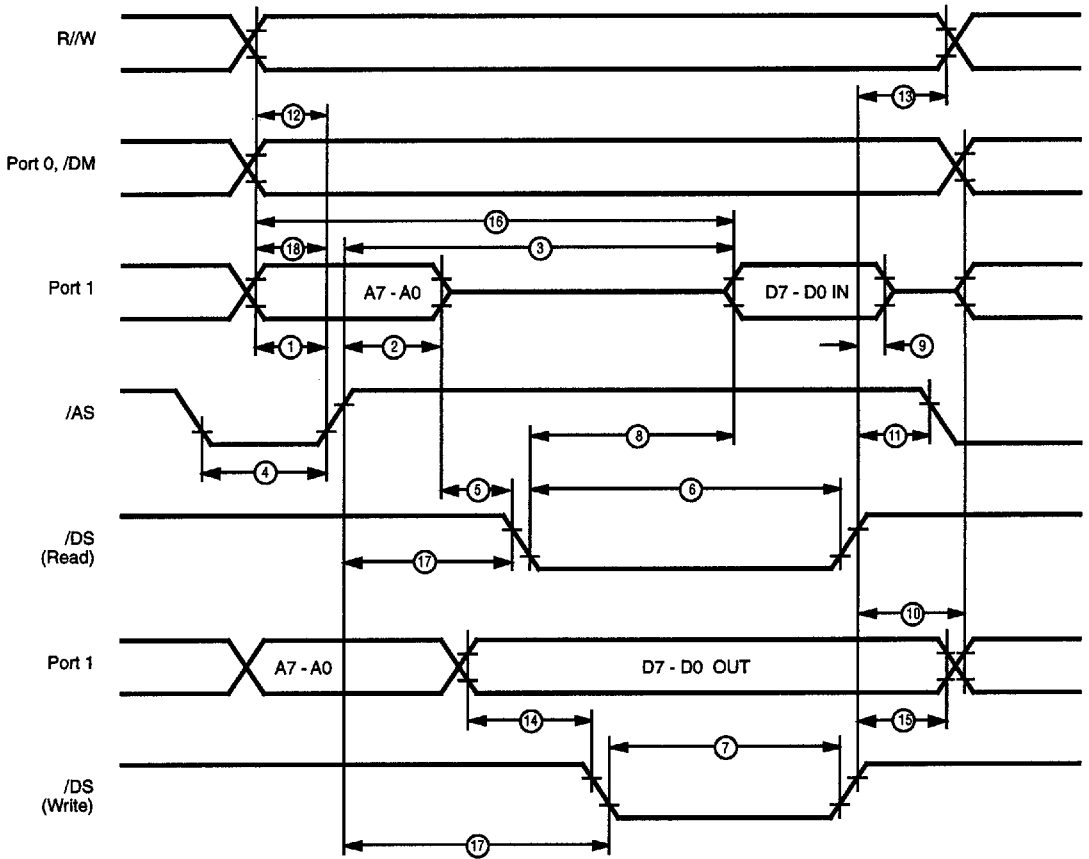


Figure 19. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read or Write Timing Table

| No | Sym | Parameter | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | | | | | | $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | | | | | | Units | Notes | |
|----|-----------|--|---|-----|--------|-----|--------|-----|--|-----|--------|-----|--------|-----|-------|---------|---------|
| | | | 12 MHz | | 16 MHz | | 20 MHz | | 12 MHz | | 16 MHz | | 20 MHz | | | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| 1 | TdA(AS) | Address Valid to /AS Rise Delay | 35 | 25 | 20 | 35 | 25 | 20 | 35 | 25 | 20 | 35 | 25 | 20 | ns | [2,3] | |
| 2 | TdAS(A) | /AS Rise to Address Float Delay | 45 | 35 | 25 | 45 | 35 | 25 | 45 | 35 | 25 | 45 | 35 | 25 | ns | [2,3] | |
| 3 | TdAS(DR) | /AS Rise to Read Data Req'd Valid | | 250 | 180 | 150 | 250 | 180 | 150 | 250 | 180 | 150 | 250 | 180 | 150 | ns | [1,2,3] |
| 4 | TwAS | /AS Low Width | 55 | 40 | 30 | 55 | 40 | 30 | 55 | 40 | 30 | 55 | 40 | 30 | ns | [2,3] | |
| 5 | TdAZ(DS) | Address Float to /DS Fall | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | | |
| 6 | TwDSR | /DS (Read) Low Width | 185 | 135 | 105 | 185 | 135 | 105 | 185 | 135 | 105 | 185 | 135 | 105 | ns | [1,2,3] | |
| 7 | TwDSW | /DS (Write) Low Width | 110 | 80 | 65 | 110 | 80 | 65 | 110 | 80 | 65 | 110 | 80 | 65 | ns | [1,2,3] | |
| 8 | TdDSR(DR) | /DS Fall to Read Data Req'd Valid | | 130 | 75 | 55 | 130 | 75 | 55 | 130 | 75 | 55 | 130 | 75 | 55 | ns | [1,2,3] |
| 9 | ThDR(DS) | Read Data to /DS Rise Hold Time | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns | [2,3] | |
| 10 | TdDS(A) | /DS Rise to Address Active Delay | 65 | 50 | 40 | 65 | 50 | 40 | 65 | 50 | 40 | 65 | 50 | 40 | ns | [2,3] | |
| 11 | TdDS(AS) | /DS Rise to /AS Fall Delay | 45 | 35 | 25 | 45 | 35 | 25 | 45 | 35 | 25 | 45 | 35 | 25 | ns | [2,3] | |
| 12 | TdR/W(AS) | R/W Valid to /AS Rise Delay | 30 | 25 | 20 | 33 | 25 | 20 | 33 | 25 | 20 | 33 | 25 | 20 | ns | [2,3] | |
| 13 | TdDS(R/W) | /DS Rise to R/W Not Valid | 50 | 35 | 25 | 50 | 35 | 25 | 50 | 35 | 25 | 50 | 35 | 25 | ns | [2,3] | |
| 14 | TdDW(DSW) | Write Data Valid to /DS Fall (Write) Delay | 35 | 25 | 20 | 35 | 25 | 20 | 35 | 25 | 20 | 35 | 25 | 20 | ns | [2,3] | |
| 15 | TdDS(DW) | /DS Rise to Write Data Not Valid Delay | 55 | 35 | 25 | 55 | 35 | 25 | 55 | 35 | 25 | 55 | 35 | 25 | ns | [2,3] | |
| 16 | TdA(DR) | Address Valid to Read Data Req'd Valid | 310 | 230 | 180 | 310 | 230 | 180 | 310 | 230 | 180 | 310 | 230 | 180 | ns | [1,2,3] | |
| 17 | TdAS(DS) | /AS Rise to /DS Fall Delay | 65 | 45 | 35 | 65 | 45 | 35 | 65 | 45 | 35 | 65 | 45 | 35 | ns | [2,3] | |
| 18 | TdDM(AS) | /DM Valid to /AS Rise Delay | 50 | 30 | 20 | 50 | 30 | 20 | 50 | 30 | 20 | 50 | 30 | 20 | ns | [2,3] | |

Notes:

[1] When using extended memory timing add 2TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

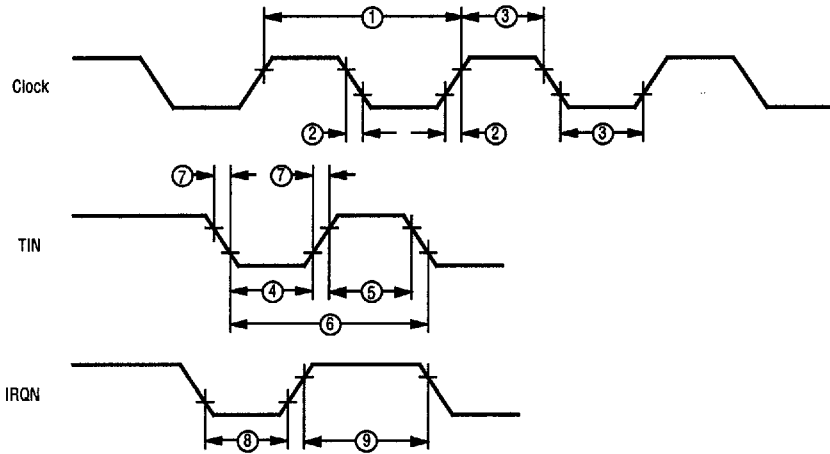
All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

| Number | Symbol | Equation |
|--------|-----------|----------------------|
| 1 | TdA(AS) | $0.40T_{pC} + 0.32$ |
| 2 | TdAS(A) | $0.59T_{pC} - 3.25$ |
| 3 | TdAS(DR) | $2.38T_{pC} + 6.14$ |
| 4 | TwAS | $0.66T_{pC} - 1.65$ |
| 6 | TwDSR | $2.33T_{pC} - 10.56$ |
| 7 | TwDSW | $1.27T_{pC} + 1.67$ |
| 8 | TdDSR(DR) | $1.97T_{pC} - 42.5$ |
| 10 | TdDS(A) | $0.8T_{pC}$ |
| 11 | TdDS(AS) | $0.59T_{pC} - 3.14$ |
| 12 | TdR/W(AS) | $0.4T_{pC}$ |
| 13 | TdDS(R/W) | $0.8T_{pC} - 15$ |
| 14 | TdDW(DSW) | $0.4T_{pC}$ |
| 15 | TdDS(DW) | $0.88T_{pC} - 19$ |
| 16 | TdA(DR) | $4T_{pC} - 20$ |
| 17 | TdAS(DS) | $0.91T_{pC} - 10.7$ |
| 18 | TdDM(AS) | $0.9T_{pC} - 26.3$ |

AC CHARACTERISTICS

Additional Timing Diagram


Figure 20. Additional Timing

AC CHARACTERISTICS

Additional Timing Table

| No | Sym | Parameter | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | | | | | | $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | | | | | | Units | Notes |
|----|--------------|------------------------------------|---|------|--------|------|--------|------|--|------|--------|------|--------|------|-------|-------|
| | | | 12 MHz | | 16 MHz | | 20 MHz | | 12 MHz | | 16 MHz | | 20 MHz | | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| 1 | TpC | Input Clock Period | 83 | 1000 | 62.5 | 1000 | 50 | 1000 | 83 | 1000 | 62.5 | 1000 | 50 | 1000 | ns | [1] |
| 2 | TrC, TfC | Clock Input Rise & Fall Times | 15 | | 10 | | 10 | | 15 | | 10 | | 10 | | ns | [1] |
| 3 | TwC | Input Clock Width | 35 | | 25 | | 15 | | 35 | | 25 | | 15 | | ns | [1] |
| 4 | TwTinL | Timer Input Low Width | 75 | | 75 | | 75 | | 75 | | 75 | | 75 | | ns | [2] |
| 5 | TwTinH | Timer Input High Width | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [2] |
| 6 | TpTin | Timer Input Period | 8TpC | | 8TpC | | 8TpC | | 8TpC | | 8TpC | | 8TpC | | | [2] |
| 7 | TrTin, TfTin | Timer Input Rise & Fall Times | 100 | | 100 | | 100 | | 100 | | 100 | | 100 | | ns | [2] |
| 8A | TwIL | Interrupt Request Input Low Times | 70 | | 70 | | 70 | | 70 | | 70 | | 70 | | ns | [2,4] |
| 8B | TwIL | Interrupt Request Input Low Times | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [2,5] |
| 9 | TwIH | Interrupt Request Input High Times | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | 5TpC | | | [2,3] |

Notes:

- [1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
- [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request through Port 3.
- [4] Interrupt request through Port 3 (P33-P31).
- [5] Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

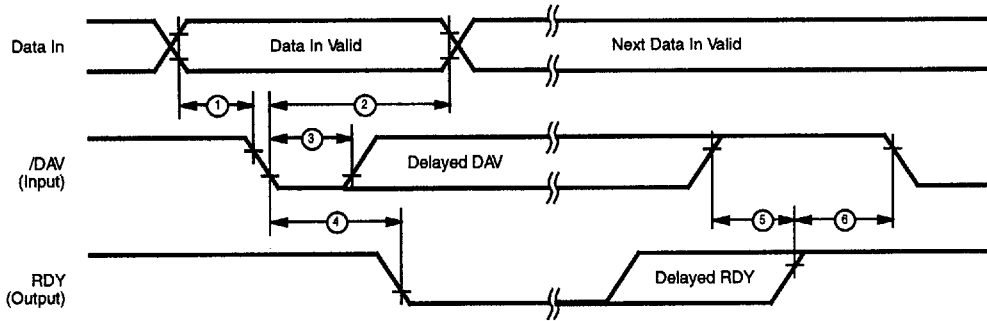


Figure 21. Input Handshake Timing

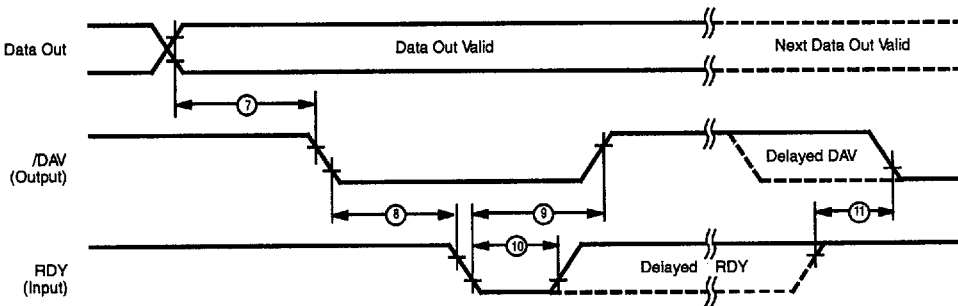


Figure 22. Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

| No | Sym | Parameter | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ | | Data Direction |
|----|--------------|----------------------------|---|-----|--|-----|----------------|
| | | | 12, 16, and 20 MHz Min | Max | 12, 16, and 20 MHz Min | Max | |
| 1 | TsDI(DAV) | Data In Setup Time | 0 | | 0 | | IN |
| 2 | ThDI(DAV) | Data In Hold Time | 145 | | 145 | | IN |
| 3 | TwDAV | Data Available Width | 110 | | 110 | | IN |
| 4 | TdDAVI(RDY) | DAV fall to RDY fall Delay | | 115 | | 115 | IN |
| 5 | TdDAVId(RDY) | DAV rise to RDY rise Delay | | 115 | | 115 | IN |
| 6 | TdRDYD(DAV) | RDY rise to DAV fall Delay | 0 | | 0 | | IN |
| 7 | TdDO(DAV) | Data Out to DAV fall Delay | | TpC | | TpC | OUT |
| 8 | TdDAVO(RDY) | DAV fall to RDY fall Delay | 0 | | 0 | | OUT |
| 9 | TdRDYD(DAV) | RDY fall to DAV rise Delay | | 115 | | 115 | OUT |
| 10 | TwRDY | RDY Width | 110 | | 110 | | OUT |
| 11 | TdRDYDd(DAV) | RDY rise to DAV fall Delay | | 115 | | 115 | OUT |

Z8 CONTROL REGISTER DIAGRAMS

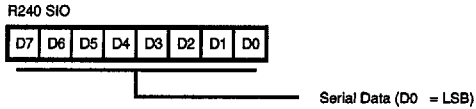


Figure 23. Serial I/O Register (F0_H: Read/Write)

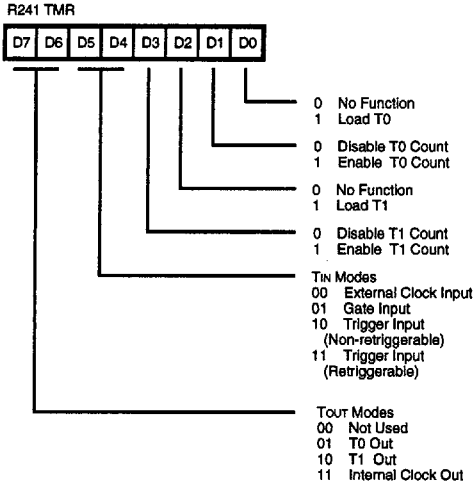


Figure 24. Timer Mode Register (F1_H: Read/Write)

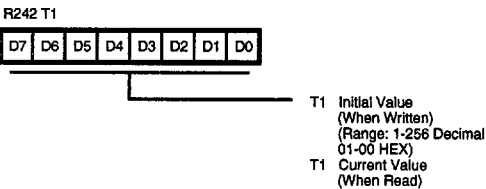


Figure 25. Counter/Timer 1 Register (F2_H: Read/Write)

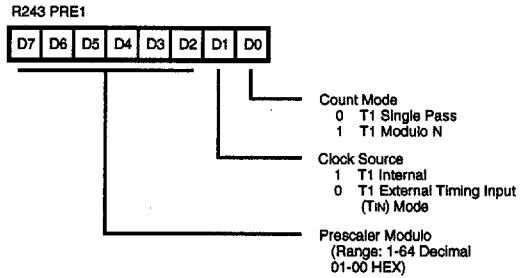


Figure 26. Prescaler 1 Register (F3_H: Write Only)

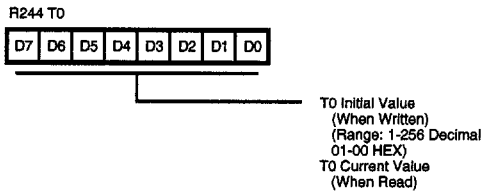


Figure 27. Counter/Timer 0 Register (F4_H: Read/Write)

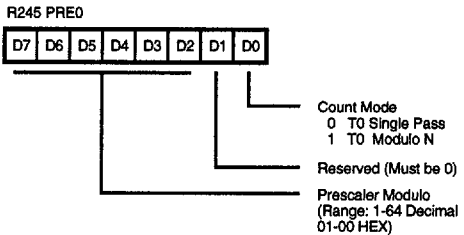


Figure 28. Prescaler 0 Register (F5_H: Write Only)

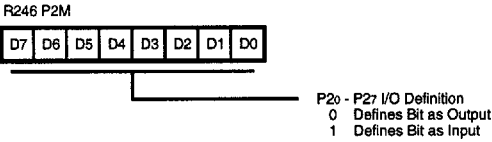


Figure 29. Port 2 Mode Register
(F6_H: Write Only)

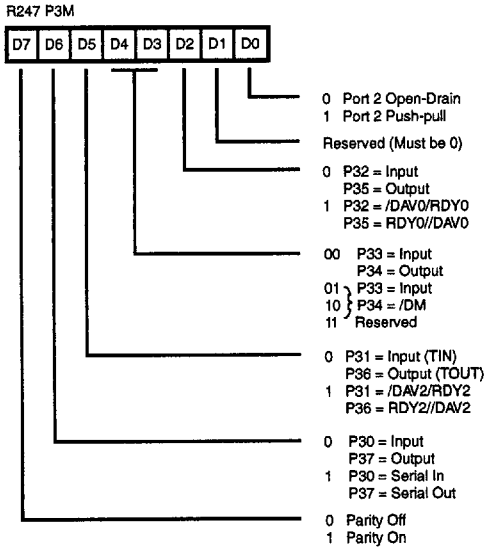


Figure 30. Port 3 Mode Register
(F7_H: Write Only)

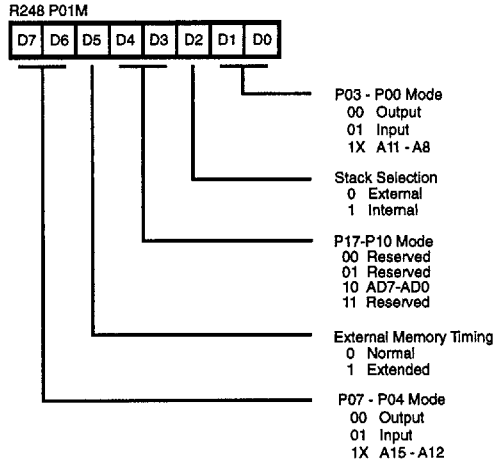


Figure 31. Port 0 and 1 Mode Register
(F8_H: Write Only)

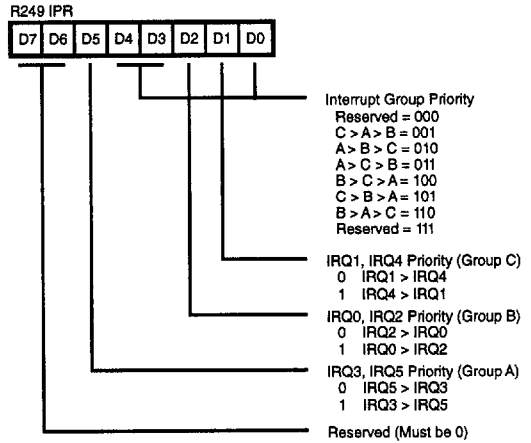


Figure 32. Interrupt Priority Register
(F9_H: Write Only)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

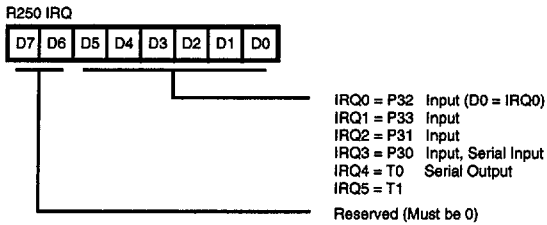


Figure 33. Interrupt Request Register (FA_n: Read/Write)

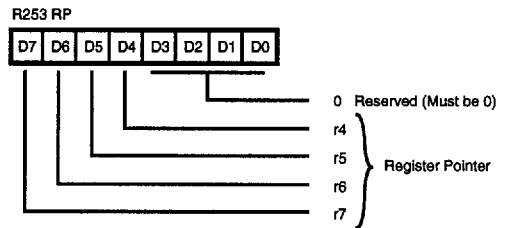


Figure 36. Register Pointer Register (FD_n: Read/Write)

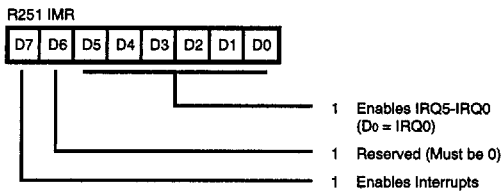


Figure 34. Interrupt Mask Register (FB_n: Read/Write)

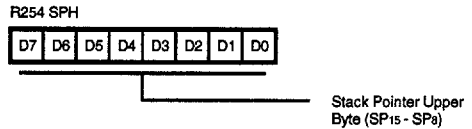


Figure 37. Stack Pointer Register (FE_n: Read/Write)

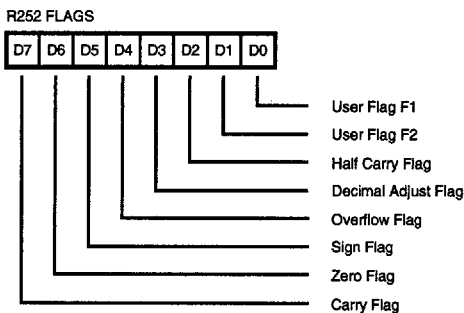


Figure 35. Flag Register (FC_n: Read/Write)

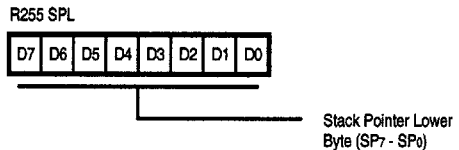


Figure 38. Stack Pointer Register (FF_n: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

| Symbol | Meaning |
|--------|--|
| IRR | Indirect register pair or indirect working-register pair address |
| Irr | Indirect working-register pair only |
| X | Indexed address |
| DA | Direct address |
| RA | Relative address |
| IM | Immediate |
| R | Register or working-register address |
| r | Working-register address only |
| IR | Indirect-register or indirect working-register address |
| Ir | Indirect working-register address only |
| RR | Register pair or working register pair address |

Symbols. The following symbols are used in describing the instruction set.

| Symbol | Meaning |
|--------|--------------------------------------|
| dst | Destination location or contents |
| src | Source location or contents |
| cc | Condition code |
| @ | Indirect address prefix |
| SP | Stack Pointer |
| PC | Program Counter |
| FLAGS | Flag register (Control Register 252) |
| RP | Register Pointer (R253) |
| IMR | Interrupt mask register (R251) |

Flags. Control register (R252) contains the following six flags:

| Symbol | Meaning |
|--------|---------------------|
| C | Carry flag |
| Z | Zero flag |
| S | Sign flag |
| V | Overflow flag |
| D | Decimal-adjust flag |
| H | Half-carry flag |

Affected flags are indicated by:

| | |
|---|-------------------------------------|
| 0 | Clear to zero |
| 1 | Set to one |
| * | Set to clear according to operation |
| - | Unaffected |
| x | Undefined |

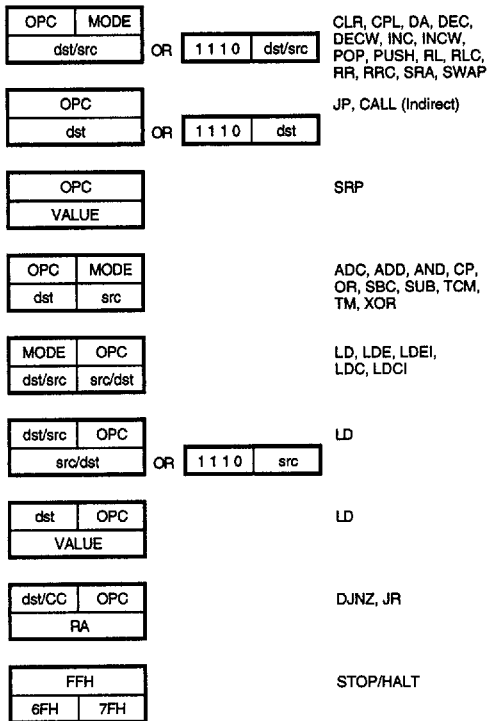
CONDITION CODES

| Value | Mnemonic | Meaning | Flags Set |
|-------|----------|--------------------------------|-----------------------|
| 1000 | | Always True | |
| 0111 | C | Carry | C = 1 |
| 1111 | NC | No Carry | C = 0 |
| 0110 | Z | Zero | Z = 1 |
| 1110 | NZ | Not Zero | Z = 0 |
| 1101 | PL | Plus | S = 0 |
| 0101 | MI | Minus | S = 1 |
| 0100 | OV | Overflow | V = 1 |
| 1100 | NOV | No Overflow | V = 0 |
| 0110 | EQ | Equal | Z = 1 |
| 1110 | NE | Not Equal | Z = 0 |
| 1001 | GE | Greater Than or Equal | (S XOR V) = 0 |
| 0001 | LT | Less than | (S XOR V) = 1 |
| 1010 | GT | Greater Than | [Z OR (S XOR V)] = 0 |
| 0010 | LE | Less Than or Equal | [Z OR (S XOR V)] = 1 |
| 1111 | UGE | Unsigned Greater Than or Equal | C = 0 |
| 0111 | ULT | Unsigned Less Than | C = 1 |
| 1011 | UGT | Unsigned Greater Than | (C = 0 AND Z = 0) = 1 |
| 0011 | ULE | Unsigned Less Than or Equal | (C OR Z) = 1 |
| 0000 | F | Never True (Always False) | |

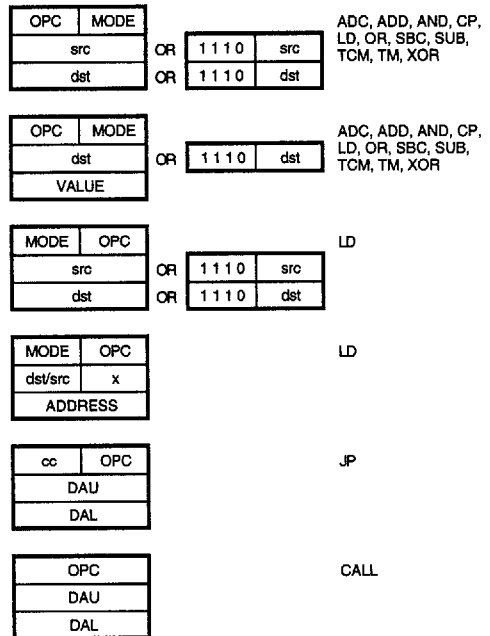
INSTRUCTION FORMATS



One-Byte Instructions



Two-Byte Instructions



Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "←". For example:

$$dst \leftarrow dst + src$$

indicates that the source data is added to the destination data and the result is stored in the destination location. The

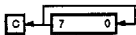
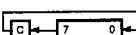
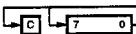
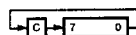
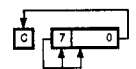
notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

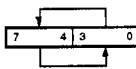
$$dst(7)$$

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

| Instruction and Operation | Address | | Opcode Byte (Hex) | Flags Affected | | | | | | |
|--|---|--|---|----------------|---|---|---|---|---|--|
| | Mode | dst src | | C | Z | S | V | D | H | |
| ADC dst, src dst←dst + src + C | † | | 1[] | * | * | * | * | 0 | * | |
| ADD dst, src dst←dst + src | † | | 0[] | * | * | * | * | 0 | * | |
| AND dst, src dst←dst AND src | † | | 5[] | - | * | * | 0 | - | - | |
| CALL dst SP←SP - 2 @SP←PC, PC←dst | DA IRR | | D6 D4 | - | - | - | - | - | - | |
| CCF C←NOT C | | | EF | * | - | - | - | - | - | |
| CLR dst dst←0 | R IR | | B0 B1 | - | - | - | - | - | - | |
| COM dst dst←NOT dst | R IR | | 60 61 | - | * | * | 0 | - | - | |
| CP dst, src dst - src | † | | A[] | * | * | * | * | - | - | |
| DA dst dst←DA dst | R IR | | 40 41 | * | * | * | X | - | - | |
| DEC dst dst←dst - 1 | R IR | | 00 01 | - | * | * | * | - | - | |
| DECW dst dst←dst - 1 | RR IR | | 80 81 | - | * | * | * | - | - | |
| DI IMR(7)←0 | | | 8F | - | - | - | - | - | - | |
| DJNZ r, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128 | RA | | rA r = 0 - F | - | - | - | - | - | - | |
| EI IMR(7)←1 | | | 9F | - | - | - | - | - | - | |
| HALT | | | 7F | - | - | - | - | - | - | |
| INC dst dst←dst + 1 | r R IR | | rE r = 0 - F 20 21 | - | * | * | * | - | - | |
| INCW dst dst←dst + 1 | RR IR | | A0 A1 | - | * | * | * | - | - | |
| IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1 | | | BF | * | * | * | * | * | * | |
| JP cc, dst if cc is true PC←dst | DA IRR | | cD c = 0 - F 30 | - | - | - | - | - | - | |
| JR cc, dst if cc is true, PC←PC + dst Range: +127, -128 | RA | | cB c = 0 - F | - | - | - | - | - | - | |
| LD dst, src dst←src | r r R r X r r R R R R IR IR | Im R r X r lr r R R R R IR IM R | rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5 | - | - | - | - | - | - | |
| LDC dst, src | r | lrr | C2 | - | - | - | - | - | - | |
| LDCI dst, src dst←src r←r + 1; rr←rr + 1 | lr | lrr | C3 | - | - | - | - | - | - | |

| Instruction and Operation | Address Mode | | Opcode Byte (Hex) | Flags Affected | | | | | | |
|--|--------------|-----|-------------------|----------------|---|---|---|---|---|---|
| | dst | src | | C | Z | S | V | D | H | |
| NOP | | | FF | - | - | - | - | - | - | - |
| OR dst, src dst←dst OR src | † | | 4[] | - | * | * | * | 0 | - | - |
| POP dst dst←@SP; SP←SP + 1 | R | | 50 | - | - | - | - | - | - | - |
| | IR | | 51 | | | | | | | |
| PUSH src SP←SP - 1; @SP←src | | R | 70 | - | - | - | - | - | - | - |
| | | IR | 71 | | | | | | | |
| RCF C←0 | | | CF | 0 | - | - | - | - | - | - |
| RET PC←@SP; SP←SP + 2 | | | AF | - | - | - | - | - | - | - |
| RL dst | R | | 90 | * | * | * | * | - | - | - |
| | IR | | 91 | | | | | | | |
|  | | | | | | | | | | |
| RLC dst | R | | 10 | * | * | * | * | - | - | - |
| | IR | | 11 | | | | | | | |
|  | | | | | | | | | | |
| RR dst | R | | E0 | * | * | * | * | - | - | - |
| | IR | | E1 | | | | | | | |
|  | | | | | | | | | | |
| RRC dst | R | | C0 | * | * | * | * | - | - | - |
| | IR | | C1 | | | | | | | |
|  | | | | | | | | | | |
| SBC dst, src dst←dst←src←C | † | | 3[] | * | * | * | * | 1 | * | * |
| SCF C←1 | | | DF | 1 | - | - | - | - | - | - |
| SRA dst | R | | D0 | * | * | * | 0 | - | - | - |
| | IR | | D1 | | | | | | | |
|  | | | | | | | | | | |
| SRP src RP←src | | Im | 31 | - | - | - | - | - | - | - |

| Instruction and Operation | Address Mode | | Opcode Byte (Hex) | Flags Affected | | | | | | |
|---|--------------|-----|-------------------|----------------|---|---|---|---|---|---|
| | dst | src | | C | Z | S | V | D | H | |
| STOP | | | 6F | - | - | - | - | - | - | - |
| SUB dst, src dst←dst←src | † | | 2[] | * | * | * | * | 1 | * | * |
| SWAP dst | R | | F0 | X | * | * | * | X | - | - |
| | IR | | F1 | | | | | | | |
|  | | | | | | | | | | |
| TCM dst, src (NOT dst) AND src | † | | 6[] | - | * | * | 0 | - | - | - |
| TM dst, src dst AND src | † | | 7[] | - | * | * | 0 | - | - | - |
| XOR dst, src dst←dst XOR src | † | | B[] | - | * | * | 0 | - | - | - |

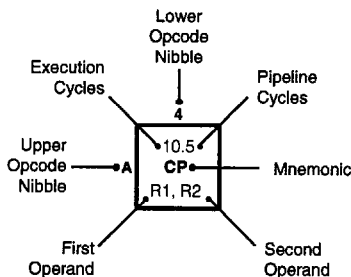
† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second opcode nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

| Address Mode | Lower Opcode Nibble | |
|--------------|---------------------|-----|
| dst | src | |
| r | r | [2] |
| r | Ir | [3] |
| R | R | [4] |
| R | IR | [5] |
| R | IM | [6] |
| IR | IM | [7] |

OPCODE MAP

| | | Lower Nibble (Hex) | | | | | | | | | | | | | | | |
|--------------------|---|-----------------------|------------------------|------------------------|--------------------------|-----------------------|------------------------|-----------------------|------------------------|---------------------|---------------------|---------------------------|-------------------------|---------------------|-------------------------|------------------|--------------|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| Upper Nibble (Hex) | 0 | 6.5 DEC R1 | 6.5 DEC IR1 | 6.5 ADD r1, r2 | 6.5 ADD r1, lr2 | 10.5 ADD R2, R1 | 10.5 ADD IR2, R1 | 10.5 ADD R1, IM | 10.5 ADD IR1, IM | 6.5 LD r1, R2 | 6.5 LD r2, R1 | 12/10.5 DJNZ r1, RA | 12/10.0 JR cc, RA | 6.5 LD r1, IM | 12/10.0 JP cc, DA | 6.5 INC r1 | |
| | 1 | 6.5 RLC R1 | 6.5 RLC IR1 | 6.5 ADC r1, r2 | 6.5 ADC r1, lr2 | 10.5 ADC R2, R1 | 10.5 ADC IR2, R1 | 10.5 ADC R1, IM | 10.5 ADC IR1, IM | | | | | | | | |
| | 2 | 6.5 INC R1 | 6.5 INC IR1 | 6.5 SUB r1, r2 | 6.5 SUB r1, lr2 | 10.5 SUB R2, R1 | 10.5 SUB IR2, R1 | 10.5 SUB R1, IM | 10.5 SUB IR1, IM | | | | | | | | |
| | 3 | 8.0 JP IRR1 | 6.1 SRP IM | 6.5 SBC r1, r2 | 6.5 SBC r1, lr2 | 10.5 SBC R2, R1 | 10.5 SBC IR2, R1 | 10.5 SBC R1, IM | 10.5 SBC IR1, IM | | | | | | | | |
| | 4 | 8.5 DA R1 | 8.5 DA IR1 | 6.5 OR r1, r2 | 6.5 OR r1, lr2 | 10.5 OR R2, R1 | 10.5 OR IR2, R1 | 10.5 OR R1, IM | 10.5 OR IR1, IM | | | | | | | | |
| | 5 | 10.5 POP R1 | 10.5 POP IR1 | 6.5 AND r1, r2 | 6.5 AND r1, lr2 | 10.5 AND R2, R1 | 10.5 AND IR2, R1 | 10.5 AND R1, IM | 10.5 AND IR1, IM | | | | | | | | |
| | 6 | 6.5 COM R1 | 6.5 COM IR1 | 6.5 TCM r1, r2 | 6.5 TCM r1, lr2 | 10.5 TCM R2, R1 | 10.5 TCM IR2, R1 | 10.5 TCM R1, IM | 10.5 TCM IR1, IM | | | | | | | | 6.0 STOP |
| | 7 | 10/12.1 PUSH R2 | 12/14.1 PUSH IR2 | 6.5 TM r1, r2 | 6.5 TM r1, lr2 | 10.5 TM R2, R1 | 10.5 TM IR2, R1 | 10.5 TM R1, IM | 10.5 TM IR1, IM | | | | | | | | 7.0 HALT |
| | 8 | 10.5 DECW RR1 | 10.5 DECW IR1 | 12.0 LDE r1, lr2 | 18.0 LDEI lr1, lr2 | | | | | | | | | | | | 6.1 DI |
| | 9 | 6.5 RL R1 | 6.5 RL IR1 | 12.0 LDE r2, lr1 | 18.0 LDEI lr2, lr1 | | | | | | | | | | | | 6.1 EI |
| | A | 10.5 INCW RR1 | 10.5 INCW IR1 | 6.5 CP r1, r2 | 6.5 CP r1, lr2 | 10.5 CP R2, R1 | 10.5 CP IR2, R1 | 10.5 CP R1, IM | 10.5 CP IR1, IM | | | | | | | | 14.0 RET |
| | B | 6.5 CLR R1 | 6.5 CLR IR1 | 6.5 XOR r1, r2 | 6.5 XOR r1, lr2 | 10.5 XOR R2, R1 | 10.5 XOR IR2, R1 | 10.5 XOR R1, IM | 10.5 XOR IR1, IM | | | | | | | | 16.0 IRET |
| | C | 6.5 RRC R1 | 6.5 RRC IR1 | 12.0 LDC r1, lr2 | 18.0 LDCI lr1, lr2 | | | | 10.5 LD r1.x, R2 | | | | | | | | 6.5 RCF |
| | D | 6.5 SRA R1 | 6.5 SRA IR1 | 12.0 LDC r1, lr2 | 18.0 LDCI lr1, lr2 | 20.0 CALL* IRR1 | | 20.0 CALL DA | 10.5 LD r2.x, R1 | | | | | | | | 6.5 SCF |
| | E | 6.5 RR R1 | 6.5 RR IR1 | | 6.5 LD r1, IR2 | 10.5 LD R2, R1 | 10.5 LD IR2, R1 | 10.5 LD R1, IM | 10.5 LD IR1, IM | | | | | | | | 6.5 CCF |
| | F | 8.5 SWAP R1 | 8.5 SWAP IR1 | | 6.5 LD lr1, r2 | | 10.5 LD R2, IR1 | | | | | | | | | | 6.0 NOP |



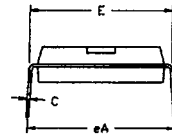
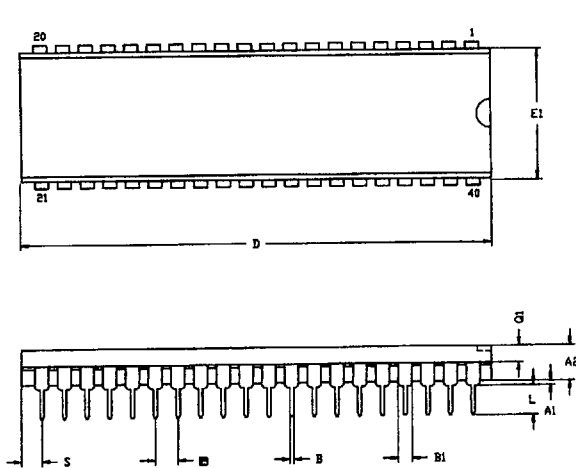
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand,
Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as
a 3-byte instruction

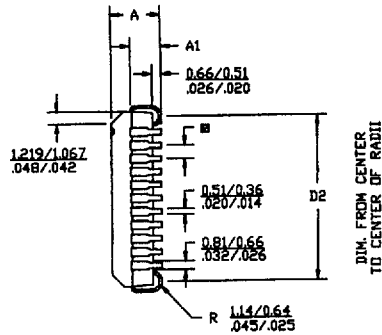
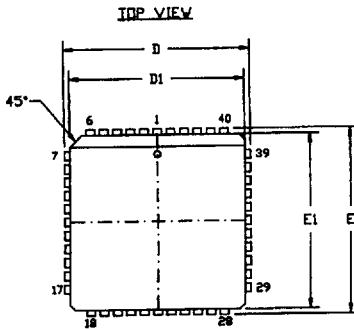
PACKAGE INFORMATION



| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|-------|-------|
| | MIN | MAX | MIN | MAX |
| A1 | 0.51 | 0.81 | .020 | .032 |
| A2 | 3.25 | 3.43 | .128 | .135 |
| B | 0.38 | 0.53 | .015 | .021 |
| B1 | 1.02 | 1.52 | .040 | .060 |
| C | 0.23 | 0.38 | .009 | .015 |
| D | 52.07 | 52.58 | 2.050 | 2.070 |
| E | 15.24 | 15.75 | .600 | .620 |
| E1 | 13.59 | 14.22 | .535 | .560 |
| ■ | 2.54 | TYP | .100 | TYP |
| eA | 15.49 | 16.51 | .610 | .650 |
| L | 3.18 | 3.81 | .125 | .150 |
| □ | 1.52 | 1.91 | .060 | .075 |
| S | 1.52 | 2.29 | .060 | .090 |

CONTROLLING DIMENSIONS : INCH

40-Pin DIP Package Diagram

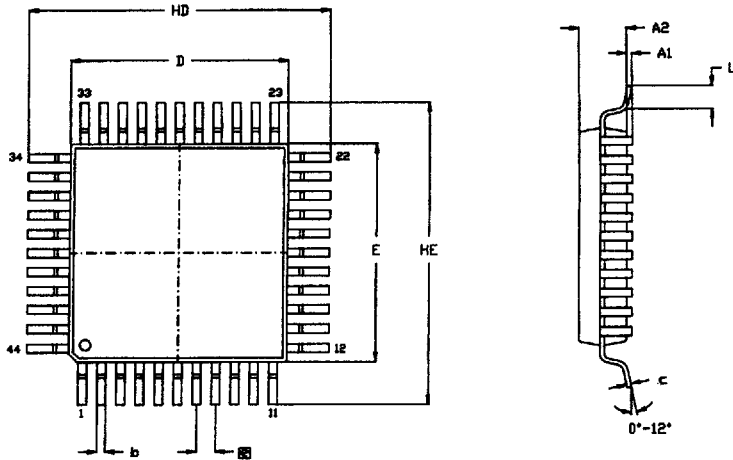

 DIM. FROM CENTER
 TO CENTER OF RADII

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : $\frac{MM}{INCH}$

| SYMBOL | MILLIMETER | | INCH | |
|--------|------------|-------|------|------|
| | MIN | MAX | MIN | MAX |
| A | 4.27 | 4.57 | .168 | .180 |
| A1 | 2.67 | 2.92 | .105 | .115 |
| D/E | 17.40 | 17.65 | .685 | .695 |
| D1/E1 | 16.51 | 16.66 | .650 | .656 |
| D2 | 15.24 | 16.00 | .600 | .630 |
| ■ | 1.27 | TYP | .050 | TYP |

44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)


NOTES:
 1. CONTROLLING DIMENSIONS : MILLIMETER
 2. LEAD COPLANARITY : MAX $\frac{.10 \text{ mm}}{.004}$

| SYMBOL | MILLIMETER | | INCH | |
|-----------|------------|-------|------|------|
| | MIN | MAX | MIN | MAX |
| A1 | 0.05 | 0.25 | .002 | .010 |
| A2 | 2.00 | 2.25 | .078 | .089 |
| b | 0.25 | 0.45 | .010 | .018 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 13.70 | 14.30 | .539 | .563 |
| D | 9.90 | 10.10 | .390 | .398 |
| HE | 13.70 | 14.30 | .539 | .563 |
| E | 9.90 | 10.10 | .390 | .398 |
| \square | 0.80 | TYP | .031 | TYP |
| L | 0.60 | 1.20 | .024 | .047 |

44-Pin QFP Package Diagram

ORDERING INFORMATION
Z86C91
12 MHz
40-pin DIP

Z86C9112PSC

Z86C9112PEC

44-pin PLCC

Z86C9112VSC

Z86C9112VEC

44-pin QFP

Z86C9112FSC

Z86C9112FEC

16 MHz
40-pin DIP

Z86C9116PSC

44-pin PLCC

Z86C9116VSC

44-pin QFP

Z86C9116FSC

20 MHz
40-pin DIP

Z86C9120PSC

44-pin PLCC

Z86C9120VSC

44-pin QFP

Z86C9120FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES
Preferred Package

P = Plastic DIP

V = Plastic Chip Carrier

Longer Lead Time

F = Plastic Quad Flat Pack

Preferred Temperature

S = 0°C to +70°C

Longer Lead Time

E = -40°C to +105°C

Speeds

12 = 12 MHz

16 = 16 MHz

20 = 20 MHz

Environmental

C = Plastic Standard

Example:
Z 86C91 12 P S C is a Z86C91, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow
