

OCTAL D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See "377" for clock enable version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability; standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSSTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the \overline{MR} input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n \overline{MR} to Q_n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15 15	15 20	ns ns
f_{max}	maximum clock frequency		66	36	MHz
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

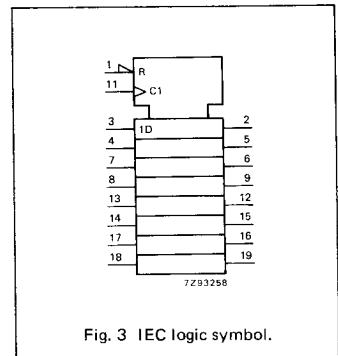
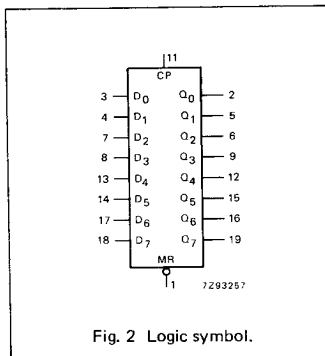
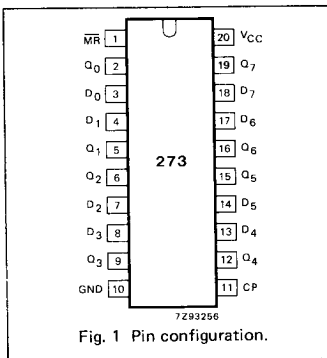
$$P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is $V_I = \text{GND to } V_{CC}$
 For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).
20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{MR}	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage



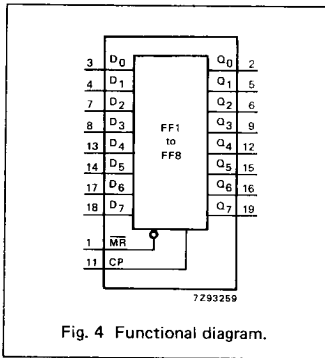


Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	\overline{MR}	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH transition
X = don't care

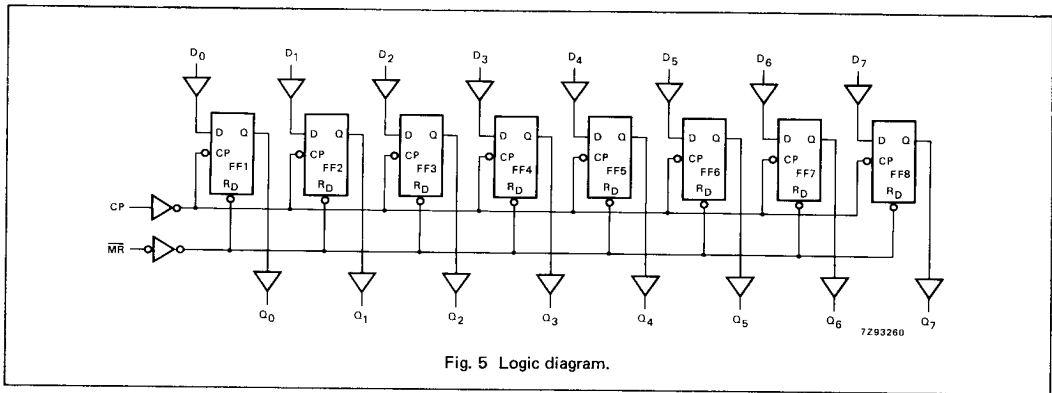


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		41 15 13	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig. 6
t _{PHL}	propagation delay MR to Q _n		44 16 14	150 30 26		185 37 31		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 15		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t _w	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t _w	master reset pulse width LOW	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t _{rem}	removal time MR to CP	50 10 9	-6 -2 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7
t _{su}	set-up time D _n to CP	60 12 10	11 4 3		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t _h	hold time D _n to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f _{max}	maximum clock pulse frequency	6.0 30 35	20.6 103 122		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

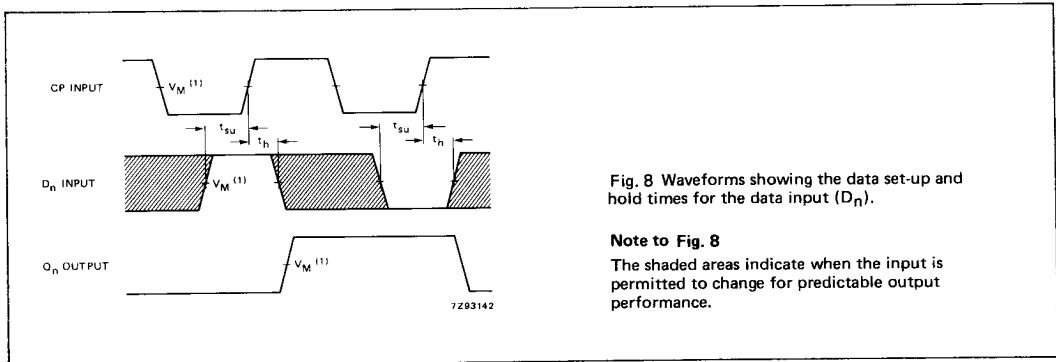
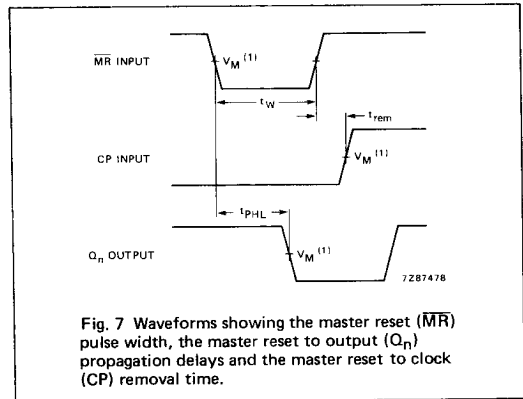
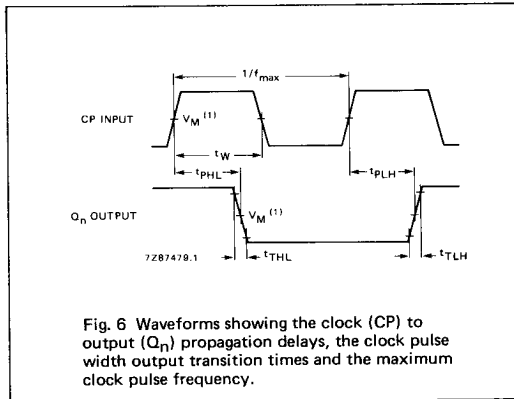
INPUT	UNIT LOAD COEFFICIENT
MR	1.00
CP	1.75
D _n	0.15

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		16	30		38		45	ns	4.5	Fig. 6	
t _{PHL}	propagation delay MR to Q _n		23	34		43		51	ns	4.5	Fig. 7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6	
t _W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig. 6	
t _W	master reset pulse width LOW	16	8		20		24		ns	4.5	Fig. 7	
t _{rem}	removal time MR to CP	10	-2		13		15		ns	4.5	Fig. 7	
t _{su}	set-up time D _n to CP	12	5		15		18		ns	4.5	Fig. 8	
t _h	hold time D _n to CP	3	-4		3		3		ns	4.5	Fig. 8	
f _{max}	maximum clock pulse frequency	30	56		24		20		MHz	4.5	Fig. 6	

AC WAVEFORMS



Note to Fig. 8
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3\text{V}$; $V_I = \text{GND to } 3\text{V}$.