SONY

CXP87500

CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

Description

The CXP87500 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87532/87540.
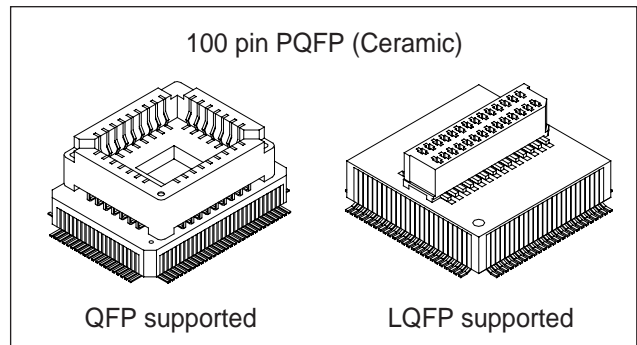
100 pin PQFP (Ceramic)

QFP supported   LQFP supported

Features

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/ boolean bit operation instructions
- Minimum instruction cycle   326ns at 12.288MHz operation
- Applicable EPROM   LCC type 27C512
  (Maximum 40Kbytes are available)
- Incorporated RAM capacity   1344bytes
- Peripheral functions
  - Arithmetic coprocessor   Signed multiplication and division, signed sum of products. high speed execution of many bits shift rotation operation
  - A/D converter   8-bit, 8-channel, successive approximation method
    (Conversion time of 13µs/12.288MHz)
    Incorporated 3-stage FIFO for A/D conversion data
  - Serial interface   Incorporated buffer RAM (auto transfer for 1 to 128bytes), 2-channel
  - Timer   8-bit timer
    8-bit timer/counter
    19-bit time base timer
  - High precision timing pattern generator   PPG 11-pin, 32-stage programmable
  - PWM output   12-bit, 2-channel (repetitive frequency 48kHz)
    8-bit, 3-channel (repetitive frequency 48kHz)
  - Servo input control   Capstan FG, drum FG/PG, reel FG input
  - FRC capture unit   Incorporated 28-bit and 8-stage FIFO
- Interruption   12 factors, 12 vectors, multi-interruption possible
- Standby mode   Sleep/stop
- Package   100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP87500. Refer to the Products List for details.
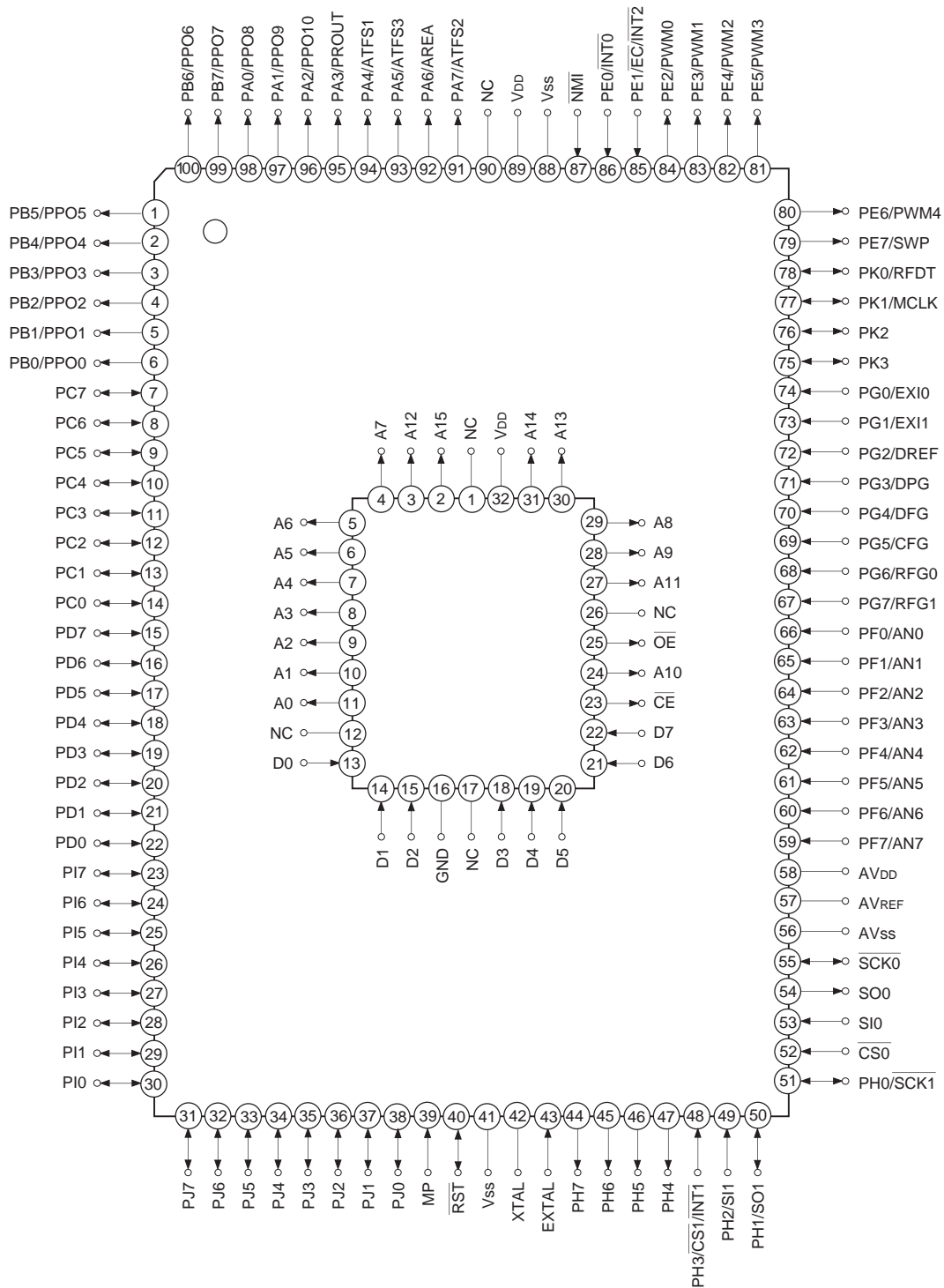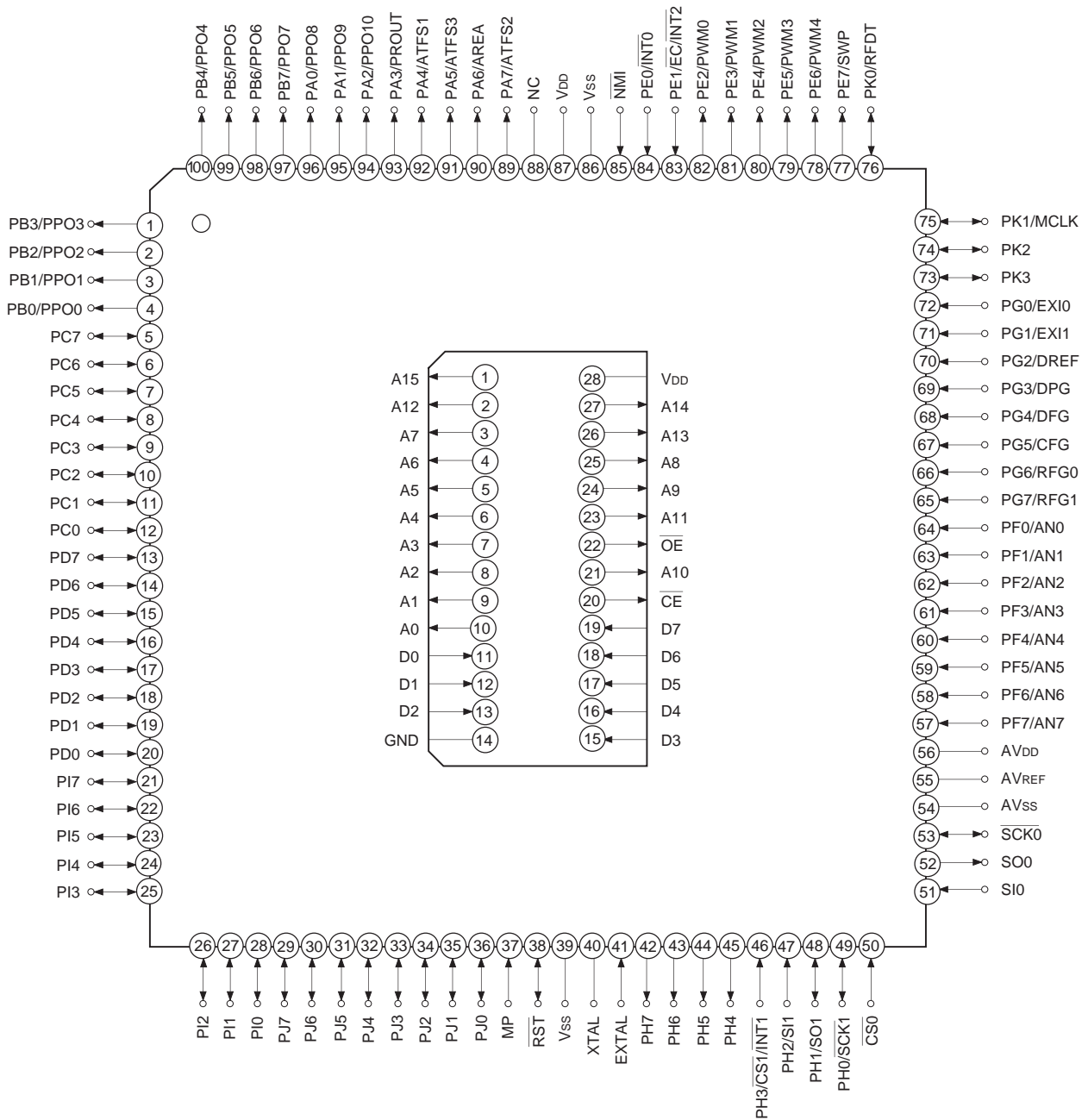
Structure

Silicon gate CMOS IC

E93X12B81-PS

Pin Assignment in Piggyback Mode (QFP package)

Top row (pins 100–81):
PB6/PPO6 (100), PB7/PPO7 (99), PA0/PPO8 (98), PA1/PPO9 (97), PA2/PPO10 (96), PA3/PROUT (95), PA4/ATFS1 (94), PA5/ATFS3 (93), PA6/AREA (92), PA7/ATFS2 (91), NC (90), V$_{DD}$ (89), V$_{SS}$ (88), $\overline{NMI}$ (87), PE0/INT0 (86), PE1/$\overline{EC}$/INT2 (85), PE2/PWM0 (84), PE3/PWM1 (83), PE4/PWM2 (82), PE5/PWM3 (81)

Left column (pins 1–30):
PB5/PPO5 (1)
PB4/PPO4 (2)
PB3/PPO3 (3)
PB2/PPO2 (4)
PB1/PPO1 (5)
PB0/PPO0 (6)
PC7 (7)
PC6 (8)
PC5 (9)
PC4 (10)
PC3 (11)
PC2 (12)
PC1 (13)
PC0 (14)
PD7 (15)
PD6 (16)
PD5 (17)
PD4 (18)
PD3 (19)
PD2 (20)
PD1 (21)
PD0 (22)
PI7 (23)
PI6 (24)
PI5 (25)
PI4 (26)
PI3 (27)
PI2 (28)
PI1 (29)
PI0 (30)

Right column (pins 80–51):
PE6/PWM4 (80)
PE7/SWP (79)
PK0/RFDT (78)
PK1/MCLK (77)
PK2 (76)
PK3 (75)
PG0/EXI0 (74)
PG1/EXI1 (73)
PG2/DREF (72)
PG3/DPG (71)
PG4/DFG (70)
PG5/CFG (69)
PG6/RFG0 (68)
PG7/RFG1 (67)
PF0/AN0 (66)
PF1/AN1 (65)
PF2/AN2 (64)
PF3/AN3 (63)
PF4/AN4 (62)
PF5/AN5 (61)
PF6/AN6 (60)
PF7/AN7 (59)
AV$_{DD}$ (58)
AV$_{REF}$ (57)
AV$_{SS}$ (56)
$\overline{SCK0}$ (55)
SO0 (54)
SI0 (53)
$\overline{CS0}$ (52)
PH0/SCK1 (51)

Bottom row (pins 31–50):
PJ7 (31), PJ6 (32), PJ5 (33), PJ4 (34), PJ3 (35), PJ2 (36), PJ1 (37), PJ0 (38), MP (39), $\overline{RST}$ (40), V$_{SS}$ (41), XTAL (42), EXTAL (43), PH7 (44), PH6 (45), PH5 (46), PH4 (47), PH3/$\overline{CS1}$/$\overline{INT1}$ (48), PH2/SI1 (49), PH1/SO1 (50)

Inner package (memory socket):
Top (pins 4–1, 32, 31, 30): A7 (4), A12 (3), A15 (2), NC (1), V$_{DD}$ (32), A14 (31), A13 (30)
Left (pins 5–13): A6 (5), A5 (6), A4 (7), A3 (8), A2 (9), A1 (10), A0 (11), NC (12), D0 (13)
Right (pins 29–21): A8 (29), A9 (28), A11 (27), NC (26), $\overline{OE}$ (25), A10 (24), $\overline{CE}$ (23), D7 (22), D6 (21)
Bottom (pins 14–20): D1 (14), D2 (15), GND (16), NC (17), D3 (18), D4 (19), D5 (20)

Note) 1. NC (Pin 90) is always connected to V$_{DD}$.

2. V$_{SS}$ (Pins 41 and 88) are both connected to GND.

3. MP (Pin 39) is always connected to GND.

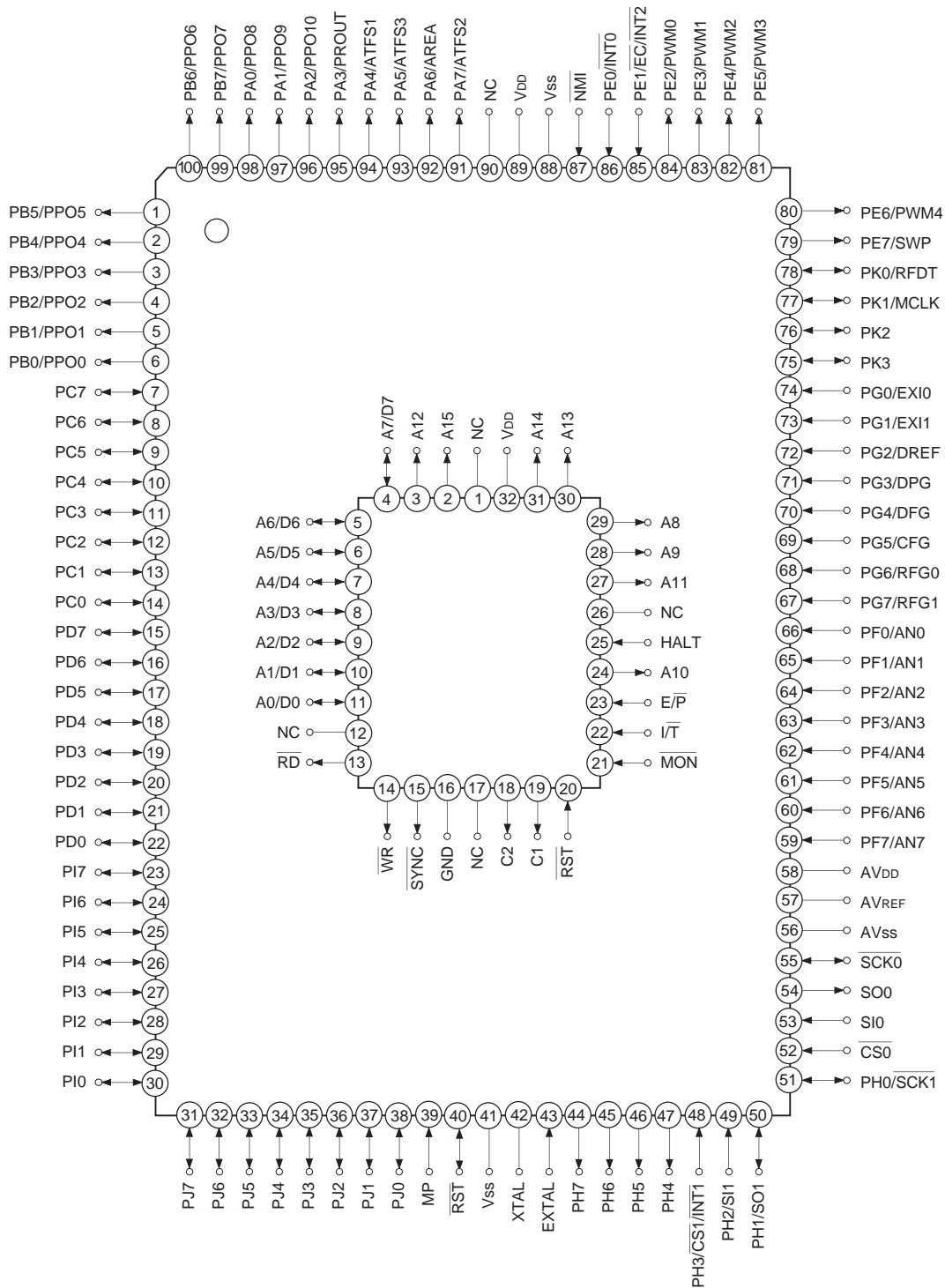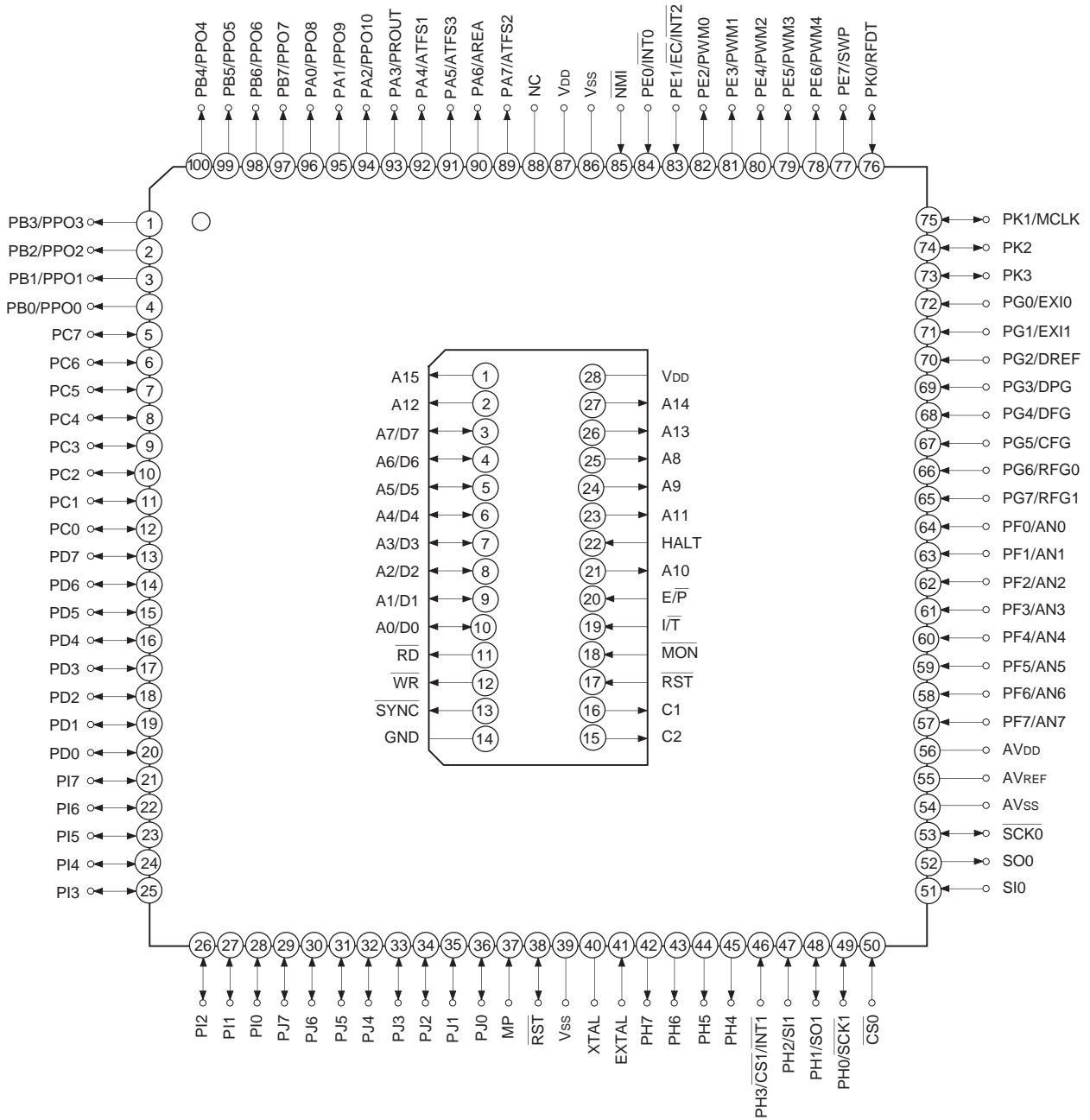## Pin Assignment in Piggyback Mode (LQFP package)

Note) 1. NC (Pin 88) is always connected to V_DD.

2. V_SS (Pins 39 and 86) are both connected to GND.

3. MP (Pin 37) is always connected to GND.

Pin Assignment in Evaluator Mode (QFP package)

Top edge (pins 100–81): PB6/PPO6, PB7/PPO7, PA0/PPO8, PA1/PPO9, PA2/PPO10, PA3/PROUT, PA4/ATFS1, PA5/ATFS3, PA6/AREA, PA7/ATFS2, NC, VDD, Vss, NMI, PE0/INT0, PE1/EC/INT2, PE2/PWM0, PE3/PWM1, PE4/PWM2, PE5/PWM3

Left edge (pins 1–30):
1 PB5/PPO5
2 PB4/PPO4
3 PB3/PPO3
4 PB2/PPO2
5 PB1/PPO1
6 PB0/PPO0
7 PC7
8 PC6
9 PC5
10 PC4
11 PC3
12 PC2
13 PC1
14 PC0
15 PD7
16 PD6
17 PD5
18 PD4
19 PD3
20 PD2
21 PD1
22 PD0
23 PI7
24 PI6
25 PI5
26 PI4
27 PI3
28 PI2
29 PI1
30 PI0

Right edge (pins 80–51):
80 PE6/PWM4
79 PE7/SWP
78 PK0/RFDT
77 PK1/MCLK
76 PK2
75 PK3
74 PG0/EXI0
73 PG1/EXI1
72 PG2/DREF
71 PG3/DPG
70 PG4/DFG
69 PG5/CFG
68 PG6/RFG0
67 PG7/RFG1
66 PF0/AN0
65 PF1/AN1
64 PF2/AN2
63 PF3/AN3
62 PF4/AN4
61 PF5/AN5
60 PF6/AN6
59 PF7/AN7
58 AVDD
57 AVREF
56 AVss
55 SCK0
54 SO0
53 SI0
52 CS0
51 PH0/SCK1

Bottom edge (pins 31–50): PJ7, PJ6, PJ5, PJ4, PJ3, PJ2, PJ1, PJ0, MP, RST, Vss, XTAL, EXTAL, PH7, PH6, PH5, PH4, PH3/CS1/INT1, PH2/SI1, PH1/SO1

Inner diagram:
Top (pins 4–30): A7/D7, A12, A15, NC, VDD, A14, A13
Inner left: 5 A6/D6, 6 A5/D5, 7 A4/D4, 8 A3/D3, 9 A2/D2, 10 A1/D1, 11 A0/D0, 12 NC, 13 RD
Inner right: 29 A8, 28 A9, 27 A11, 26 NC, 25 HALT, 24 A10, 23 E/P, 22 I/T, 21 MON
Inner bottom (14–20): WR, SYNC, GND, NC, C2, C1, RST

Note) 1. NC (Pin 90) is always connected to VDD.

2. Vss (Pins 41 and 88) are both connected to GND.

3. MP (Pin 39) is always connected to GND.

Pin Assignment in Evaluator Mode (LQFP package)

Top pins (100–76):
PB4/PPO4 (100), PB5/PPO5 (99), PB6/PPO6 (98), PB7/PPO7 (97), PA0/PPO8 (96), PA1/PPO9 (95), PA2/PPO10 (94), PA3/PROUT (93), PA4/ATFS1 (92), PA5/ATFS3 (91), PA6/AREA (90), PA7/ATFS2 (89), NC (88), VDD (87), VSS (86), NMI (85), PE0/INT0 (84), PE1/EC/INT2 (83), PE2/PWM0 (82), PE3/PWM1 (81), PE4/PWM2 (80), PE5/PWM3 (79), PE6/PWM4 (78), PE7/SWP (77), PK0/RFDT (76)

Left pins (1–25):
PB3/PPO3 (1), PB2/PPO2 (2), PB1/PPO1 (3), PB0/PPO0 (4), PC7 (5), PC6 (6), PC5 (7), PC4 (8), PC3 (9), PC2 (10), PC1 (11), PC0 (12), PD7 (13), PD6 (14), PD5 (15), PD4 (16), PD3 (17), PD2 (18), PD1 (19), PD0 (20), PI7 (21), PI6 (22), PI5 (23), PI4 (24), PI3 (25)

Right pins (75–51):
PK1/MCLK (75), PK2 (74), PK3 (73), PG0/EXI0 (72), PG1/EXI1 (71), PG2/DREF (70), PG3/DPG (69), PG4/DFG (68), PG5/CFG (67), PG6/RFG0 (66), PG7/RFG1 (65), PF0/AN0 (64), PF1/AN1 (63), PF2/AN2 (62), PF3/AN3 (61), PF4/AN4 (60), PF5/AN5 (59), PF6/AN6 (58), PF7/AN7 (57), AVDD (56), AVREF (55), AVSS (54), SCK0 (53), SO0 (52), SI0 (51)

Bottom pins (26–50):
PI2 (26), PI1 (27), PI0 (28), PJ7 (29), PJ6 (30), PJ5 (31), PJ4 (32), PJ3 (33), PJ2 (34), PJ1 (35), PJ0 (36), MP (37), RST (38), VSS (39), XTAL (40), EXTAL (41), PH7 (42), PH6 (43), PH5 (44), PH4 (45), PH3/CS1/INT1 (46), PH2/SI1 (47), PH1/SO1 (48), PH0/SCK1 (49), CS0 (50)

Inner chip, left pins (1–14):
A15 (1), A12 (2), A7/D7 (3), A6/D6 (4), A5/D5 (5), A4/D4 (6), A3/D3 (7), A2/D2 (8), A1/D1 (9), A0/D0 (10), RD (11), WR (12), SYNC (13), GND (14)

Inner chip, right pins (28–15):
VDD (28), A14 (27), A13 (26), A8 (25), A9 (24), A11 (23), HALT (22), A10 (21), E/P (20), I/T (19), MON (18), RST (17), C1 (16), C2 (15)

Note) 1. NC (Pin 88) is always connected to VDD.

2. VSS (Pins 39 and 86) are both connected to GND.

3. MP (Pin 37) is always connected to GND.

EPROM Read Timing

(Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns
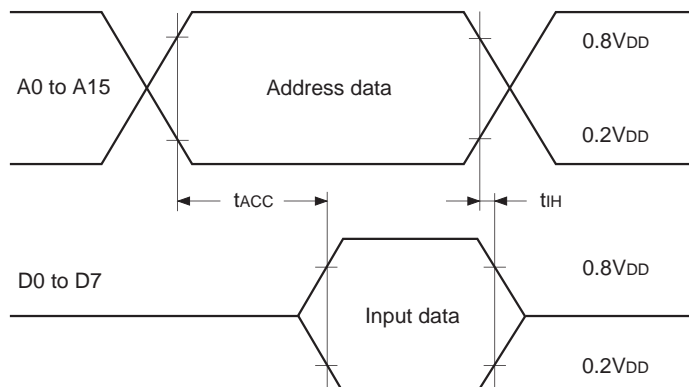
Products List

Optional item		Products		
		Mask		Piggyback/evaluator
		CXP87532	CXP87540	CXP87500-U01Q CXP87500-U01R
Package		100-pin plastic QFP/LQFP		100-pin ceramic PQFP
ROM capacity		32Kbytes	40Kbytes	EPROM 40Kbytes
Pull-up resistance for reset pin		Existent/Non-existent		Existent
Power on reset circuit		Existent/Non-existent		Existent
Input circuit format*1	PG0 to PG7, PK1	CMOS schmitt/TTLschmitt		TTL schmitt
	PK0	Buffer amplifier/Normal input		Buffer amplifier

*1 On PK1/MCLK pin and PG0/EXI0 to PG7/RFG1 pin, the input circuit format of CMOS schmitt or TTL schmitt can be selected to every pin.

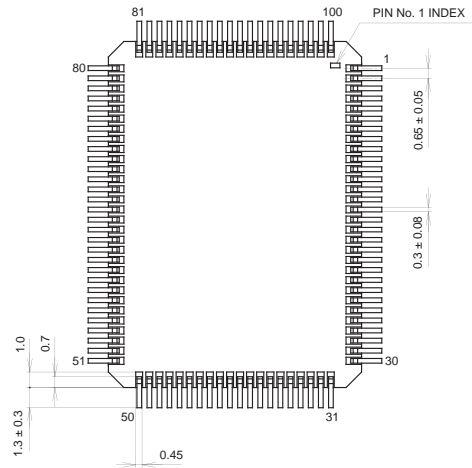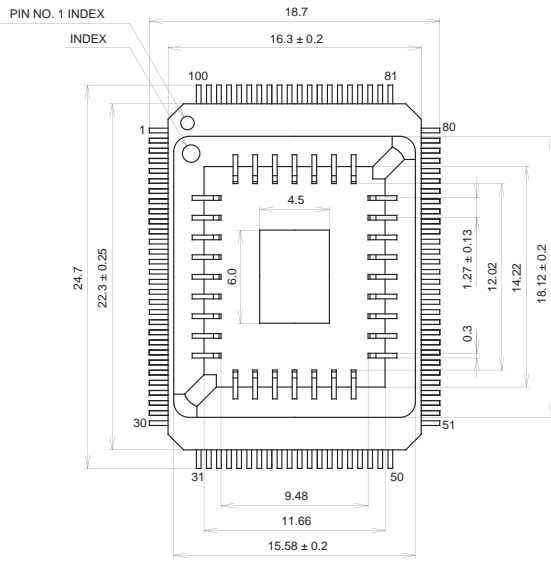On PK0/RFDT pin, buffer amplifier or normal input circuit format can be selected.

Piggyback mode/evaluator mode can be switched as shown below.

Piggyback mode

Piggyback/evaluator product

Evaluator mode

Pin 1 marking

LCC type EPROM
Pin 1 marking

Pin 1 index

Note)

CPU probe

Note) Evaluator cap should be
connected to CPU probe.

EPROM adaptor
Pin 1 marking

Pin 1 index

CPU probe for LQFP
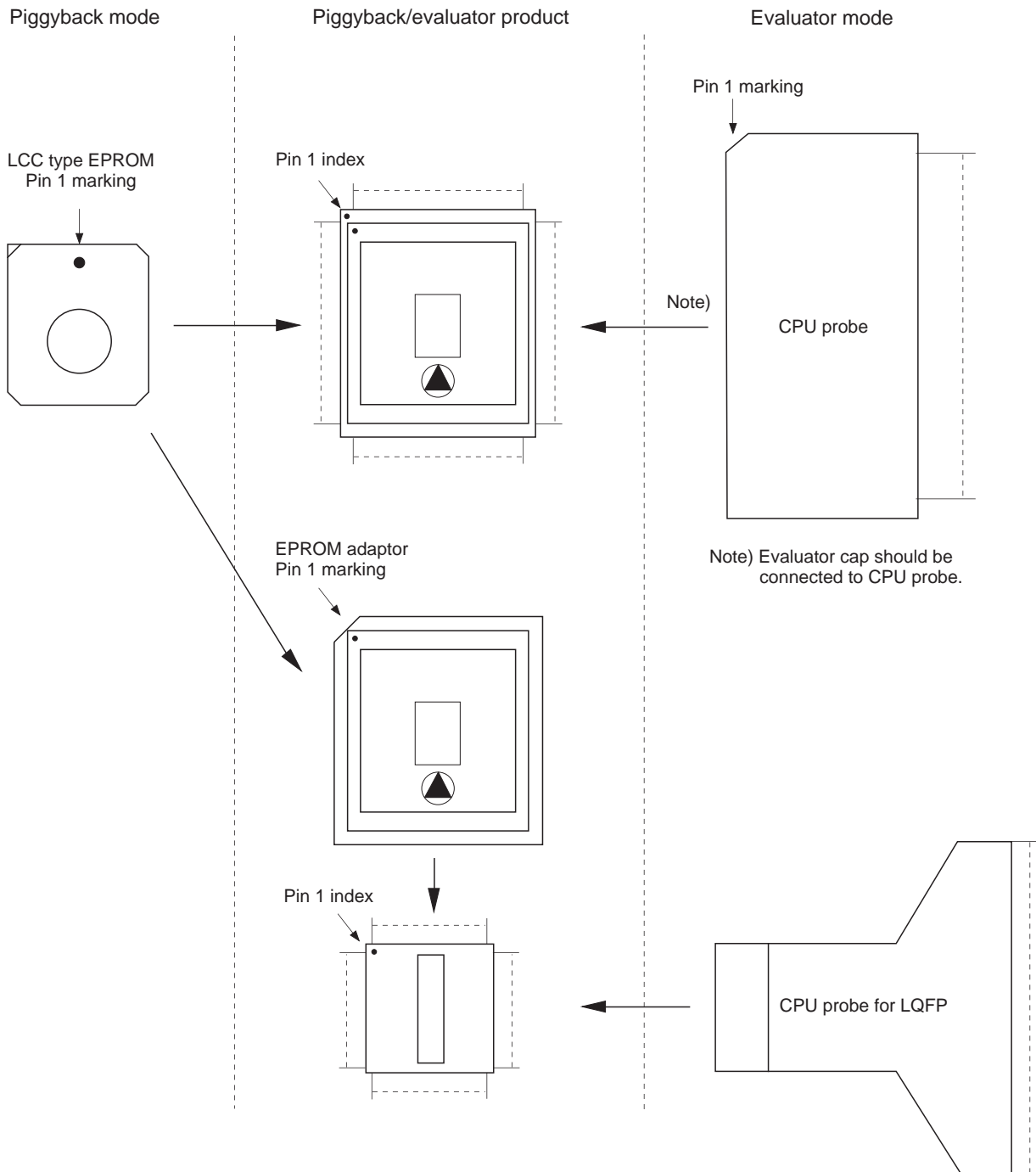
Package Outline   Unit: mm

100PIN PQFP (CERAMIC)
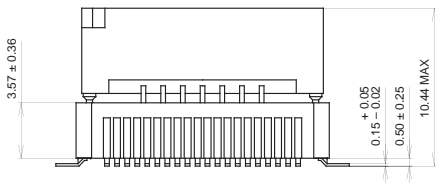
SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)
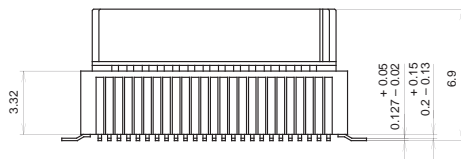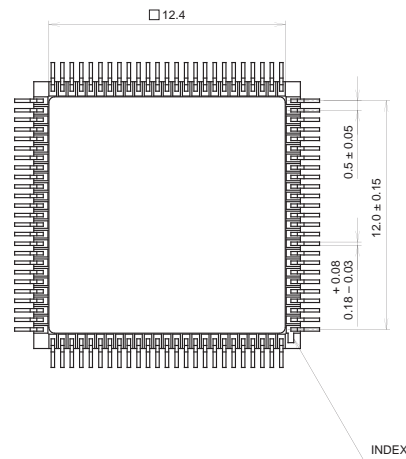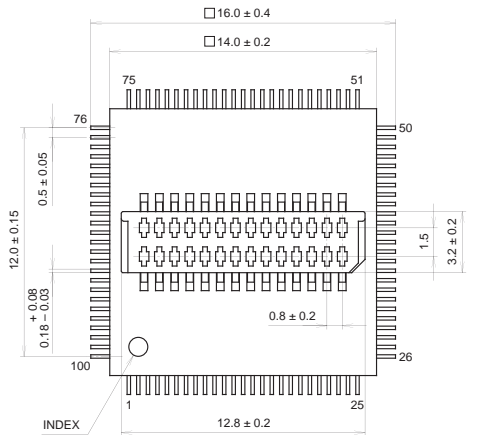
SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g