

Component input video switch with I²C BUS

Monolithic IC MM1519XQ

Outline

This IC is a color difference input video switch with I²C BUS control, developed for high resolution TV. With 3 output lines, it supports, among others, P-IN-P, monitor output and decoder output.

Features

1. Serial control by I²C BUS.
2. 4 color difference input lines, 3 output lines (3 input lines support D pin standards)
3. Built-in 6dB amp
4. Slave address can be changed: 94H or 96H
5. High band video SW supports D4 input (Y: 50MHz/P_B, P_R: 25MHz)
6. out 2 and out 3 have power save function.
7. 1 output line that can be controlled optionally by I²C BUS built-in.

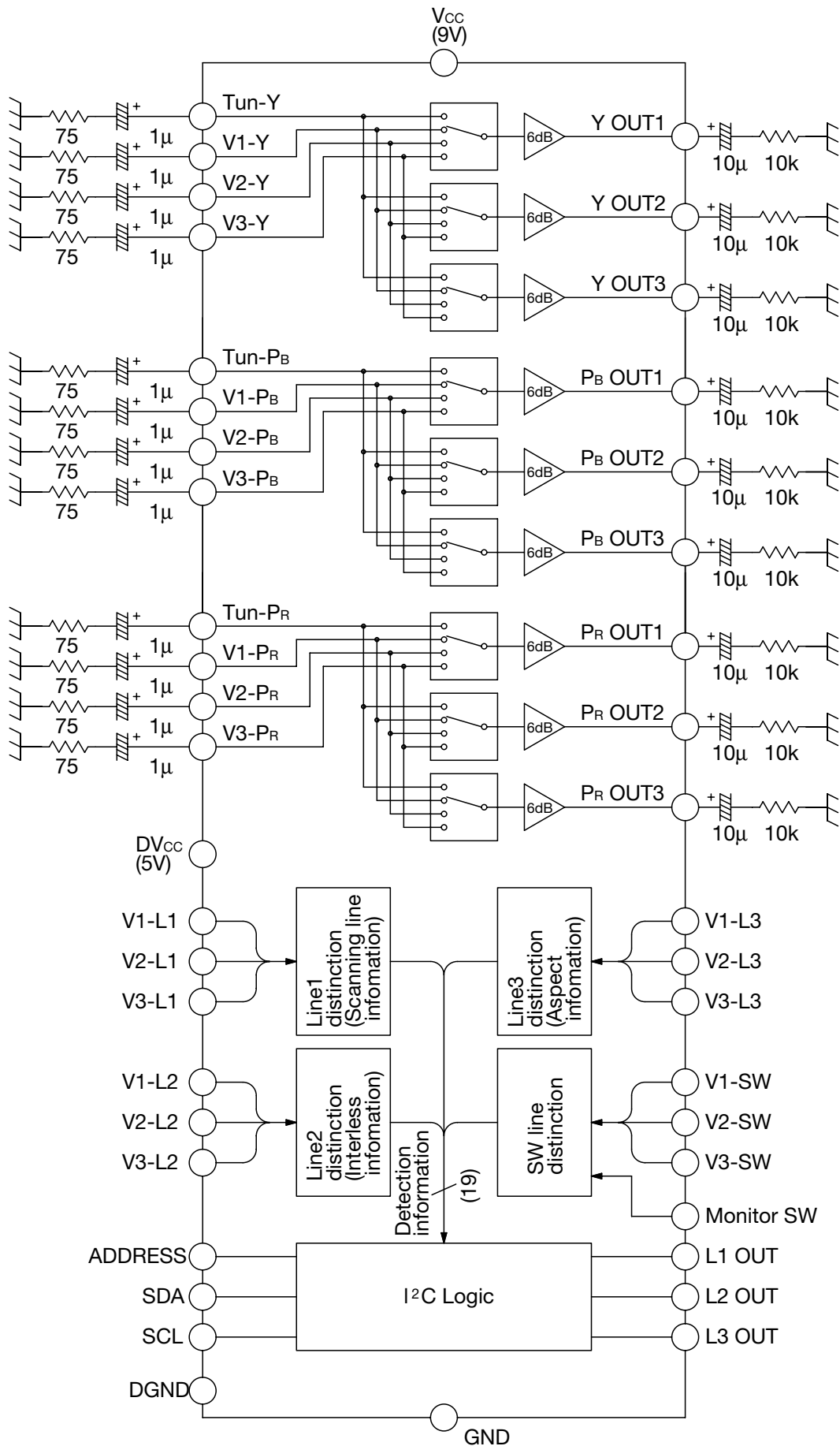
Package

QFP-64B

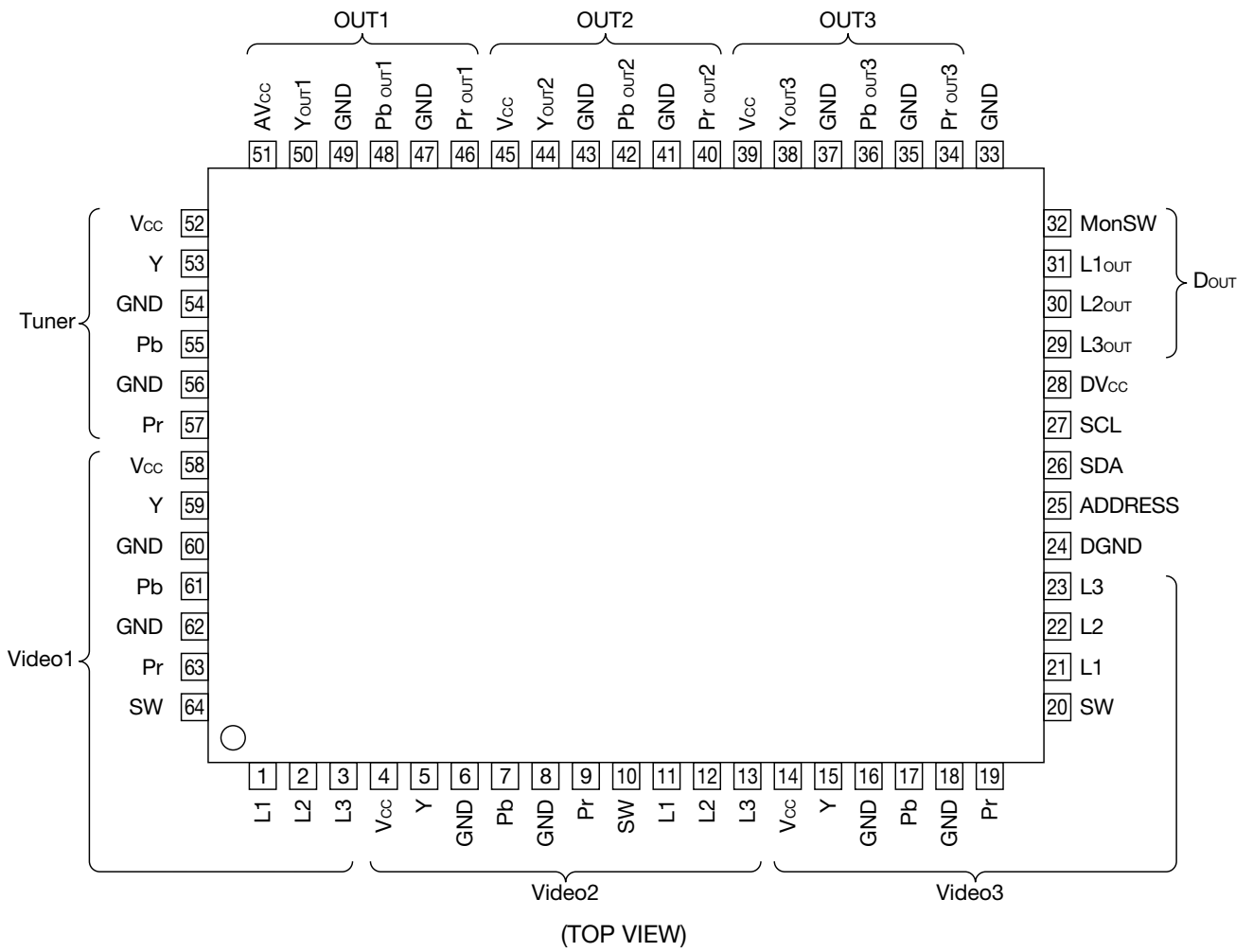
Applications

1. HDTV
 2. SDTV
 3. Other video equipment
-

Block Diagram



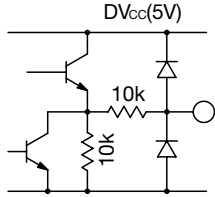
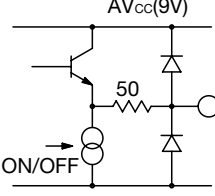
Pin Assignment



Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 2 3 11 12 13 21 22 23	Video1-L1 Video1-L2 Video1-L3 Video2-L1 Video2-L2 Video2-L3 Video3-L1 Video3-L2 Video3-L3	Line input of D-terminal	
4 14 39 45 51 52 58	Vcc AVcc	Analog Vcc	
5 15 53 59	Video2-Y Video3-Y Tuner-Y Video1-Y	Y input	
6 8 16 18 24 33 35 37 41 43 47 49 54 56 60 62	GND DGND	GND	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7 9 17 19 55 57 61 63	Video2-Pb Video2-Pr Video3-Pb Video3-Pr Tuner-Pb Tuner-Pr Video1-Pb Video1-Pr	Pb,Pr input	
10 20 32 64	Video2-SW Video3-SW MonSW Video1-SW	SW-Line of D terminal	
25	ADDRESS	Slave Address select pin	
26	SDA	Data input of I ² C BUS	
27	SCL	CLK input of I ² C BUS	

Pin No.	Pin name	Function	Internal equivalent circuit diagram
28	DVcc	Digital Vcc	
29 30 31	L3out L2out L1out	Line output for Monitor	
34 36 38 40 42 44 46 48 50	Pr out3 Pb out3 Y out3 Pr out2 Pb out2 Y out2 Pr out1 Pb out1 Y out1	Video output	

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Supply voltage	V _{CC max.}	13	V
Power dissipation	P _d	1300	mW

Recommended Operating Conditions

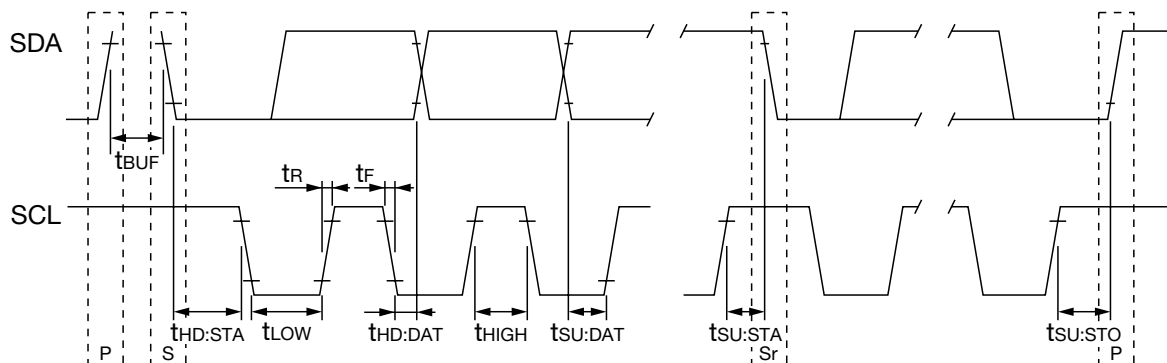
Item	Symbol	Ratings	Units
Operating temperature	T _{OPR}	-20~+75	°C
Operating voltage	V _{OP1}	+8.0~+10.0	V
Operating voltage	V _{OP2}	+4.5~+5.5	V

Electrical Characteristics (Except where noted therwise, Ta=25°C, V_{CC}=AV_{CC}=9V, DV_{CC}=5V)

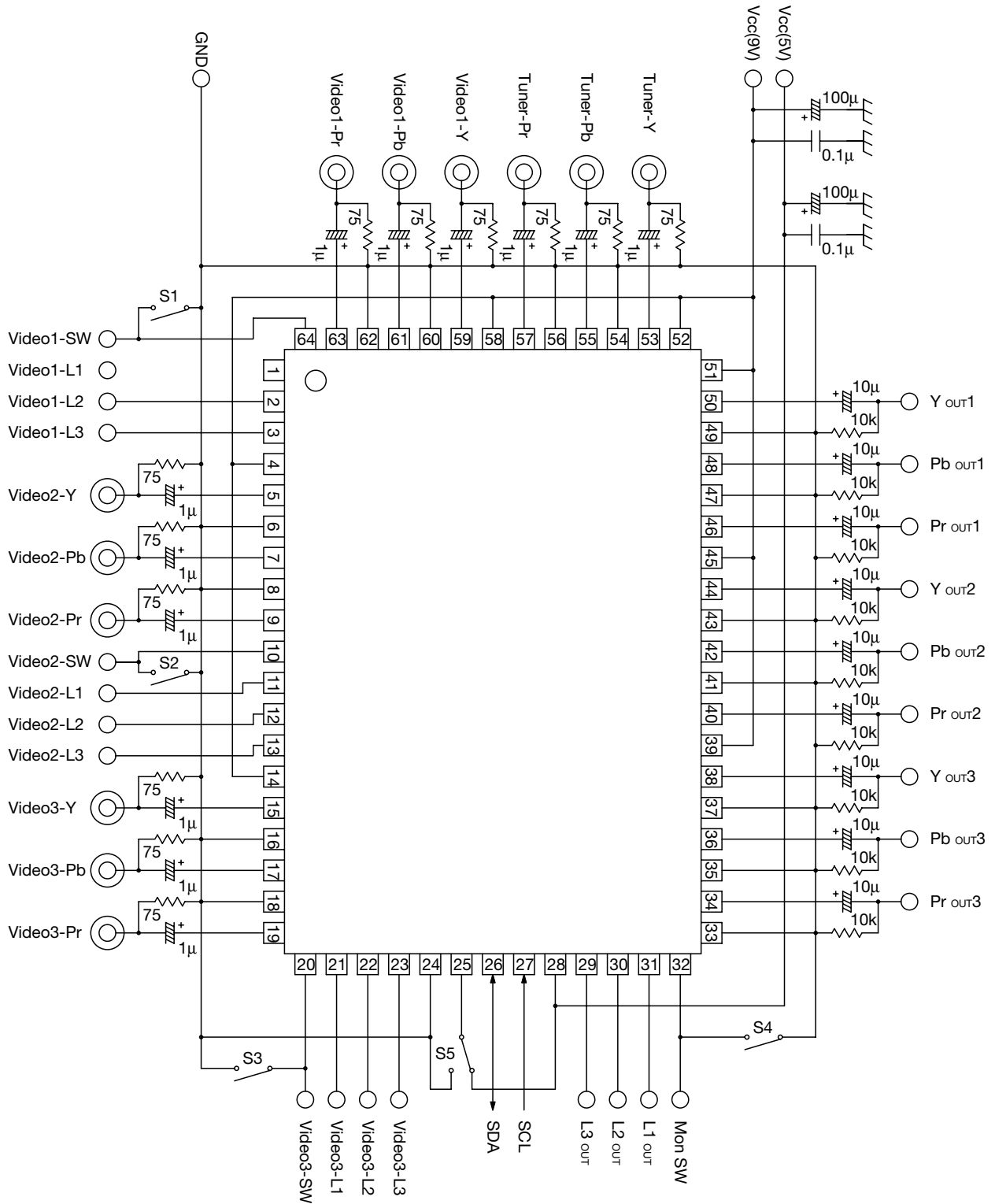
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[V_{CC} & AV_{CC}] (Analog V_{CC} [9V])						
Current consumption	I _{CC0}	No signal		67	87	mA
Current of power-save 1	I _{CC1}	Out2 is turn-off, Out1&3 are active		55	72	mA
Current of power-save 2	I _{CC2}	Out3 is turn-off, Out1&2 are active		55	72	mA
Current of power-save 3	I _{CC3}	Out2&3 are turn-off, Out1 is active		43	60	mA
[DV_{CC}] (Digital V_{CC} [5V])						
Current consumption	I _{CC4}	No signal		8	10	mA
[Terminal voltage]						
Y input terminal	V _{YIN}	53, 59, 5, 15 pin	4.8	5.2	5.6	V
Pb,Pr input terminal	V _{PIN}	55, 57, 61, 63, 7, 9, 17, 19 pin	4.5	4.9	5.3	V
Y output terminal	V _{YOUT}	50, 44, 38 pin	4.0	4.4	4.8	V
Pb, Pr output terminal	V _{POUT}	48, 46, 42, 40, 36, 34 pin	3.9	4.3	4.7	V
[D connecter conditions]						
Line1~3 detect level L	V _{detL}	1, 2, 3, 11, 12, 13, 21, 22, 23 pin	0.6	1.0	1.4	V
Line1~3 detect level H	V _{deth}	1, 2, 3, 11, 12, 13, 21, 22, 23 pin	2.4	2.9	3.4	V
Switch detect level L	V _{detL}	64, 10, 20, 32 pin			1.8	V
Switch detect level H	V _{deth}	64, 10, 20, 32 pin	3.5			V
Line output level L	V _{LL}				0.4	V
Line output level M	V _{LM}		1.4		2.4	V
Line output level H	V _{LH}		3.4			V
[Address terminal]						
Address threshold level	V _{thADR}		1.5	2.0	2.5	V
[Input terminal impedance]						
Y input	R _{YIN}		100	150	200	kΩ
Pb input	R _{PBIN}		100	150	200	kΩ
Pr input	R _{PBIN}		100	150	200	kΩ
[Y_{OUT1}]						
Voltage gain	G _{Y1}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 50MHz/100kHz	-3			dB
Input dynamic range	D _{Y1}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Y_{OUT2}]						
Voltage gain	G _{Y2}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 50MHz/100kHz	-3			dB
Input dynamic range	D _{Y2}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Y_{OUT3}]						
Voltage gain	G _{Y3}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 50MHz/100kHz	-3			dB
Input dynamic range	D _{Y3}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Pb out1]						
Voltage gain	G _{PB1}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PB1}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Pb out2]						
Voltage gain	G _{PB2}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PB2}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
[Pb out3]						
Voltage gain	G _{PB3}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PB3}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Pr out1]						
Voltage gain	G _{PR1}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PR1}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Pr out2]						
Voltage gain	G _{PR2}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PR2}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Pr out3]						
Voltage gain	G _{PR3}	SIN wave: 1V _{P-P} , 100kHz	5.5	6.0	6.5	dB
Frequency characteristic	f _{Y1}	SIN wave: 1V _{P-P} 25MHz/100kHz	-3			dB
Input dynamic range	D _{PR3}	SIN wave: 100kHz THD=1.0%	2.5	3.0		V _{P-P}
[Crosstalk]						
Y _{out1}	CT _{Y1L}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Y _{out2}	CT _{Y2L}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Y _{out3}	CT _{Y3L}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pb _{out1}	CT _{PB1}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pb _{out2}	CT _{PB2}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pb _{out3}	CT _{PB3}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pr _{out1}	CT _{PR1}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pr _{out2}	CT _{PR2}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
Pr _{out3}	CT _{PR3}	SIN wave: 1V _{P-P} , 5MHz		-65	-55	dB
[I²C condition]						
Input voltage L	V _{IL}		0		1.5	V
Input voltage H	V _{IH}		3.0		5.0	V
SDA low level output voltage	V _{OL}	SDA sink 3mA	0		0.4	V
High level input current	I _{IH}	SDA, SCL=4.5V	-10		10	μA
Low level input current	I _{IL}	SDA, SCL=0.4V	-10		10	μA
Clock frequency	f _{SCL}				100	kHz
Data transfer wait time	t _{BUF}		4.7			μs
SCL start hold time	t _{HD} ; STA		4.0			μs
SCL low level hold time	t _{LOW}		4.7			μs
SCL high level hold time	t _{HIGH}		4.0			μs
Start condition setup time	t _{SU} ; STA		4.7			μs
SDA data hold time	t _{HD} ; DAT		200			ns
SDA data setup time	t _{SU} ; DAT		250			ns
SDA, SCL rise time	t _R				1000	ns
SDA, SCL fall time	t _F				300	ns
Stop condition setup time	t _{SU} ; STO		4.0			μs

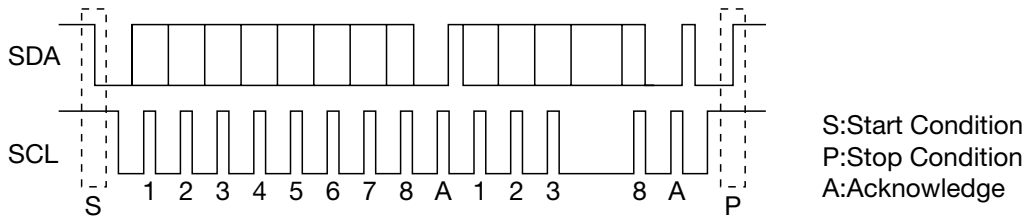
Note.1 I²C condition



Measuring Circuit



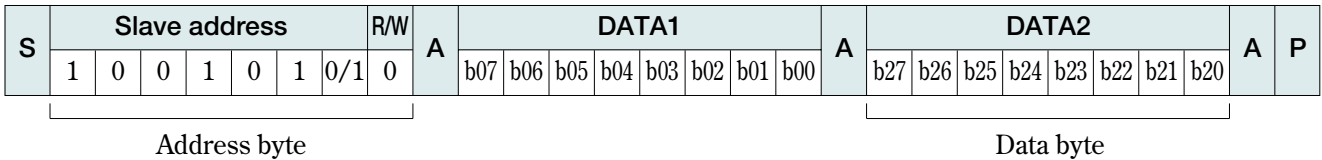
I²C BUS



I²C BUS is inter bus system controlled by 2 lines (SDA,SCL).
Data are transmitted and received in the units of byte and Acknowledge.
It is transmitted by MSB first from the Start conditions.

[Control registers]

Control registers are data sent from the master for determining the switch conditions.
The data format is set as shown in the following figure.



Out of the Address byte, first 7bit are assigned to the slave address,while the residual 1bit is assigned to the R/W bit.

Set the R/W bit to 0 when data are used control registers.

As MM1519 slave address, either 94H or 96H can be selected according to the ADR terminal conditions.

When ADR terminal is L,94H is selected.

The following figure indicates the control contents of control registers and switches.

Each bit of control registers is reset to 0,when power-on.

No.	DATA condition							
DATA1 [00H]	b07	b06	b05	b04	b03	b02	b01	b00
	Power save 2	Power save 3	Out1 select		Out2 select		Out3 select	
DATA2 [00H]	b17	b16	b15	b14	b13	b12	b11	b10
	Line1 output			Line2 output		Line3 output		
	1080	720	480	60p	60i	16 : 9	Letter Box	4 : 3

MM1519 consists of one address byte and two control data bytes (3bytes in total).

All data over the limited length (4th and subsequent bytes) are fully neglected.

For details of the control contents of switches, refer to the another table.

Switch Control Table

Out1 select

b05	b04	Y _{out1}	Pb _{out1}	Pr _{out1}
0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
0	1	Video1-Y	Video1-Pb	Video1-Pr
1	0	Video2-Y	Video2-Pb	Video2-Pr
1	1	Video3-Y	Video3-Pb	Video3-Pr

Out2 select

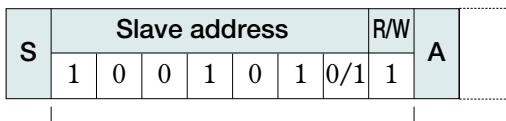
b07	b03	b02	Y _{out2}	Pb _{out2}	Pr _{out2}
0	0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
	0	1	Video1-Y	Video1-Pb	Video1-Pr
	1	0	Video2-Y	Video2-Pb	Video2-Pr
	1	1	Video3-Y	Video3-Pb	Video3-Pr
1			OFF	OFF	OFF

Out3 select

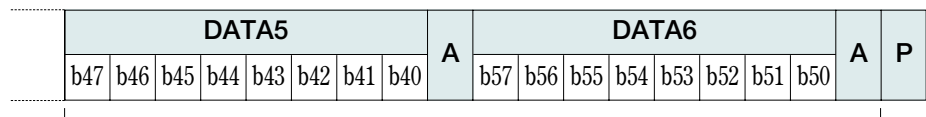
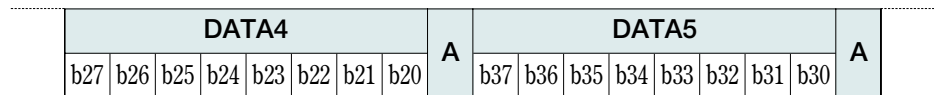
b06	b01	b00	Y _{out3}	Pb _{out3}	Pr _{out3}
0	0	0	Tuner-Y	Tuner-Pb	Tuner-Pr
	0	1	Video1-Y	Video1-Pb	Video1-Pr
	1	0	Video2-Y	Video2-Pb	Video2-Pr
	1	1	Video3-Y	Video3-Pb	Video3-Pr
1			OFF	OFF	OFF

[Status registers]

Status registers are data to inform the master of the device status. The data format is set as shown in the following figure.



Address byte



Status byte

Line1 output

b17	b16	b15	L1 _{out}
0	0	0	0V
0	0	1	0V
0	1	0	2.2V
0	1	1	0V
1	0	0	5V
1	0	1	0V
1	1	0	0V
1	1	1	0V

Line2 output

b14	b13	L2 _{out}
0	0	0V
0	1	0V
1	0	5V
1	1	0V

Line3 output

b12	b11	b10	L1 _{out}
0	0	0	0V
0	0	1	0V
0	1	0	2.2V
0	1	1	0V
1	0	0	5V
1	0	1	0V
1	1	0	0V
1	1	1	0V

Out of the Address byte, first 7bit are assigned to the slave address, while the residual 1bit is assigned to the R/W bit. Set the R/W bit to 1 when data are used status registers.

As MM1519 slave address, either 95H or 97H can be selected according to the ADR terminal conditions.

When ADR terminal is L,95H is selected.

Set the confirmation acknowledgement after the end of status register to non-ACK.

The following figure shows the correspondence of the output data of status registers.

No.	DATA condition							
	b27	b26	b25	b24	b23	b22	b21	b20
DATA3	Line1 (Out1)			Line2 (Out1)		Line3 (Out1)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA4	Line1 (Out2)			Line2 (Out2)		Line3 (Out2)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA5	Line1 (Out3)			Line2 (Out3)		Line3 (Out3)		
	1080	720	480	60p	60i	16:9	Letter Box	4 : 3
DATA6	b57	b56	b55	b54	b53	b52	b51	b50
					Switch line detect			
				Video1	Video2	Video3	Mon SW	

L1 voltage	Scanning line		
	1080	720	480
DC ≤ 0.8V	0	0	1
1.4V ≤ DC ≤ 2.4V	0	1	0
3.5V ≤ DC ≤ 5.0V	1	0	0

L2 voltage	I/P	
	60p	60i
DC ≤ 2.4V	0	1
3.5V ≤ DC ≤ 5.0V	1	0

L3 voltage	Aspect		
	16 : 9	Letter box	4 : 3
DC ≤ 0.8V	0	0	1
1.4V ≤ DC ≤ 2.4V	0	1	0
3.5V ≤ DC ≤ 5.0V	1	0	0

SW voltage	Switch line
DC ≤ 1.8V (connected)	0
3.2V ≤ DC (unconnected)	1

Application Circuit

