1. GENERAL

TC8801 is an ADM (Adaptive Delta Modulation) type voice synthesizing 1-chip CMOS LSI, with which low-voltage operation and low-power consumption can be realized. The circuit consists of a control unit, 256Kbit ROM storing voice data, voice synthesizing unit and a D / A converter. With a simple interface circuit and an audio circuit connected, the LSI is applicable to a variety of systems.

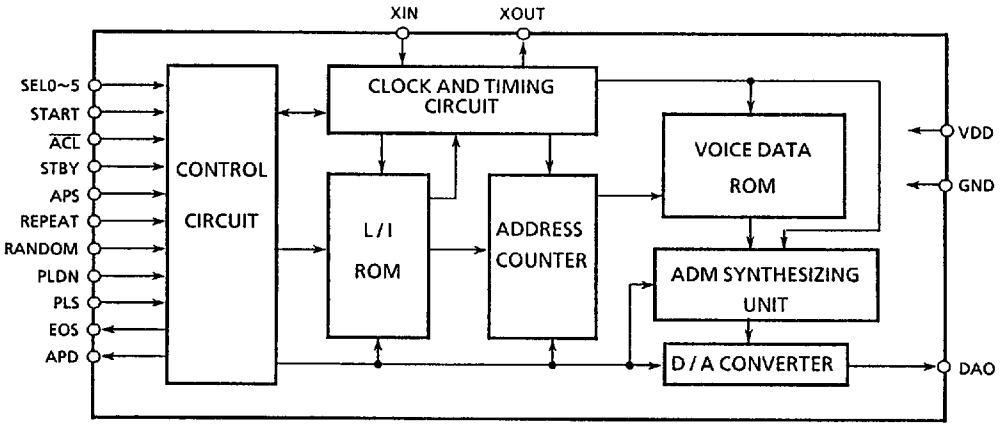
2. FEATURES

- ☐ A 256Kbit mask ROM is built-in for voice data.
- ☐ A maximum of 63 phrases is selectable.
- ☐ One out of four types of bit rates can be selected (32kbps, 22kbps, 16kbps, 11kbps).
- ☐ Speech time is 16 seconds (when a bit rate of 16kbps is selected).
- ☐ Repeat function ····· One phrase is talked repeatedly.
- ☐ Random function ····· One phrase is selected randomly from a maximum of 8 phrases, and talked.
- ☐ A built-in 10 bit D / A converter
- ☐ Low power consumption realized by stand-by function
  - ◦ Stand-by for inner circuit of TC8801
    1. Forced stand-by input at pin
    2. Automatic stand-by after speech
  - ◦ Stand-by for external circuit using APD signal
    1. APD (Audio Power Down) output is built in for turning on / off the switching regulator for external audio circuit.
- ☐ Low voltage operation ····· 2.4 – 5.5V
- ☐ Built-in ceramic oscillating circuit (oscillating frequency ····· 640kHz)
  Built-in RC oscillating circuit (oscillating frequency ····· 64kHz)
- ☐ Package ····· TC8801N : SDIP 28 pin
  TC8801F : SOP 28 pin

◦ The bit rate means the number of bits per second to be used

3. BLOCK DIAGRAM

3.1 TC8801 Block Diagram



3.2 Block Diagram Description

(1) Control circuit

Start of speech, repeated speech, random speech, stand-by, automatic power stand-by, etc are controlled.

(2) Clock and timing circuit

Various clocks and timing pulses for control are generated.

(3) L/I ROM (Label Index ROM)

This mask ROM sets the followings according to each phrase selected by SEL0 – SEL5.

① The start address and the end address of voice data ROM

② Bit rate

(4) Address counter

After the start address and the end address are set, the start address is incremented. Incrementing is stopped when counted up address reaches the end address.

(5) Voice data ROM

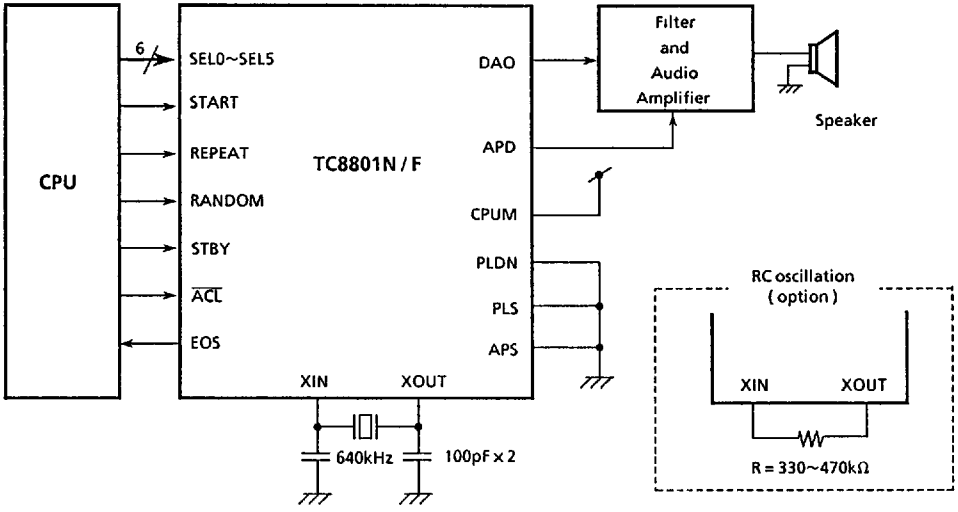
256Kbit ROM which stores the analyzed voice data.

(6) ADM synthesizing unit

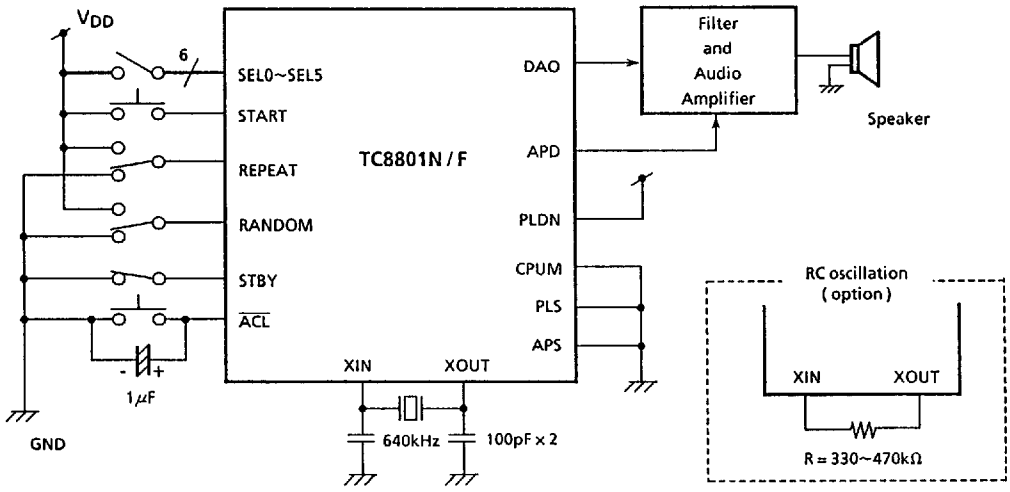
Analyzed voice data is synthesized to voice according to voice conditions.

3.3 Example of Voice System Configuration

3.3.1 CPU Control Type



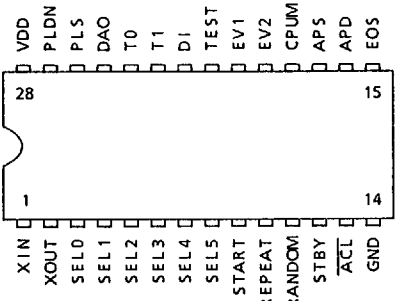
3.3.2 Manual Control Type



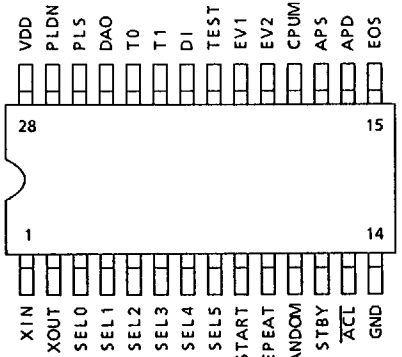
4. PIN DESCRIPTION

4.1 Pin Assignments

1) SDIP



2) SOP



4.2 Pin Descriptions

Name	No.	Structure				Functional explanation
		Manual Control		CPU Control		
		I/O	Pull-down / pull-up resistance	I/O	Pull-down / pull-up	
XIN	1	Input	–	Input	–	I/O pins for oscillating circuit. For ceramic oscillation, connect a ceramic resonator and capacitors to these pins. For RC oscillation, connect a resistor. For external clock, enter clock to XIN.
XOUT	2	Output	–	Output	–	
SEL0 SEL1 SEL2 SEL3 SEL4 SEL5	3 4 5 6 7 8	Input	Pull-down (For detail see 5.11.1)	Input	None	The pins for phrase select. A maximum of 63 phrases can be set. In Random speech, determine Qty. of speech phrases with SEL0 – SEL5. (See 5.10.2)
START	9	Input	Pull-down (For detail see 5.11.1)	Input	None	The pin for speech start input. Speech is begun by high level (manual control) or pulse (CPU control) at this pin.
REPEAT	10	Input	None	Input	None	The pin for repeat function. Repeat speech is begun by setting this pin high and giving speech start input. To end, reset repeat function or use the pin STBY or $\overline{ACL}$.
RANDOM	11	Input	None	Input	None	The pin for random function. Random speech is begun by setting this pin high determining Qty. of selected phrases by SEL0 – 5 and giving speech start input.
STBY	12	Input	Pull-up	Input	Pull-up	The pin for stand-by function. High level input to STBY stops oscillation and places TC8801 in stand-by mode. This PIN is ignored with APS PIN high.
$\overline{ACL}$	13	Input	Pull-up	Input	Pull-up	All clear input pin. With low level or pulse, the system is reset. However, oscillation continues. * Connect capacitor externally.
GND	14	Power supply	–	Power supply	–	The pin for power supply (negative voltage)

Name	No.	Structure				Functional explanation
		Manual Control		CPU Control		
		I/O	Pull-down / pull-up resistance	I/O	Pull-down / pull-up	
EOS	15	Output	–	Output	–	Output pin for End Of Speech. Outputting the status of speech or not. Low and high level is output after start and end of speech, respectively.
APD	16	Output	–	Output	–	Output pin for power down of external circuit. (Audio Power Down) Power down of external amplifier can be controlled. High is output in stand-by state.
APS	17	Input	None	Input	None	The pin for automatic power stand-by. Being set high, stand-by mode occurs automatically after the end of speech. Given with speech start input, speech begins.
CPUM	18	Input	None	Input	None	The pin for CPU / manual control select. ◦ CPU control with the CPUM high ◦ Manual control with the CPUM low
EV2 EV1 TEST	19 20 21	Input	Pull-down	Input	Pull-down	The pin for test circuit. Used normally open.
DI	22	Output	–	Output	–	Output pin for test circuit. Used normally open.
T1 T0	23 24	Output	–	Output	–	Output pin for test circuit. Used normally open.
DAO	25	Output	–	Output	–	Voice output pin. Output signal oscillates centering around VDD / 2.
PLS	26	Input	None	Input	None	Pin which controls the states of START, SEL0 – SEL5 pins in stand-by (Pull-down resistor or high-impedance) For details, see 5.11.1.
PLDN	27	Input	None	Input	None	Pin for assigning presence / absence of pull-down resistor as to SEL0 – SEL5, START in manual control.For details, see 5.11.1.
VDD	28	Power supply	–	Power supply	–	The pin for power supply (positive voltage)

5. SPECIFICATIONS

5.1 Voice Synthesizing Part

Synthesizing system	ADM system
D / A converter	10 bit voltage type
Bit rate	32k / 22k / 16k / 11kbps
Maximum number of phrases	63 phrases
Voice data capacity	256Kbit
Functions	◦ Automatic power stand-by function ◦ Audio power down function ◦ Repeat function ◦ Random function

5.2 Speech Time

Bit rate (kbps)	Speech time (sec)
32	8
22	12
16	16
11	24

Condition of f_{CLK} (clock frequency) = 640kHz (upon ceramic oscillation)
64kHz (upon RC oscillation)

5.3 Operations and Functions

5.3.1 Internal States

Internal states are the following three states.

- Speech state ····· Voice waveform is output from the DAO pin.
- Waiting state ····· Non-speech state in which the oscillation is continued while the circuit being reset to the initial status.
  The DAO pin is fixed at VDD/2.
- Stand-by state ····· Non-speech state in which the oscillation is stopped while resetting the circuit to the initial status. The DAO pin is fixed to the GND level.

Each state above can be monitored at the EOS (End of Speech) output and the APD (Audio Power Down) output. For the timings of EOS, APD pin signals, see 6.4. AC characteristics.

The three states and outputs of the TC8801 are shown in the following table.

Table 5.1 3 states and outputs of TC8801

	State of inner circuit	DAO voice output pin	EOS output pin level	APD output pin level
Speech state	◦ Operating state ◦ In oscillation	Voice waveform output	Low	Low
Waiting state	◦ Reset to initial status ◦ In oscillation	VDD/2 level	High	Low
Stand-by state	◦ Reset to initial status ◦ Oscillation stop	GND level	High	High

In addition, the TC8801 is provided with the $\overline{ACL}$ and STBY input pins for setting waiting or stand-by state. By setting the $\overline{ACL}$ low during speech, the TC8801 becomes waiting state, while becoming stand-by state by setting the STBY high during speech or waiting.
Transition between these state is as follows.

Note that, in the automatic power stand-by function(APS = H), the function of the $\overline{ACL}$ and STBY become different from those in this case.
For more details, see 5.9.2.

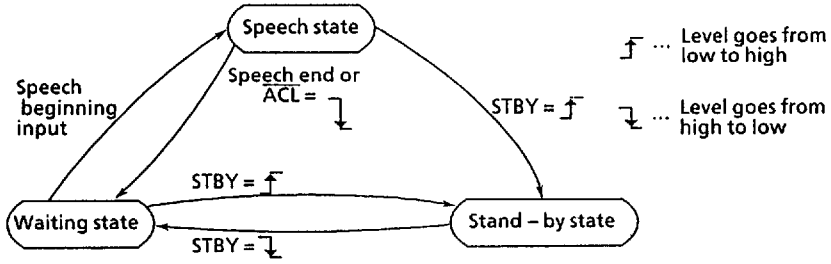


Fig. 5.1 State transition of TC8801 (APS = L)

5.4 Setting of Phrase

Set a speech phrase using the SEL0 – SEL5. However, TC8801 does not synthesize with all pins SEL0 – SEL5 set low. Therefore, a total number of selectable phrases with SEL0 – SEL5 is 63. Each phrase number corresponds to the setting of the pins SEL0 – SEL5 as shown in the following Table 5.2.

Table 5.2 Phrase no. vs. the SEL0 – SEL5 pin

Phrase No.	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮
62	1	1	1	1	1	0
63	1	1	1	1	1	1

1 = High level
0 = Low level

5.5 Speech Start Input

The method for operating the TC8801 is classified into the CPU control using microprocessor etc. and the manual control using switches. TC8801 is in CPU control mode with the CPUM high, and in the manual control mode with CPUM low. And there are two kinds of speech start inputs for each control mode.

Once a speech start input is given, voice waveform is output from the DAO, while the EOS changes from high to low.

5.5.1 Manual Control

(1) Speech start input – 1

Speech begins by setting the SEL0 – SEL5 and then setting START high. The START and the SEL0 - SEL5 are connected to a chattering preventing circuit in manual control. Therefore, after passing the chattering preventing time, the phrase number is read and the speech begins. (Fig. 5.2)(For details on the chattering preventing circuit, see 5.3.6)

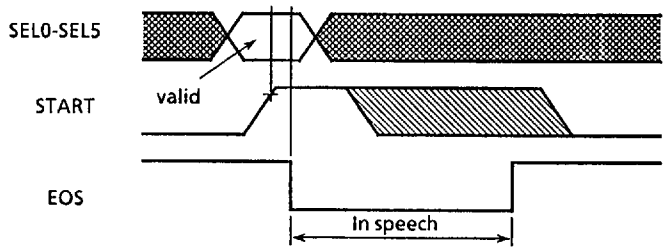


Fig. 5.2 Speech beginning input – 1 (manual control)

(2) Speech start input – 2

Speech is also begun by fixing the START pin to high level and all SEL0 - SEL5 pins to low level and then setting SEL0 - SEL5 pins to high level. When plural pins among SEL0 - SEL5 are set to high level, they must be changed to high level within chattering preventing time.

In the manual control, the START and SEL0 - SEL5 are connected to the chattering preventing circuit. Therefore, after passing the chattering preventing time, the phrase number is read and the speech begins. (Fig. 5.3) This method of speech beginning input is inhibited with the random function.

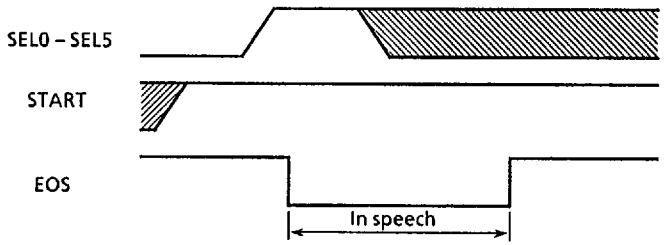


Fig. 5.3 Speech beginning input – 2 (manual control)

5.5.2 CPU Control

(1) Speech start input – 1

At the time of pulse rising of START pin, the phrase being set at the SEL0 - SEL5 pins is loaded to TC8801 and speech begins at the falling of START. (Fig.5.4)

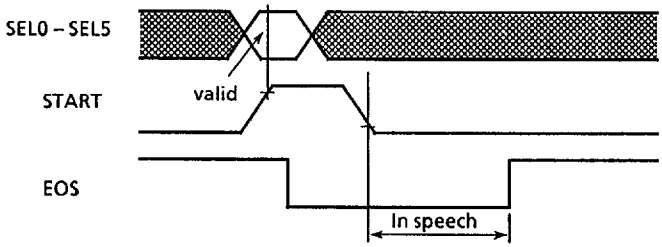


Fig.5.4 Speech beginning input – 1 (CPU control)

(2) Speech start input – 2

At first, fix the START pin to high level, all SEL0 - SEL5 pins to low level. And then, after inputting the pulse to one of SEL0 - SEL5, the setting of the phrase at SEL0 - SEL5 is read at the pulse rise time and speech begins at the pulse falling time. (Fig.5.5) Therefore, the maximum number of selectable phrases is six.

This method of speech beginning input is inhibited with the random function.

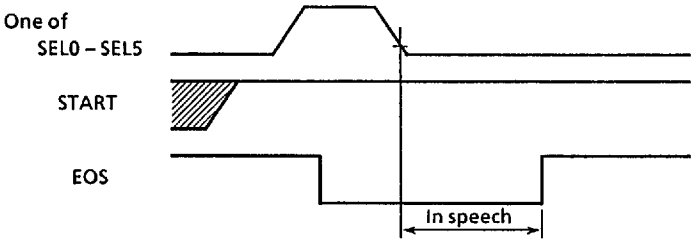


Fig.5.5 Speech beginning input – 2 (CPU control)

5.6 End of Speech

During speech, the EOS pin outputs low level, and changes to high level upon completion of speech. Speech is forcefully terminated during speech by any of the following three methods.

The EOS becomes high even after forced terminating of speech.

(1) The case of using the $\overline{ACL}$

The $\overline{ACL}$ pin is provided for initializing. Speech is forcefully terminated by setting the $\overline{ACL}$ low. (See 6.4, AC characteristics) After termination of speech, the TC8801 becomes waiting or stand-by state according to low or high level at the APS pin, respectively.

(2) The case of using the STBY

Speech is forcefully terminated by setting the STBY high when the APS is set low After termination, the TC8801 becomes stand-by state.

(3) The case of changing speech phrase

In this case, a phrase without voice data (the terminating phrase : the phrase of which the start and the end addresses are the same in L / I ROM) is first set up upon development of the mask ROM. Then a speech is terminated when assigning this phrase during the speech and giving the speech start input during the speech. (For the case of changing a phrase during speech, see next section 5.7)

5.7 Change of Speech Phrase during Speech

5.7.1 Method by Speech Beginning Input – 1

A new phrase b is assigned during speech of phrase a by the SEL0 - SEL5. Next, the talked phrase a is terminated and speech of the new phrase b begins by inputting high level or a pulse to the START in the manual or the CPU control, respectively. The relationship among the previous, new phrases and external input is shown in Fig.5.6.

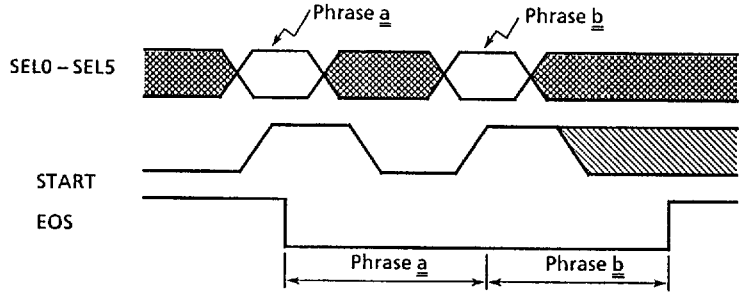


Fig.5.6 Changeover of speech phrase by speech beginning input – 1 (manual control)

5.7.2 Method by Speech Beginning Input – 2

All SEL0 - SEL5 pins are first set to L level during speech and then the START is set high. (Where START is already high, it is maintained high.) The high level or a pulse is given to one of SEL0 - SEL5 in the manual or the CPU control, respectively. Thereby the talked phrase is terminated and the new phrase speech begins. The relationship among the previous, new phrases and external input becomes as shown in Fig.5.7.

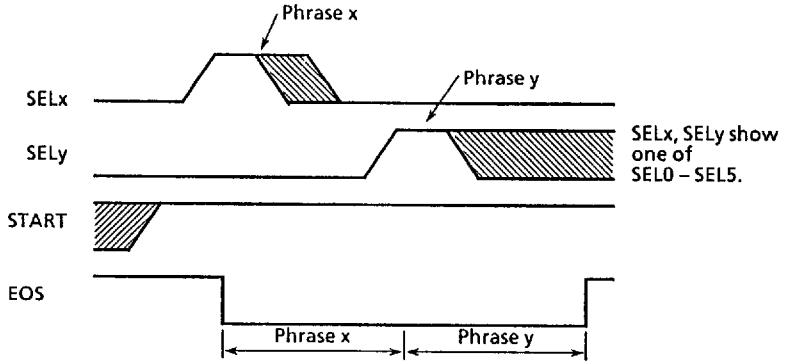
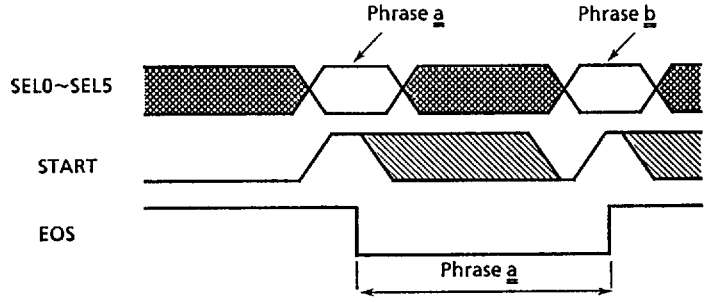


Fig.5.7 Changeover of speech phrase by speech beginning instruction – 2 (manual control)

5.7.3 Forced Termination of Speech

Speech is forcefully terminated, as described in 5.6 by change to the phrase of which the start and the end addresses are the same (the terminating phrase) in the data ROM. At that time, the timing is as follows.



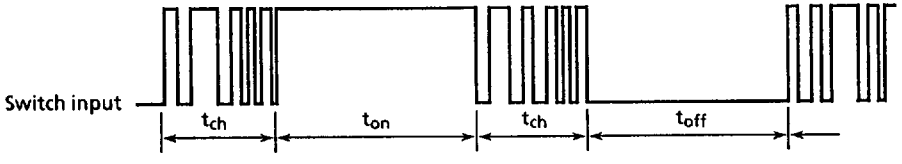
Phrase b ··· Phrase of which the start and the end addresses of voice data are the same.

Fig.5.8 Termination of speech by forced changing phrase (manual control)

5.8 Chattering Preventing Circuit

The chattering preventing circuit is available at the START and SEL0 - SEL5, during the manual control. It prevents error operation due to chattering by switches connected to the START and the SEL0 - SEL5.

Speech is begun provided high level is maintained stably at about 32 ms after chattering. Before the switch is once turned off and then again on, apply low level stably for 32 ms or more.



t_{ch}	Chattering time	(32 ms or less)
t_{on}	Switch ON time	(32 ms or above)
t_{off}	Switch OFF time	(32 ms or above)

f_{CLK} = 640kHz (ceramic oscillation)
64kHz (RC oscillation)

Fig.5.9 Chattering

5.9 Stand-by Function

The TC8801 is provided with the stand-by function to decrease current consumption.

Transition to the stand-by state is activated by using the STBY or the APS. In addition, the APD pin is also useful when turning on / off the power supply to an external circuit (audio circuit such as Amplifier and Filter).

The stand-by state can be assigned in any of the CPU or manual control.

5.9.1 The Stand-by State

1. Oscillation is stopped.
2. High level is output to the EOS and APD.
3. The DAO is fixed to low. (The DAO oscillates centering around VDD / 2 as the Voice Output pin in a state other than stand-by.)
4. The internal circuit is reset to the initial state.
5. SEL0 - SEL5 and START become open.(refer to 5.11)

5.9.2 The STBY, APS, APD pins and Stand-by State

1. Stand-by state by STBY pin

   TC8801 becomes stand-by state by setting the STBY high, when the APS is low. In the stand-by state using the STBY, synthesis is not begun by any speech start input.

2. Stand-by state by APS (automatic power stand-by state)

   By fixing the APS to high, the internal circuit is automatically placed in the stand-by state when speech is finished. Speech is forcefully terminated by setting the $\overline{ACL}$ low during speech, resulting is stand-by state.

   The STBY pin must be fixed high or open in this case to prevent current of pull up resistors of STBY pin. The automatic power stand-by function is disabled provided the START is high and at least one of the SEL0 – SEL5 is high.

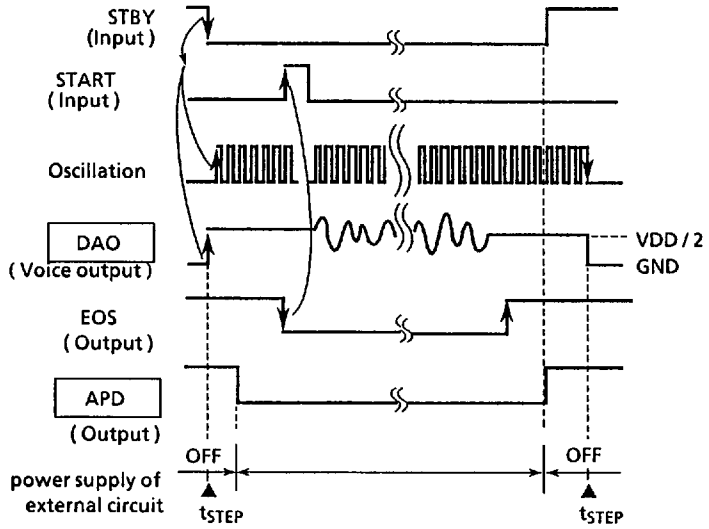
3. Stand-by state of the external circuit using APD Output pin

When TC8801 goes to the stand-by state, the APD (output) goes from low to high. Therefore, by using this pin signal, the stand-by (power down) for the external circuit is automatically effected during non-speech period.

Fig.5.10 show the relationships between stand-by state by the STBY input and the APD output when the APS pin is low, and those when the APS is high. (For more details, see the AC characteristics.)

Referring to Fig.5.10, time when the output level of the DAO changes is not the same as that of the APD pin. Now assume the power supply to the external circuit is turned off with the APD output high. Then, the power supply connected to external audio circuit is in off state when the level of the DAO Voice Output pin changes between 1/2 V_{DD} and GND (at t_{step} in the figure). Therefore, noise due to the change of output level at the DAO is reduced.

(1) APS = low level



(2) APS = high level

STBY ····· Invalid

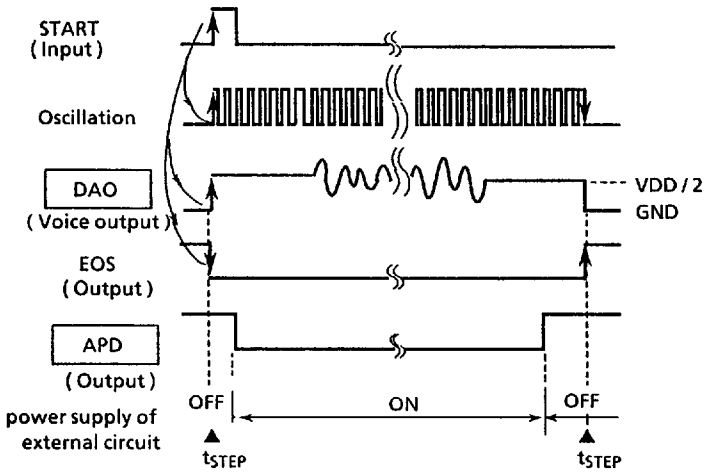


Fig.5.10 Stand-by state and APD output (CPU control)

5.10 Other Functions

5.10.1 Repeat Function

In manual control, an assigned phrase is repeatedly synthesized by setting the REPEAT high and giving speech start input -1 or -2. In the CPU control, speech is begun by speech start input -1 only. (Speech start input -2 is inhibited.)

Repeat speech is terminated by the STBY (STBY = high), the $\overline{ACL}$($\overline{ACL}$ = low), or resetting of the repeat function (REPEAT = low). With the STBY or $\overline{ACL}$ used for termination, the speech is terminated when it is effected. On the other hand, with the repeat function resetting used for resetting, the phrase in speech upon resetting is synthesized to the end of the phrase then terminated.

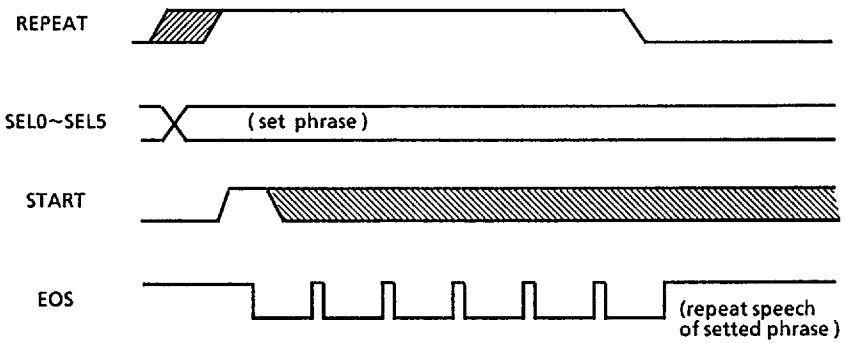


Fig.5.11 Repeat function (manual control)

When a phrase is changed during operation of the repeat mode, the phrase before the change is talked to its end, then the speech of a newly set phrase is begun. When a new speech start input -1 or -2 is given upon changing the phrase, the new phrase is talked at the input. (Fig.5.12)

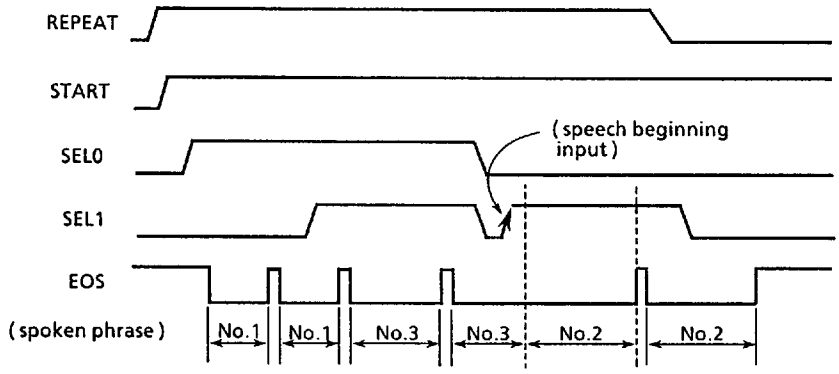


Fig.5.12 Change of phrase on repeat function (manual control)

The repeat function cannot be used together with neither the APS function or RANDOM function. And in the repeat speech, there are non-speech state (about 80 ms) between phrases.

5.10.2 Random Function

One phrase is randomly selected out of a certain number of phrases and talked by setting the RANDOM pin high and giving the speech start input - 1.(the speech start input - 2 cannot be used .)

Maximum of 8 phrases can be talked at random. The number is to be set by the input of the SEL0 – SEL5. The following table shows the setting of the SEL0 – SEL5 pins which instruct quantity of phrases to be talked randomly and the number of phrase where the phrase is stored.

Table 5.3 SEL0 – SEL5 and phrases in random function

Setting of SEL PINs						Qty. of phrases	No. of phrase
SEL5	SEL4	SEL3	SEL2	SEL1	SEL0		
0	0	0	*	*	*	8	56~63
0	0	1	1	1	1	7	56~62
0	0	1	1	1	0	6	56~61
0	0	1	1	0	1	5	56~60
0	0	1	1	0	0	4	56~59
0	0	1	0	1	1	3	56~58
0	0	1	0	1	0	2	56~57

1 = high level
0 = low level
* = don't care

The random function cannot be used together with neither the APS function or repeat function.

5.11 Input Resistors

The $\overline{ACL}$ and the STBY are connected with pull-up resistors, while the TEST, the EV1 and the EV2 being connected with pull-down resistors. The START and SEL0 – SEL5 are connected with pull-down resistors under certain conditions.

5.11.1 The SEL0 – SEL5 and START pins, and Pull-down Resistors

The pull-down resistors are connected to the START, the SEL0 – SEL5 according to inputs at the PLDN, the PLS, the CPUM and the RANDOM, as shown in the following table.

Table 5.4 Pull-down resistors of SEL0 – SEL5 and START

CONDITION				START		SEL0~SEL5	
CPUM	RAN -DOM	PLDN	PLS	Stand-by	Non-Stand-by	Stand-by	Non-Stand-by
1	*	*	*	None	None	None	None
0	*	0	*	None	None	None	None
0	1	1	0	Pull-down	Pull-down	None	None
0	1	1	1	None °	Pull-down	None	None
0	0	1	0	Pull-down	Pull-down	None °	Pull-down
0	0	1	1	None °	Pull-down	Pull-down	Pull-down

1 = high
0 = low
* = Don't care

None····· Pull-down resistor is not connected. (Open input)

Pull-down··· Pull-down resistor is connected.

°····· PIN input level is not entered in the internal circuit which is fixed at high level. (Internal circuit is stabilized, despite open input.)

5.11.2 Operating Status and Pins Setting in Manual Control

The settings of pins when actually constructing a system, are shown in the following.

Table 5.5 Operating status in manual control and setting of the PLDN and the PLS

No.	APS function	Operating status	PIN setting		Drawing
			PLDN	PLS	
1	APS = Low	· Speech beginning input – 1	High	Low	Fig.5 – 13 (a)
2		· Speech beginning input – 2	High	High	Fig.5 – 13 (b)
3		· Random speech · (Speech beginning input – 1)	High	Low	Fig.5 – 13 (c)
4	APS = High	· Speech beginning input – 1	High	Low	Fig.5 – 13 (a)
5		· Speech beginning input – 2	High	High	Fig.5 – 13 (b)

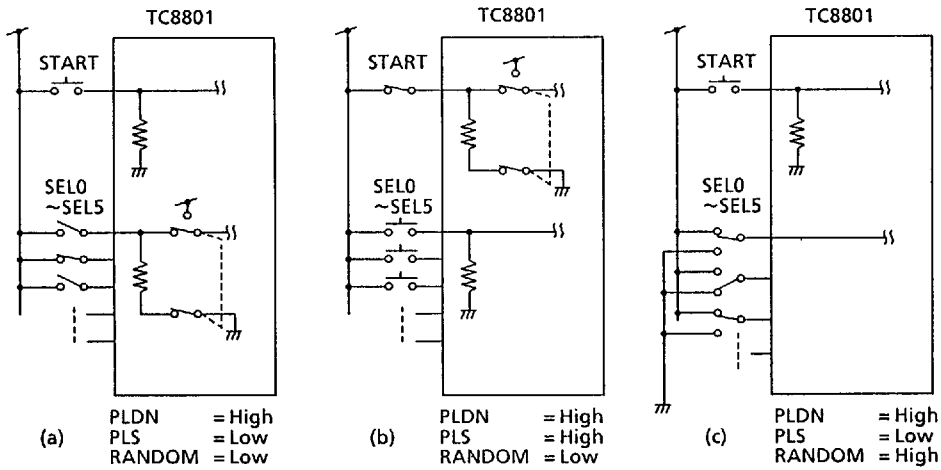


Fig.5.13 Examples of setting on the manual control and internal states

5.11.3 APS function and Pull - down Resistance

An example No.4 in the Table 5.5 is described in the following, where speech is synthesized by the speech start input - 1 using the automatic power stand-by function. (Fig.5.15)

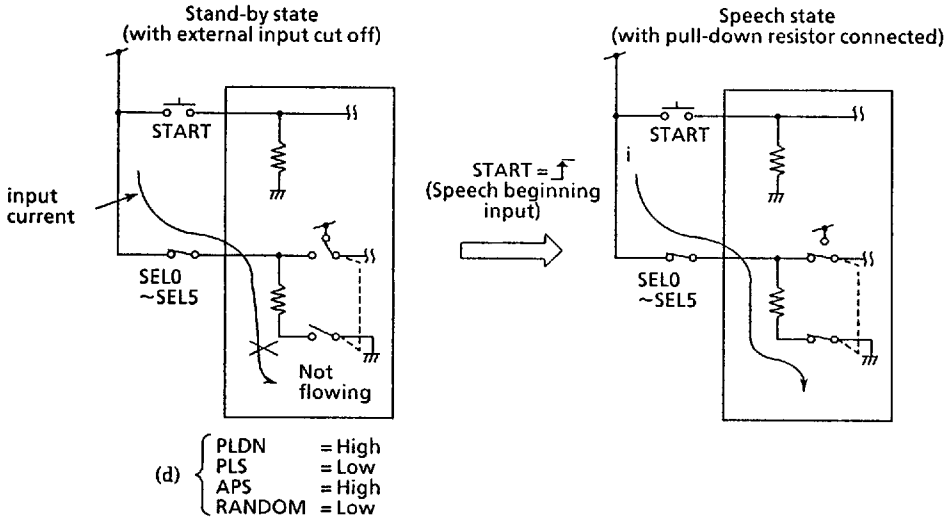


Fig.5.14 Pull-down resistors at the START, the SEL0 – SEL5 in manual control

In stand-by, the SEL0 – SEL5 are disconnected from the pull-down resistors to cut off current entering into the pull-down resistor. (Internally, the SEL0 – SEL5 are fixed at high level.) Next, when a speech start input is given at the START, the pull-down resistors are connected to SEL0 – SEL5 pins and speech begins. In other words, current flows into the pull-down resistor only during speech state, thus reducing current consumption during stand-by.

On the CPU control, the SEL0 – SEL5 and START are not connected with pull down resistors.

5.12 Phrase Edition

Follow the following flow chart, when you make TC8801 speak several phrases continuously (phrase Edition)

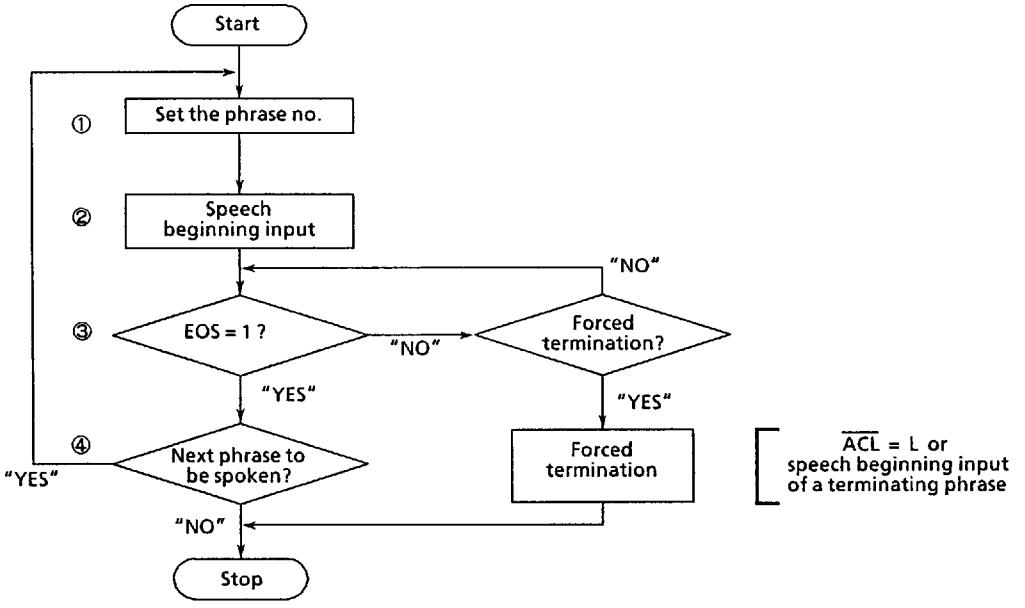


Fig.5.15 Flow chart; phrase edition

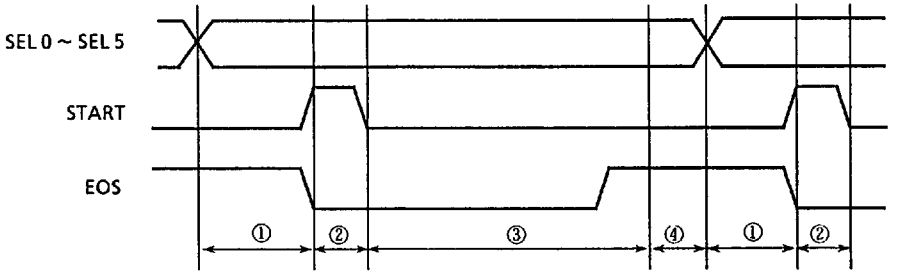
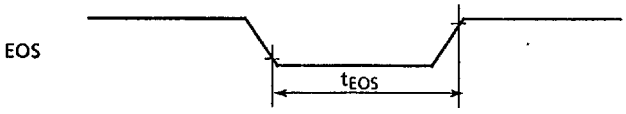


Fig.5.16 Timing for phrase edition (CPU control)

Phrases can be spoken continuously (phrase Edition can be executed), when CPUM is either high or low. But, when CPUM is low, note that SEL0~SEL5 and START are connected the chattering preventing circuit. (For more detail, see 5.8 and 6.4.3)

EOS goes from high to low, even when a phrase, that has no voice data, is executed.

In this case, the EOS low time (t_{EOS}) is as follows.



Item and Conditions		Max	note
t_{EOS}	CPUM = L , APS = L	2000tΦ	
	CPUM = L , APS = H	3000tΦ	
	CPUM = H , APS = L	t_{PWH} + 2500tΦ	1
	CPUM = H , APS = H	t_{STA} + t_{PWH} + 4500tΦ	1,2

1tΦ = 10 / f_{CLK} (ceramic oscillation)
1 / f_{CLK} (RC oscillation)

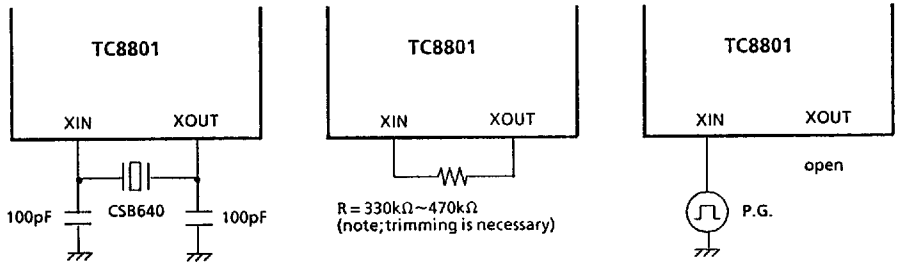
Note 1 The start pulse width (t_{PWH}) is added to the EOS low time,when CPUM is high level.
Note 2 t_{STA} is oscillation start time. (refer to 6.3 DC characteristics)

Fig.5.17 t_{EOS}, when the phrase without voice data is executed.

5.13 Oscillating Circuit

The TC8801 contains a built-in oscillating circuit which oscillates by connecting a ceramic resonator and capacitors or a resistor to the XIN and the XOUT, for the ceramic or RC oscillation, respectively.

When external clock is to be entered, input directly to XIN. At that time, XOUT need not be connected to an external circuit. (Fig.5.18 (c))



(a) use of internal oscillation circuit (640kHz)
[ceramic oscillation circuit]

(b) use of internal oscillation circuit (64kHz)
[RC oscillation circuit]

(c) use of external clock
[ceramic oscillation circuit ··· 640kHz]
[RC oscillation circuit ····· 64kHz]

Fig.5.18 Example of connecting parts with oscillation circuit

Note Where the TC8801 is mounted on board, etc. together with resistor R for RC oscillation, there are stray capacity on the XIN, XOUT and resistor R, so adjust external resistance R accordingly.

The R value of 330kΩ – 470 kΩ shown previous relate to a stray capacity of 5 pF or less

5.14 The $\overline{ACL}$ pin

Connect a capacitor parallel to the external switch of the $\overline{ACL}$ to ensure clearing the inner circuit on supplying the power. (Fig.5.19)

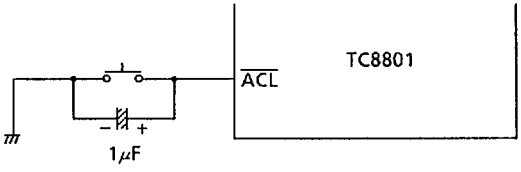


Fig. 5.19 Connection of the ACL

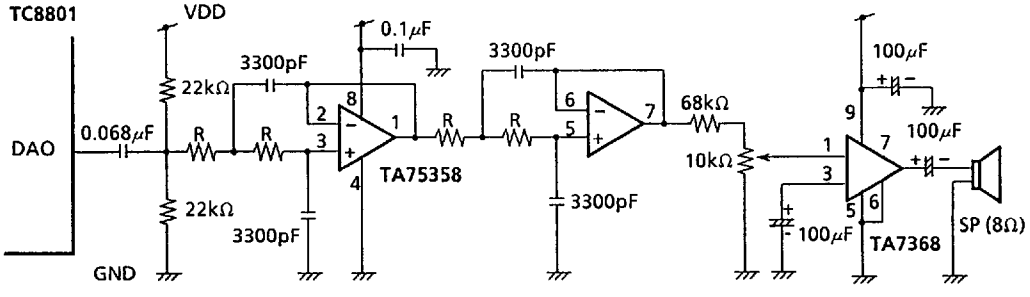
However, power on clear in this case is effective only for a step power rise, and when power rise is gentle power on clear is not performed.

5.15 The DAO pin

The voice synthesis system is configured by connecting the DAO with a filter and an amplifier

5.15.1 Active Filter

Fig 5.20 is an example of connection the DAO with an active filter, an amplifier and a speaker.



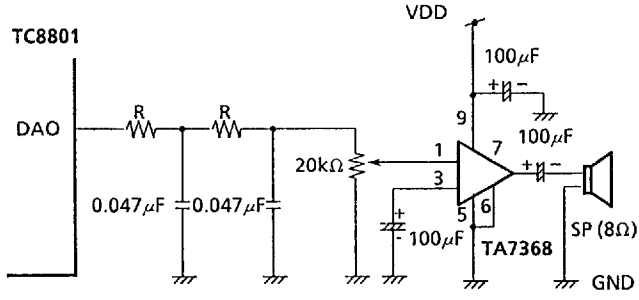
Bit Rate	R
32kbps	10kΩ
16kbps	22kΩ

Adjust the value of R according to voice quality.

Fig.5.20 Example of connection of active filter

5.15.2 Passive Filter

Fig 5.21 is an example of connection the DAO with an passive filter, amplifier and a speaker



Bit Rate	R
32kbps	1.2kΩ
16kbps	10kΩ

Adjust the value of R according to voice quality.

Fig.5.21 Example of connection of passive filter

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	−0.3 ~ 6.0	V
V_{IN}	Input voltage	−0.3 ~ V_{DD}+0.3	V
V_{OUT}	Output voltage	−0.3 ~ V_{DD}+0.3	V
T_{STG}	Storage temperature	−55 ~ 125	°C

6.2 Recommended Operating Conditions

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	2.4 ~ 5.5	V
V_{IN}	Input voltage	0 ~ V_{DD}	V
V_{OUT}	Output voltage	0 ~ V_{DD}	V
T_{OPR}	Operating temperature	−10 ~ 70	°C
f_{CLK1}	Operating frequency (Ceramic Oscillation)	610 ~ 670	kHz
f_{CLK2}	Operating frequency (RC Oscillation)	61 ~ 67	kHz

6.3 DC Characteristics

(Unless otherwise specified, V_{DD} = 5.0V, Ta = 25°C)

SYMBOL	ITEM	CONDITION		MIN	TYP	MAX	UNIT
I_{IH}	High level input current	SEL0~SEL5、START TEST、EV1、EV2	V_{DD} = 5V、V_{IN} = 5V (with pull - down resistor)	10	50	100	μA
I_{IL1}	Low level input current 1	$\overline{ACL}$	V_{DD} = 5V、V_{IN} = 0V	200	500	800	μA
I_{IL2}	Low level input current 2	STBY	V_{DD} = 5V、V_{IN} = 0V	5	25	100	μA
I_{ILK}	Leak input current	Other than uppers	V_{DD} = 2.4~5.5V、V_{IN} = 0~V_{DD}	-	-	3	μA
V_{IH1}	High level input voltage 1	CPUM、APS、PLDN、PLS	V_{DD} = 5.5V	4.7	-	-	V
			V_{DD} = 2 4V	2 0	-	-	V
V_{IH2}	High level input voltage 2	Other than upper pins	V_{DD} = 4 5~5 5V	2.3	-	-	V
			V_{DD} = 2.4V	1.8	-	-	V
V_{IL1}	Low level input voltage 1	CPUM、APS、PLDN、PLS	V_{DD} = 5.5V	-	-	0.8	V
			V_{DD} = 2 4V	-	-	0.2	V
V_{IL2}	Low level input voltage 2	Other than upper pins	V_{DD} = 4.5~5.5V	-	-	0.5	V
			V_{DD} = 2.4V	-	-	0.2	V
I_{OH}	High level output current	APD、EOS	V_{DD} = 2.4V、V_{OUT} = 2.0V	200	-	-	μA
I_{OL}	Low level output current	APD、EOS	V_{DD} = 2 4V、V_{OUT} = 0 4V	500	-	-	μA
I_{DDO}	Current consumption in waiting state	VDD	V_{DD} = 5 0V、I_{OUT} = 0mA	-	-	900	μA
			V_{DD} = 2.4V、I_{OUT} = 0mA	-	-	400	μA
I_{DDS}	Current consumption in stand-by state	STBY > V_{DD} - 0 2V	V_{DD} = 2.4~5.5V、I_{OUT} = 0mA	-	-	3	μA
T_{STA}	Oscillation starting time	XOUT	V_{DD} = 5 0V	-	-	500	ms
			V_{DD} = 2 4V	-	-	700	ms

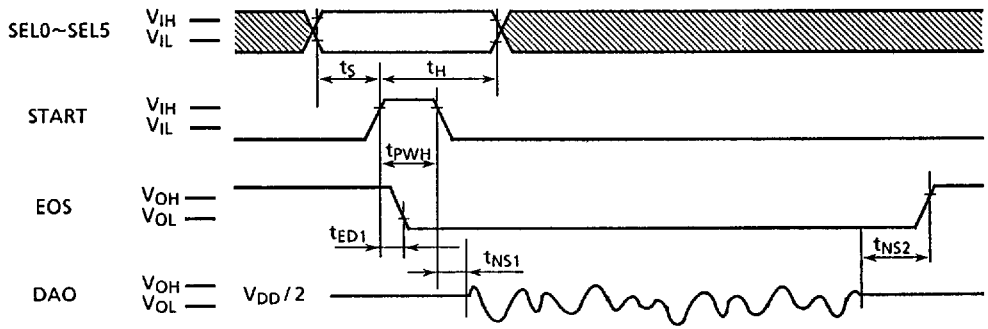
Precautions : 1) The values in the table are the absolute values.
2) Ceramic oscillation ··· f_{CLK} = 640kHz, RC oscillation ··· f_{CLK} = 64kHz

6.4 AC Characteristics (f_{OSC} = 640kHz (ceramic oscillation), 64kHz (RC oscillation))

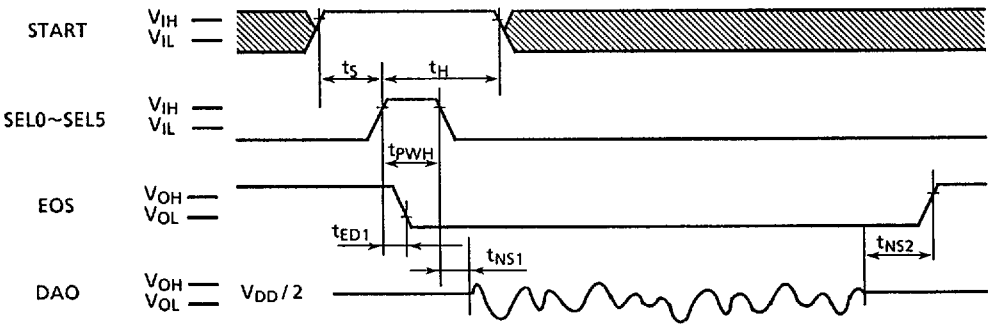
6.4.1 Timing In CPU Control (APS = STBY = low)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_S	Setup time	400	—	—	ns
t_H	Hold time	360	—	—	
t_{PWH}	Start pulse width	600	—	—	
t_{ED1}	EOS delay time	—	—	900	
t_{NS1}	No voice time 1	—	2	—	ms
t_{NS2}	No voice time 2	10	—	40	

(1) Speech beginning input - 1



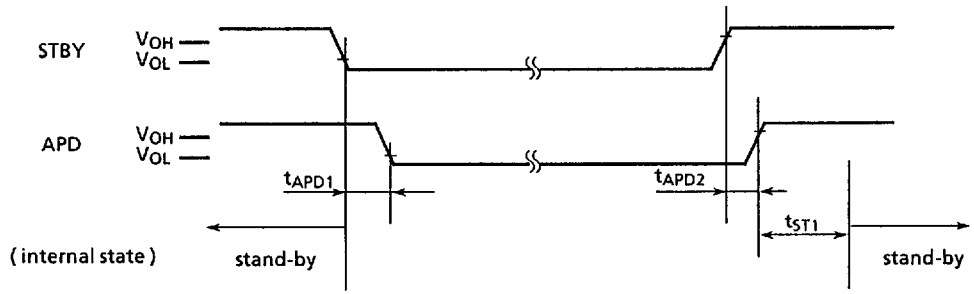
(2) Speech beginning input - 2



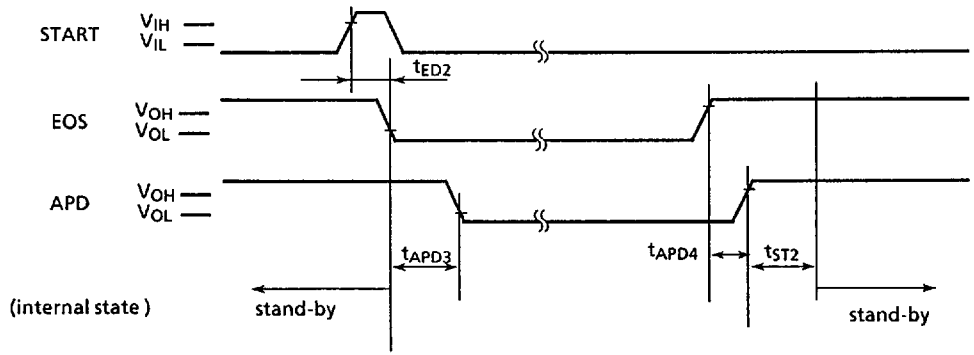
6.4.2 Standby State and APD Output In CPU Control

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{APD1}	APD delay time 1	—	—	700	ms
t_{APD2}	APD delay time 2	—	—	900	ns
t_{APD3}	APD delay time 3	—	—	700	ms
t_{APD4}	APD delay time 4	—	—	20	μs
t_{ED2}	EOS delay time 2	—	—	900	ns
t_{ST1}	Stand-by delay time 1	—	—	20	ms
t_{ST2}	Stand-by delay time 2	—	—	20	

(1) Stand-by state by the STBY pin (APS = L level)



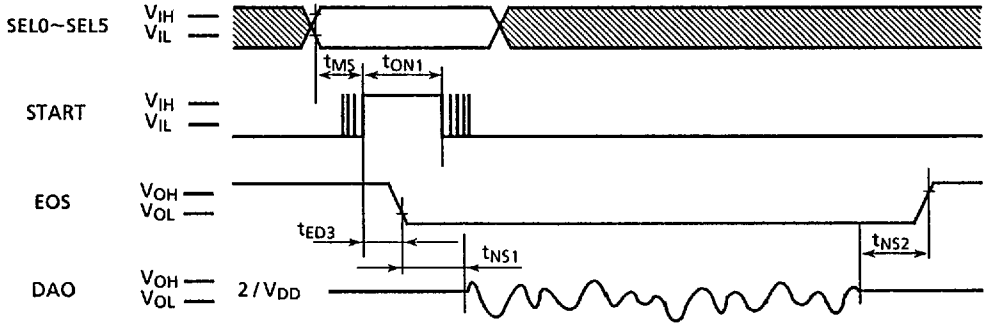
(2) Stand-by state by the APS pin (APS = H level)



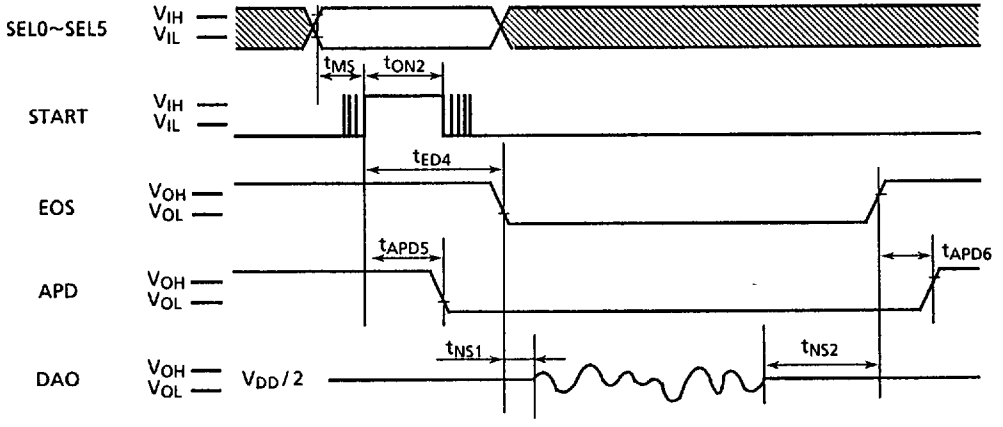
6.4.3 Timing on Manual Control

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{MS}	Manual control set up time	0	—	—	ns
t_{ON1}	Switch on time 1	32	—	—	ms
t_{ON2}	Switch on time 2	750	—	—	
t_{ED3}	EOS delay time 3	—	—	32	
t_{ED4}	EOS delay time 4	—	—	750	ns
t_{NS1}	No speech time 1	—	2	—	ms
t_{NS2}	No speech time 2	10	—	40	
t_{APD5}	No speech time 5	—	—	700	
t_{APD6}	APD delay time 6	—	—	20	μs

(1) Not during automatic power stand-by function (APS = low)

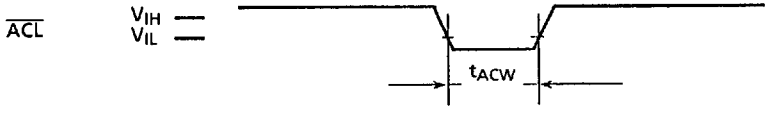


(2) During automatic power stand-by function (APS = high)

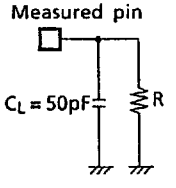


6.4.4 $\overline{ACL}$ Pulse Width

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT
t_{ACW}	$\overline{ACL}$ pulse width	500	—	—	ns



6.4.5 Measurement Circuit



Input level
- V_{IH} = 2.6V
- V_{IL} = 0.6V

Comparison level
- V_{IH} = 2.4V
- V_{IL} = 0.8V
- V_{OH} = 2.4V
- V_{OL} = 0.8V

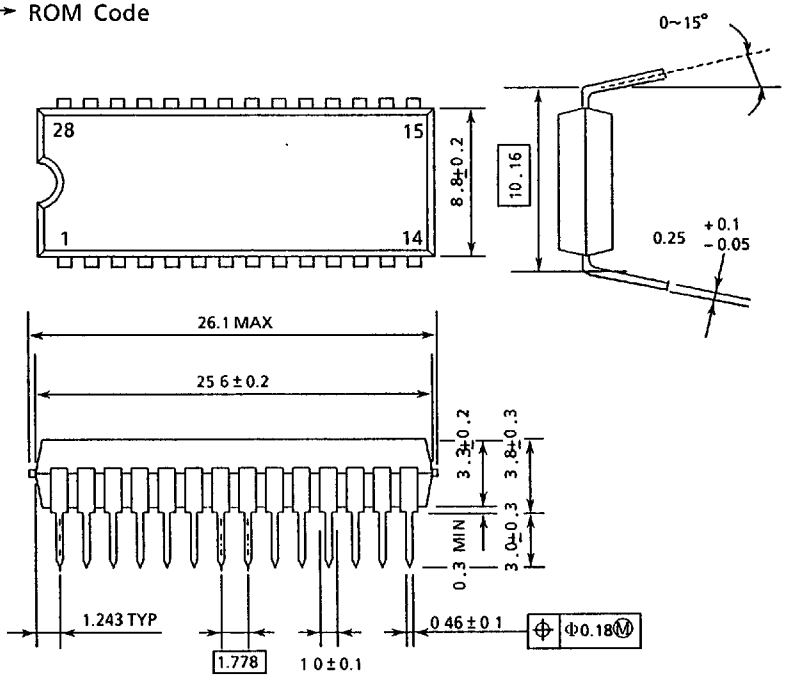
※ R =
t_{ACC} ····· 10kΩ
t_{OD} ····· 1kΩ

7. OUTLINE DRAWINGS

(1) 28pin shrink dual in-line package (SDIP28 - P - 400)

TC8801N-XXXX
ROM Code

unit : mm

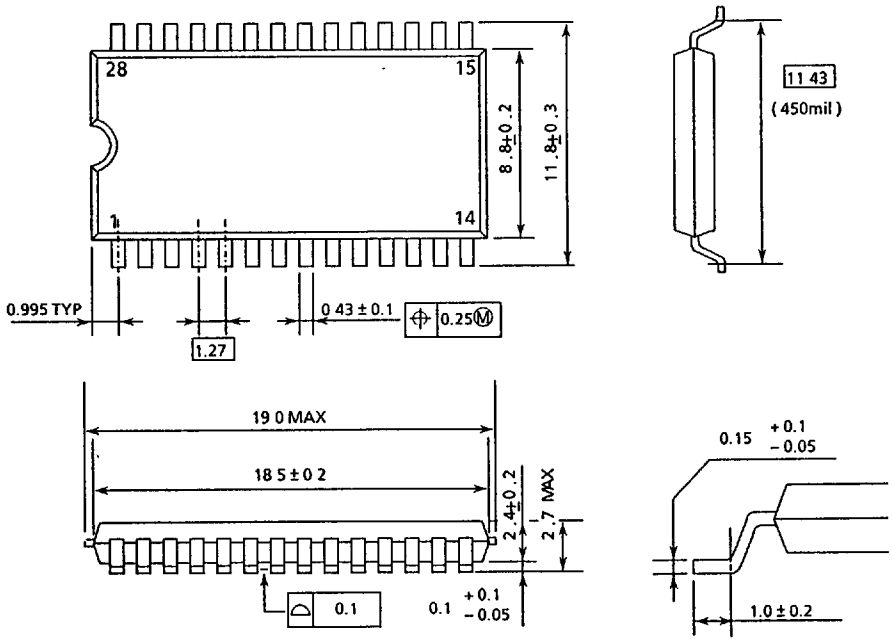


NOTE . Tolerance of lead position : ⌖ Φ0.18Ⓜ ows that the leads exist in all circles with a radius of {(0.46 + 0.1) + 0.18}/2 mm against the center position of lead (geometrical position).

(2) 28pin small outline package (SOP28 - P - 450)

TC8801F-XXXX
└→ ROM Code

unit : mm



NOTE . Tolerance of lead position : 0.25M shows that the lead flat positions exist in all range of {(0.43 + 0.1) + 0.5}/2 mm against the center position of lead (geometrical position).

Lead coplanarity : 0.1 shows the uniformity of bottom of leads, Maximum value is 0.1.

8. APPLICATION CIRCUIT

8.1 Normal Speech or Repeat Speech

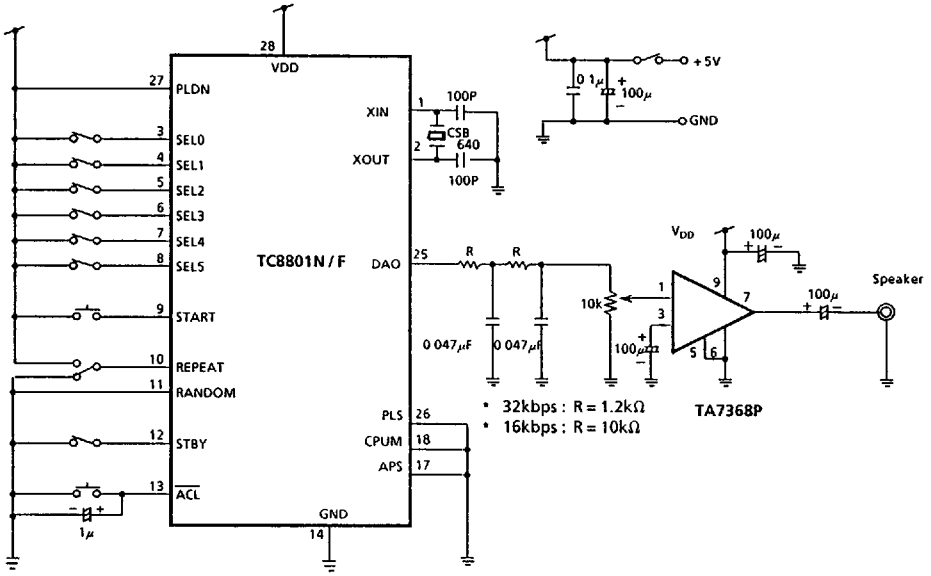
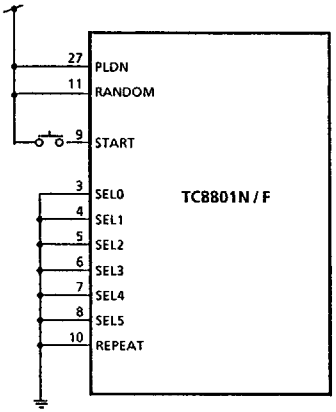


Fig.10.1 Normal speech, repeat speech application circuit

8.2 Random Speech



This figure is in the case of 8 phrase of random speech.

Other pins are the same as the above figure

Fig.10.2 Random speech