POWER MANAGEMENT

Description

The SC2616 is a fully integrated DDR power solution providing power for the VDDQ and the VTT rails. The SC2616 also completely adheres to the ACPI sleep state power requirements. A synchronous buck controller provides the high current of the VDDQ at high efficiency, while a linear sink/source regulator provides the termination voltage with 2 Amp Source/Sink capability. This approach makes the best trade-off between cost and performance. Additional logic and UVLOs complete the functionality of this single chip DDR power solution in compliance with S3 and S5 motherboard signals.

The SC2616 is capable of sourcing up to 20A at the switcher output, and 2A source/sink at the VTT output. The MLP package provides excellent thermal impedance while keeping small footprint. VDDQ current limit as well as 3 independent thermal shutdown circuits assure safe operation under all fault conditions.

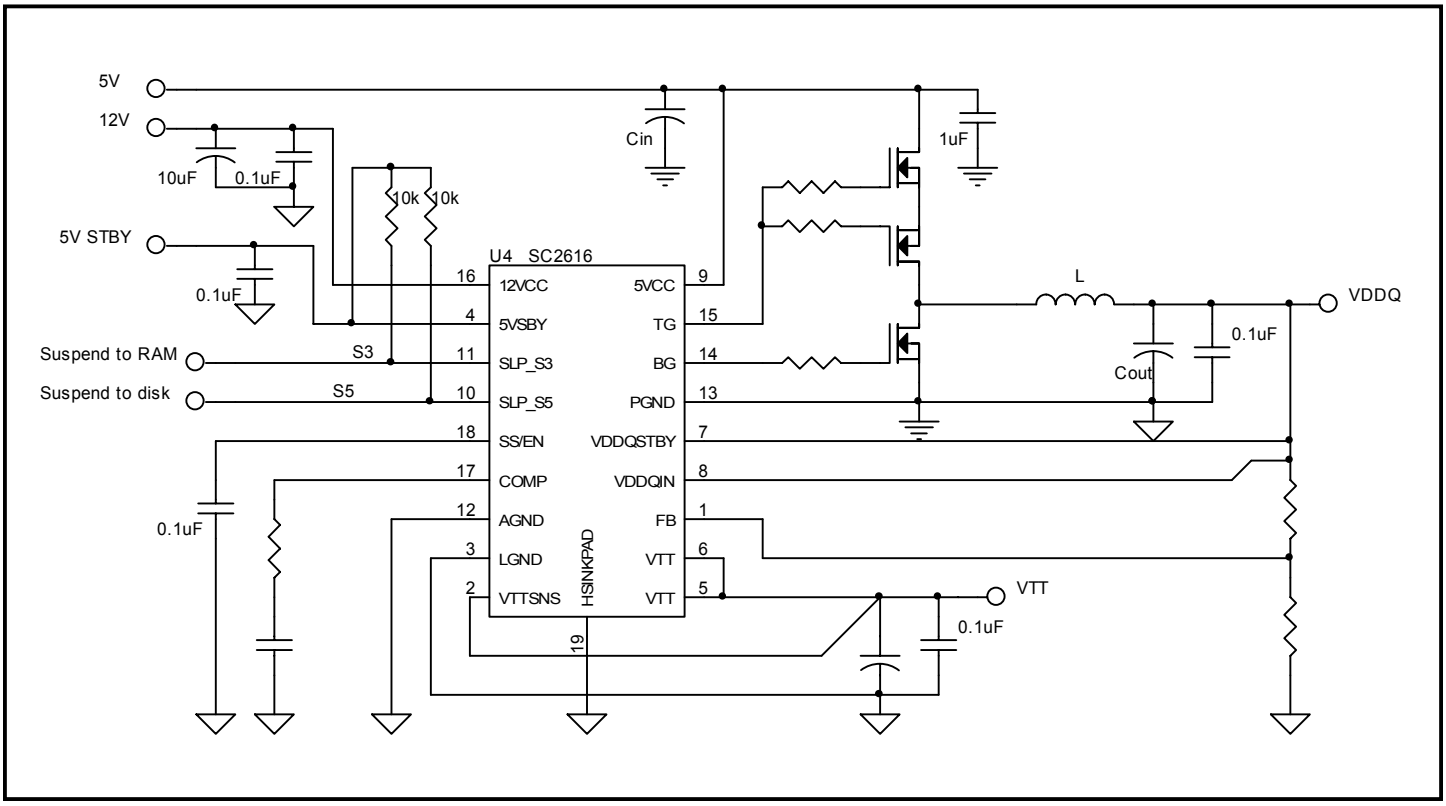
Features

- High efficiency (90%) switcher for **VDDQ supplies 20 Amps**
- High current gate drives
- Single chip solution complies fully with ACPI power sequencing specifications
- **Internal S3 state LDO supplies high standby VDDQ current (0.65Amp Min.)**
- ACPI sleep state controlled
- **2 Amp VTT source/sink capability**
- UVLO on 5V and 12V
- Independent thermal shutdown for VDDQ and VTT
- Fast transient response
- 18 pin MLP package

Applications

- Power solution for DDR memory per ACPI motherboard specification
- High speed data line termination
- Memory cards

Typical Application Circuit



Dual 5V Typical Application Schematic

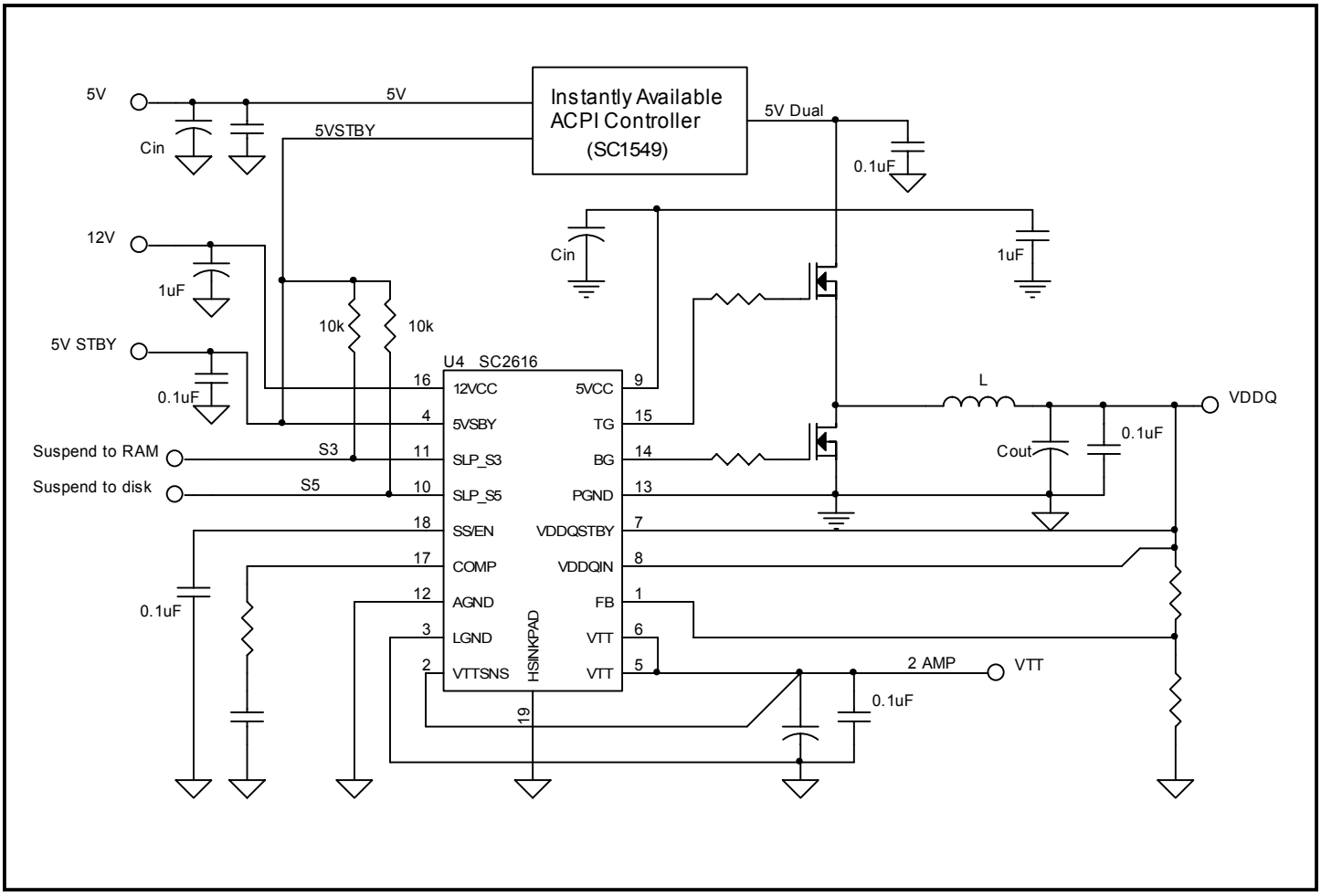


Figure 1: ACPI controller supplies “always on” 5V supply, eliminating the need for back to back MOSFETs. (see applications section)

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Supply Voltage, 5VCC to AGND	V_{5VCC}	7	V
Supply Voltage, 12VCC to AGND	V_{12VCC}	15	V
Standby Input Voltage	V_{5VSBY}	7	V
Inputs	I/O	5VSTBY +0.3, AGND -0.3	V
AGND to PGND or LGND		0.3	V
VTT Output Current	$I_{O(VTT)}$	±2	A
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature	T_J	125	°C
Thermal Resistance Junction to Ambient *	θ_{JA}	25	°C/W
Thermal Resistance Junction to Case *	θ_{JC}	4	°C/W
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering) 10seconds	T_{LEAD}	300	°C
TG/BG DC Voltage		12Vcc + 0.3, AGND -0.5	V
TG/BG AC Voltage		12Vcc + 1.0, AGND -1.0	V
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

* See Mounting Considerations.

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
5V Supply Voltage	V_{5VCC}		4.5	5	5.5	V
12V Supply Voltage	V_{12VCC}		10.8	12	13.2	V
5V Standby Voltage	V_{5VSBY}		4.5	5	5.5	V
Quiescent Current	$I_{Q(5VSBY)}$	S0, S5		1.8	2.5	mA
		S3		3.5	5.0	
S3/S5 Threshold				TTL		V
12VCC Under Voltage Lockout	$UVLO_{12VCC}$		7	8.2	10	V
5VCC Under Voltage Lockout	$UVLO_{5VCC}$		3.5	3.7	4	V
Feedback Reference	V_{REF}			1.25		V
Feedback Current	I_{FB}	V_{FB} = 1.25V			2	µA
SS/EN Shutdown Threshold	$V_{EN(TH)}$			0.3		V
Thermal Shutdown	T_{J-SHDN}			150		°C
Thermal Shutdown Hysteresis	T_{J-HYST}			10		°C

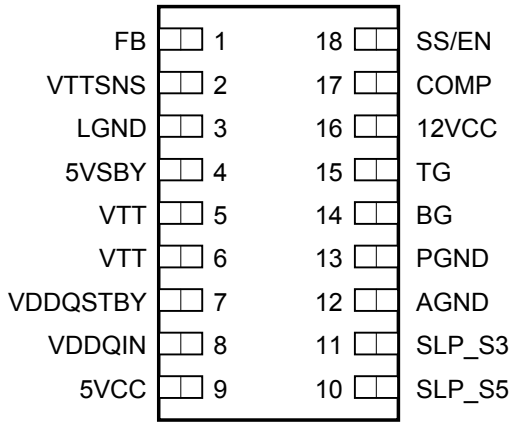
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, 12VCC = 12V, 5VCC = 5V, 5VSBY = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Switcher						
Load Regulation		I_{VDDQ} = 0A to 10A; S0; Fig 2:		0.2		%
Oscillator Frequency	f_{OSC}		225	250	275	KHz
Soft Start Current	I_{SS}			25		µA
Duty Cycle			0		80	%
Overcurrent Trip Voltage	V_{TRIP}	% of VDDQ Setpoint	50	60	70	%
Top Gate Rise Time	TG_R	Gate capacitance = 4000pF		25		nS
Top Gate Fall Time	TG_F	Gate capacitance = 4000pF		25		nS
Bottom Gate Rise Time	BG_R	Gate capacitance = 4000pF		35		nS
Bottom Gate Fall Time	BG_F	Gate capacitance = 4000pF		35		nS
Dead Time	t_d		20	50		nS
Error Amplifier Transconductance	gm			0.8		mS
Error Amplifier Gain @ DC	A_{EA}	R_{COMP} = open		38		dB
Error Amplifier Bandwidth	G_{BW}			5		MHz
Error Amplifier Source/Sink Current				±60		µA
Modulator Gain	A_M	V_{IN} = 5V		19		dB
Power Good Low		I_{PWRGD} = 1mA, sink		50	400	mV
Power Good High Leakage		V_{PWRGD} = 5V; S0		0.1	2	µA
STBY LDO						
Output Current	$I_{VDDQSTBY}$	DC current	750			mA
Load Regulation	ΔV/ΔI	I_{VDDQ} = 0A to 750mA; S3; Fig1:		0.5		%
Current Limit	I_{LIM}	S3 = 0, VTT floating		1		A
VTT LDO						
Output Voltage	VTT	$V_{VDDQSTBY}$ = 2.500V	1.235	1.250	1.265	V
Source and Sink Currents	I_{VTT}		±1.8			A
Load Regulation	ΔVTT/ ΔI	I_{VTT} =+1.8A to -1.8A			±1	%
Error Amplifier Gain	A_{EA_VTT}			75		dB
Current Limit	VTT_{ILIM}	S3 = high		3		A

Pin Configuration

TOP VIEW



(18 Pin MLP)

Note: Pin 19 is the thermal Pad on the bottom of the device

Ordering Information

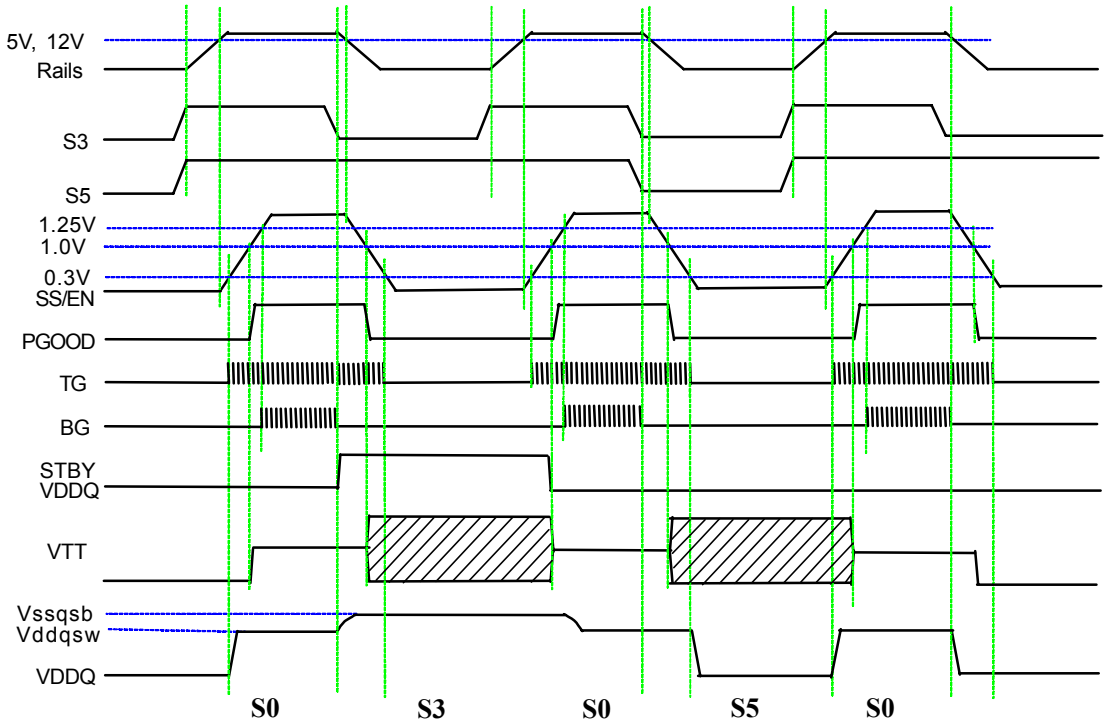
Part Numbers	Package
SC2616MLTR(1)	MLP-18

Note:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

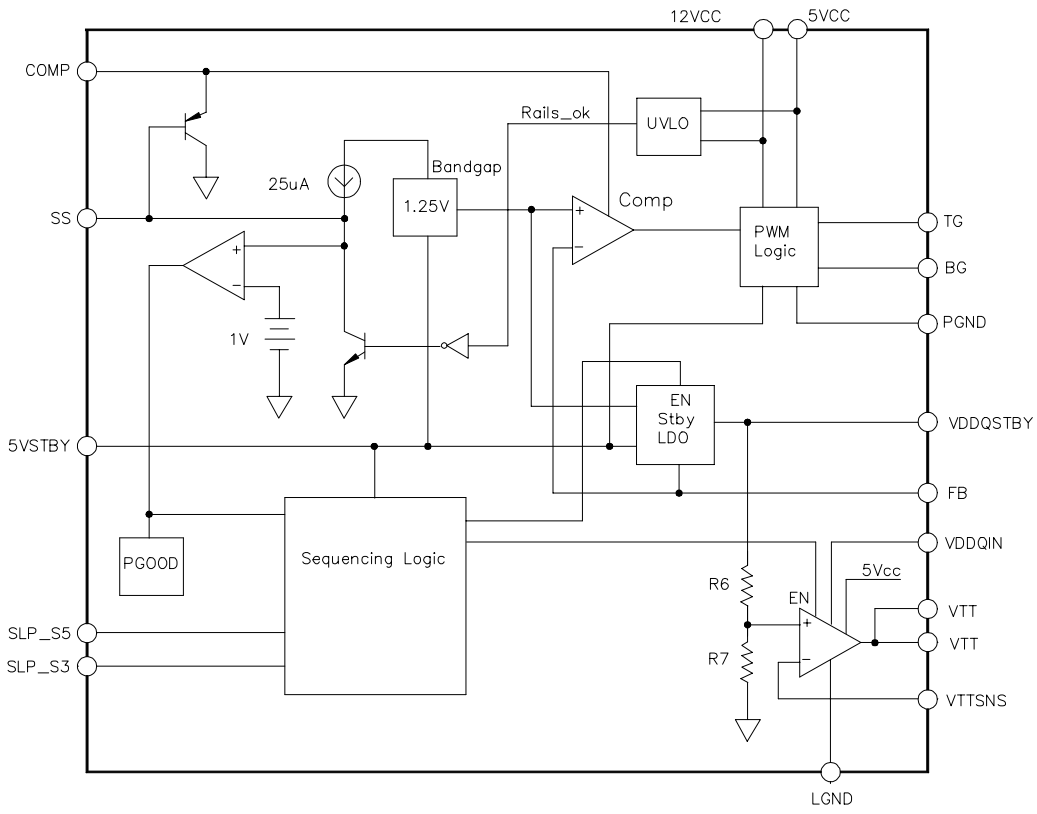
Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback for the STBY LDO and the switcher for VDDQ.
2	VTTSNS	VTT LDO feedback and remote sense input.
3	LGND	VTT return. Connect to point of load return. The trace connecting to this pin must be able to carry 2 Amps.
4	5VSBY	Bias supply for the chip. Connect to 5V standby.
5, 6	VTT	VTT return. Connect to point of load return. The trace connecting to this pin must be able to carry 2 Amps.
7	VDDQSTBY	S3 VDDQ output. Provision must be made to prevent the VDDQSTBY supply from back feeding the input supply (see typical application schematic). Traces connecting to this pin must be capable of carring 1 Amp.
8	VDDQIN	VDDQ power input to VTT LDO. The trace connecting to this pin must be able to carry 2 Amps.
9	5VCC	Supply to the lower gate drive.
10	SLP_S5	Connect to S5 signal from motherboard.
11	SLP_S3	Connect to S3 signal from motherboard.
12	AGND	Analog ground.
13	PGND	Gate drive return. Keep this pin close to bottom FET source.
14	BG	Bottom gate drive.
15	TG	Top gate drive.
16	12VCC	Supply to the upper and lower gate drives.
17	COMP	Compensation pin for the PWM transconductance amplifier.
18	SS/EN	Soft start capacitor to GND. Pull low to less than 0.3V to disable controller.
19	TH_PAD	Copper pad on bottom of chip used for heatsinking. This pin is internally connected to AGND.

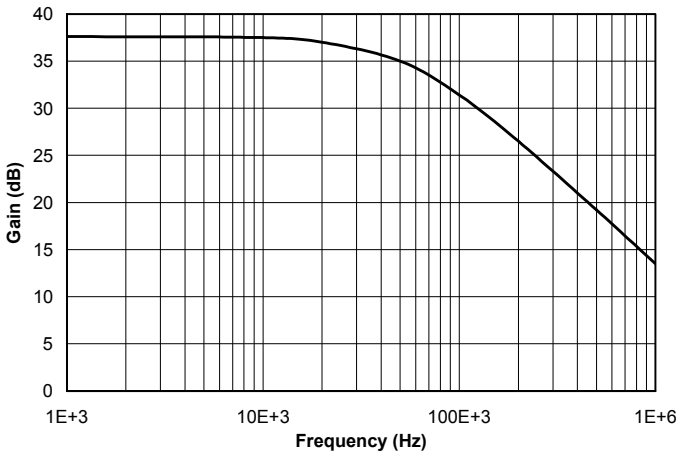
Timing Diagram



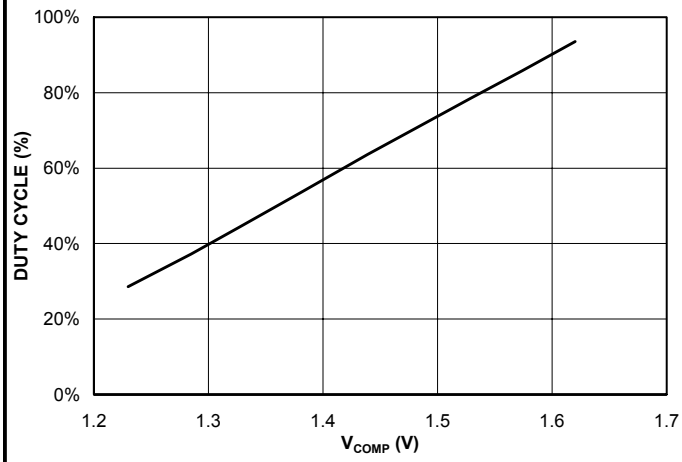
Block Diagram



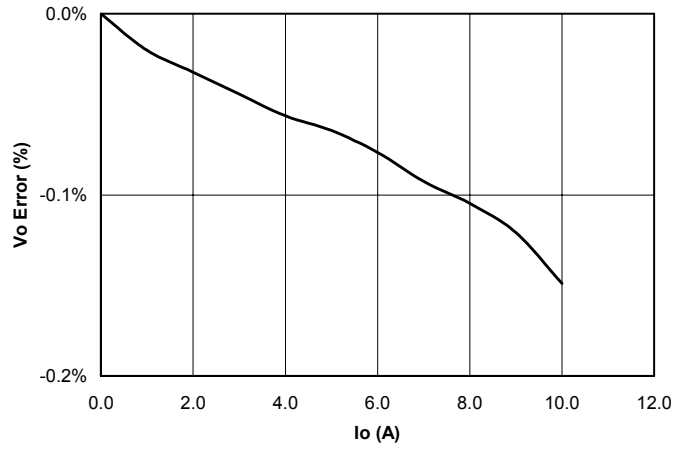
Typical Characteristics



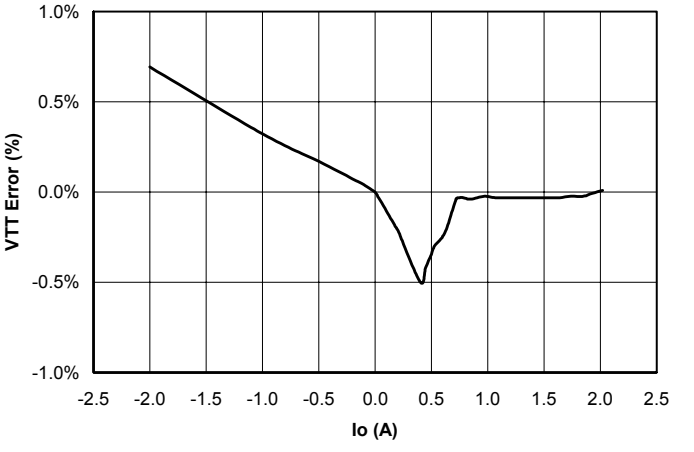
Switching Section Error Amplifier Gain



VCOMP vs Duty Cycle



VDDQ Load Regulation



VTT Load Regulation, Source and Sink

Evaluation Board Schematic

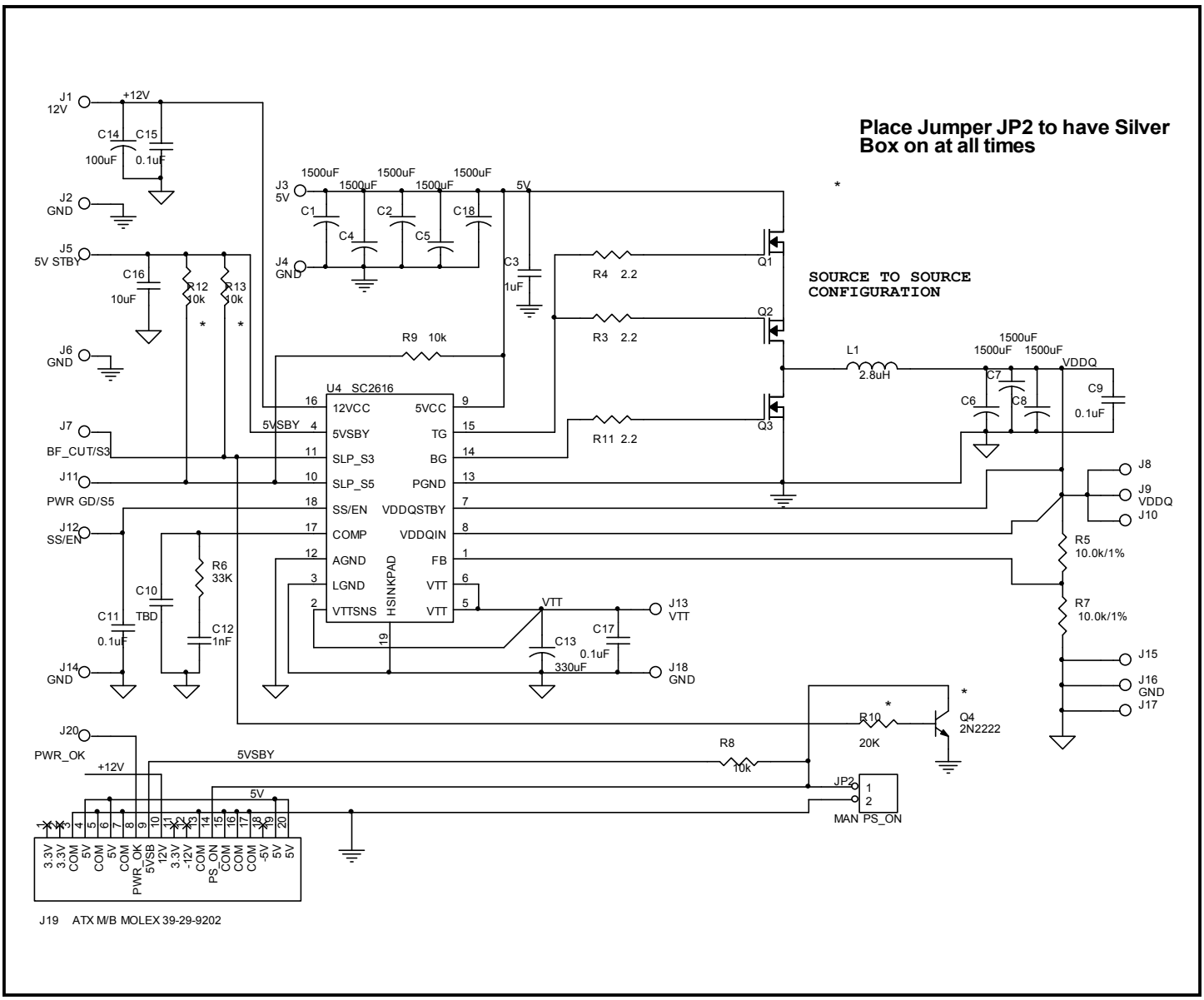


Figure 2

Evaluation Board Bill of Materials

Item	Quantity	Reference	Part	Manufacturer
1	8	C1,C2,C4,C5,C6,C7,C8,C18	1500uF	Sanyo MX_CX
2	1	C3	1uF	any
3	5	C9,C11,C15,C16,C17	0.1uF	any
4	1	C10	TBD	
5	1	C12	1nf	
6	1	C13	330uF	any
7	1	C14	100uF	any
8	1	JP2	MAN PS_ON	
9	19	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11, J12,J13,J14,J15,J16,J17,J18,J20	ED5052	
10	1	J19	ATX M/B	MOLEX P/N: 39-29-9202
11	1	L1	2.8uH	FALCO P/N: T50168 (www.falco.com)
12	3	Q1,Q2,Q3	FDB7030BL	Fairchild P/N: FDB7030BL
13	1	Q4	2N2222	any
14	3	R3,R4,R11	2.2	any
15	2	R5,R7	10.0k, 1%	any
16	1	R6	33k	any
17	4	R8,R9,R12,R13	10k	any
18	1	R10	20k	any
19	1	U4	SC2616	Semtech

Typical Characteristics (Cont.)

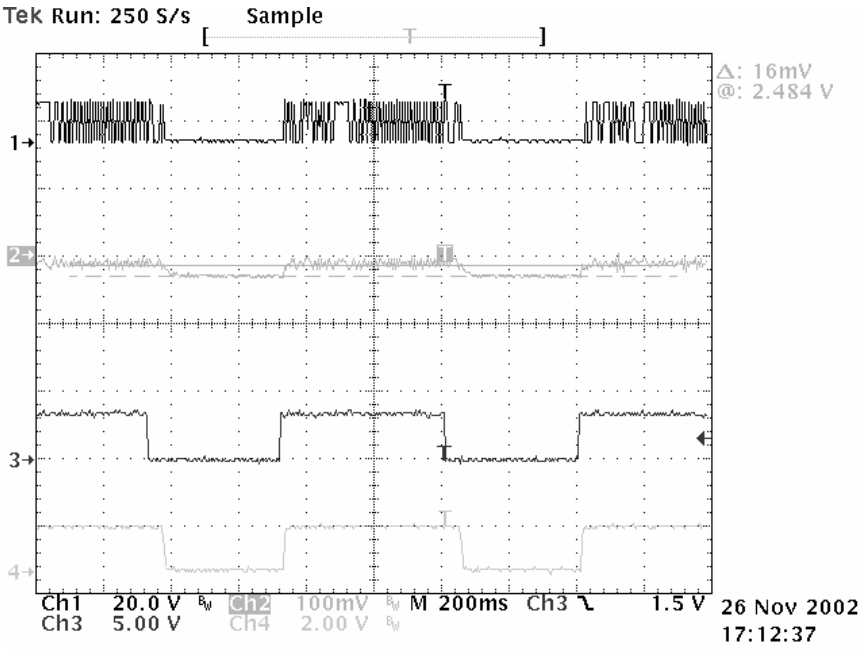


Figure 3: S3 to S0 state transition with **600mA** load on VDDQ
Ch1: TG drive, Ch2: VDDQ w/2.5V offset, Ch3, S3, Ch4: SS/EN

Note: VDDQ changes 16mV between S0 and S3 states (see cursor).

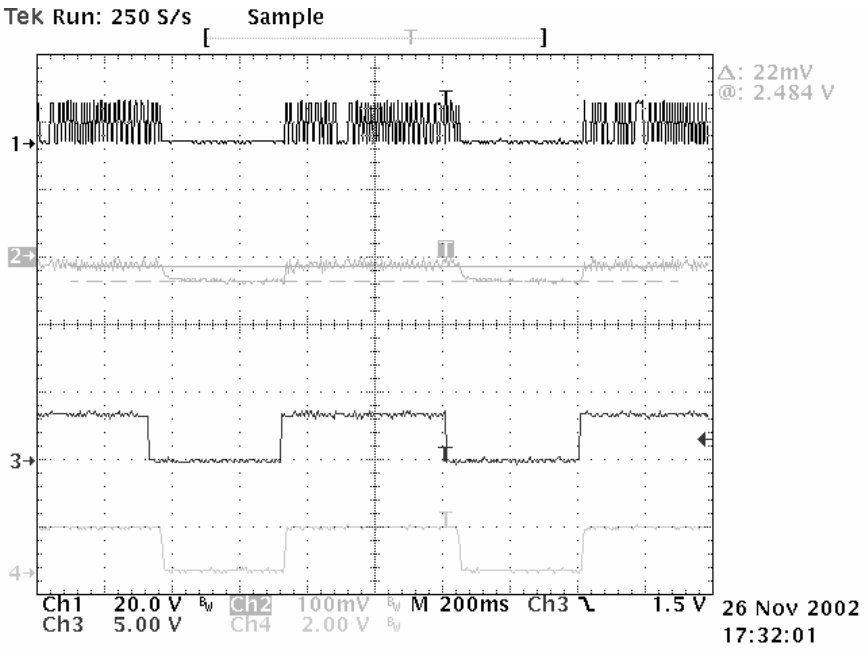


Figure 4: S3 to S0 state transition with **800mA** load on VDDQ
Ch1: TG drive, Ch12 VDDQ w/2.5V offset, Ch3, S3, Ch4: SS/EN

Note: VDDQ changes 22mV between S0 and S3 states (see cursor).

Applications Information

Description

The Semtech SC2616 DDR power supply controller is the latest and most complete switching and linear regulator combination, providing the necessary functions to comply with S3 and S5 sleep state signals generated by the Desktop Computer Motherboards. VDDQ supply, and VTT termination voltage are supplied to the Memory bus during S0 (normal operation) state. During S0, VDDQ is supplied via the Switching regulator, sourcing high output currents to the VDD bus as well as supplying the termination supply current. The SC2616 is capable of driving a 4000pf capacitor in 25ns (typical, top gate). This drive capability allows 15-20A DC load on the VDDQ supply. The VTT termination voltage is an internal sink/source linear regulator, which during S0 state receives its power from the VDDQ bus. It is capable of sourcing and sinking 2 Amps (max). The current limit on this pin is set to 3 Amps (typical).

Output Current and PCB layout

The current handling capacity of SC2616 depends upon the amount of heat the PC board can sink from the SC2616 thermal pad. (See mounting instructions). The PC board layout must take into consideration the high current paths, and ground returns for both the VDDQ and VTT supply pins. VTT, LGND, VDDQ, 5VCC and PGND traces must also be routed using wide traces to minimize power loss and heat in these traces, based on the current handling requirements.

S3 and S5 States

During S3 and S5 sleep states, the operation of the VDDQ and VTT supplies is governed by the internal sequencing logic in strict adherence with motherboard specifications. The timing diagram demonstrates the state of the controller, and each of the VDDQ and VTT supplies during S3 and S5 transitions. When S3 is low, the VDDQ supplies the “Suspend To RAM” current of 650 mA (min) to maintain the information in memory while in standby mode. The VTT termination voltage is not needed during this state, and is thus tri-stated during S3. Once S3 goes high, the VDDQ switcher recovers and takes control of the VDDQ supply voltage. When S5 and S3 are pulled low, all supplies shut down. The SS/EN pin must be pulled low (<0.3V) and high again to restart the SC2616. This can be achieved by cycling the input supplies, 5V and 12V since both supplies have to be higher than their UVLO thresholds for proper start-up.

Initial Conditions and Event Sequencing

The main switcher will start-up in Asynchronous Mode when the voltage on SS/EN pin is greater than ~0.3V. The SS/EN will go high only after the 5Vcc and 12Vcc are higher than their respective UVLO thresholds. The switcher achieves maximum duty cycle when SS/EN reaches 0.8V. When the SS/EN equals 1.25V, the synchronous FET will also be activated.

When the S5 and S3 go high for the first time, the VDDQ is supplied by the switcher, thus removing the burden of charging the output capacitors via the linear regulator. An internal latch guarantees that the supply goes through S0 state for the first time.

During a transition from S3 to S0, where the 5V and 12V rails and subsequently the SS/EN pin go high, the internal VDDQ standby supply will remain ”on” until SS/EN has reached 1V, at which point only the switcher is supplying VDDQ , andthe internal “power good” indicator goes high.

The “Memory” activity should be slaved off the “Power OK” signal from the Silver Box supply, and since the “Power OK” is asserted after all supplies are within close tolerance of their final values, the VDDQ switcher should have been running for some time before the memory is activated. This is true for typical SS/EN capacitor values (10nf to 220nf). Thus during transitions from S3 to S0, the concern that the VDDQ Standby supply may have to provide high currents before the switcher is activated is alleviated.

The logic inputs to S3 and S5 pins must be defined before application of power to the SC2616. This can be guaranteed by pulling up the S3 and S5 inputs to 5VStandby. If the chipset that asserts these signals is powered after the SC2616 powers up, and S3 and S5 are not pulled up, erroneous startup and operation can result.

Care must be taken not to exceed the maximum voltage/current specifications on to the interface supplying these signals. The pullup voltage and resistor must be chosen such that when high, the S3 and S5 do not “back drive”

Applications Information (Cont.)

the interface chipset (Southbridge, etc.) and the maximum voltage applied to these pins do not exceed the chipsets specifications. A separate lower pullup supply may be necessary to avoid damage to the chipset.

"Back Feeding" the Input Supply

When in S3 state, VDDQ is supplied by the linear regulator and current can flow back from the VDDQ supply through the body diode of the Top switching MOSFET to the 5V supply of the Silver Box, which is off during the S3 state. This in turn shorts out the VDDQ supply and is not desirable.

There are two approaches to avoiding this reverse current flow. One method is to place a MOSFET in series with the top switching MOSFET, but with the source and drain reversed. (see typical application circuit). The MOSFETs should be connected *with sources connected to each other*, to prevent Gate Source (Vgs) break-down in the even the inductor current flows in the negative direction, which subsequenstly can give rise to the switching (Phase) node voltage flying up to voltages higher than VGS_Breakdown.

The connection of the MOSFETs in this manner places the body diodes back to back, thus removing a current path from VDDQ supply back into the input power source.

Another way is to use the Instantly available ACPI controllers (such as Semtech SC1549). Such controllers serve to provide a 5V bus to the user, irrespective of the Status of S3 and S5 signals. Thus the 5V supply and the 5V Standby are multiplexed to provide an "always On" 5V to the VDDQ supply. Since the 5V supply is always greater than VDDQ, the back to back MOSFET connection is no longer necessary.

Current Limit

Current limit is implemented by sensing the VDDQ voltage If it falls to 60% off its nominal voltage, as sensed by the FB pin, the TG and BG pins are latched off and the switcher and the linear converters are shut down. To recover from the current limit condition, either the power rails, 5VCC or 12VCC have to be recycled, or the SS/EN pin must be pulled low and released to restart switcher operation.

Thermal Shutdown

There are three independent Thermal Shutdown protection circuits in the SC2616: the VDDQ linear regulator, the VTT source regulator, and the VTT sink regulator. If any of the three regulators' temperature rises above the threshold, that regulator will turn off independently, until the temperature falls below the thermal shutdown limit.

Applications Information (Cont.)

Compensation Components

Once the filter components have been determined, the compensation components can be calculated. The goal of compensation is to modify the frequency response characteristics of the error amplifier to ensure that the closed loop feedback system has the highest gain and bandwidth possible while maintaining stability.

A simplified stability criteria states that the open loop gain of the converter should fall through 0dB at 20dB/decade at a frequency no higher than 20-25% of the switching frequency.

This objective is most simply met by generating asymptotic bode plots of the small signal response of the various sections of the converter.

It is convenient to split the converter into two sections, the Error amp and compensation components being one section and the Modulator, output filter and divider being the other.

First calculate the DC Filter + Modulator + Divider gain. The DC filter gain is always 0dB, the Modulator gain is 19dB at 5V in and is proportional to Vin, so modulator gain at any input voltage is.

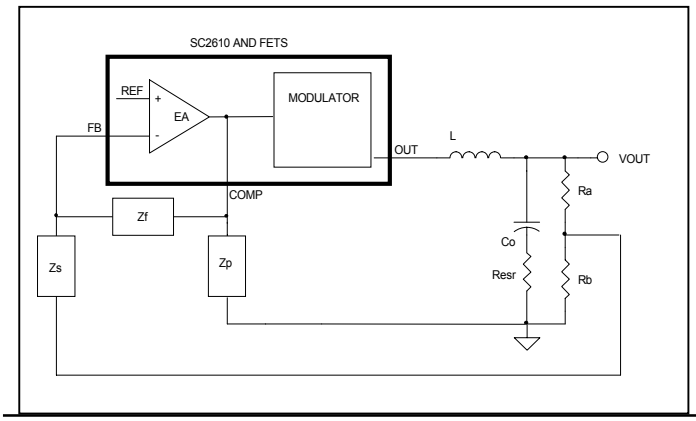
$$G_{MOD} = 19 + 20 \cdot Log\left(\frac{V_{IN}}{5}\right)$$

the divider gain is given by

$$G_{DIV} = 20 \cdot Log\left(\frac{R_B}{R_A + R_B}\right)$$

So the total Filter + Modulator + Divider DC Gain is

$$G_{FMD} = 19 + 20 \cdot Log\left(\frac{V_{IN}}{5}\right) + 20 \cdot Log\left(\frac{R_B}{R_A + R_B}\right)$$



Calculate the filter double pole frequency (Fp(lc))

$$Fp(lc) = \frac{1}{2\pi\sqrt{LCo}}$$

and calculate ESR Zero frequency (Fz(esr))

$$Fz(esr) = \frac{1}{2\pi \cdot Co \cdot Resr}$$

Choose an open loop crossover frequency (Fco) no higher than 20% of the switching frequency (Fs).

The proximity of Fz(esr) to the crossover frequency Fco determines the type of compensation required, if Fz(esr)>Fco/4, use type 3 compensation, otherwise use type 2. Type 1 compensation is not appropriate and is not discussed here.

Type 2 Example

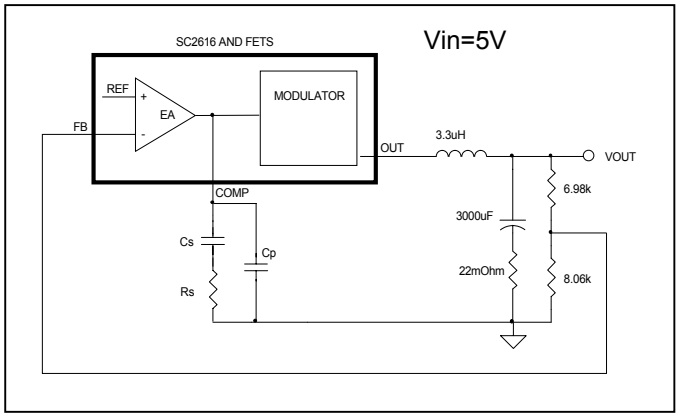
As an example of type 2 compensation, we will use the Evaluation board schematic.

The total Filter+Modulator+Divider DC Gain is:

$$G_{FMD} = 19 + 20 \cdot Log\left(\frac{5}{5}\right) + 20 \cdot Log\left(\frac{8.06}{6.98 + 8.06}\right) = 13.6dB$$

This is drawn as the line A-B in Figure 5.

$$Fp(lc) = \frac{1}{2\pi\sqrt{LCo}} = \frac{1}{2\pi\sqrt{3.3 \cdot 10^{-6} \cdot 3000 \cdot 10^{-6}}} \approx 1.6kHz$$



Applications Information (Cont.)

This is point B in Figure 5.

$$Fz(esr) = \frac{1}{2\pi \cdot 3000 \cdot 10^{-6} \cdot 22 \cdot 10^{-3}} = 2.4kHz$$

This is point C in Figure 5., the line joining B-C slopes at -40dB/decade, the line joining C-D slopes at -20dB/decade.

For 600kHz switching frequency, crossover is designed for 100kHz.

Since Fz(esr)<<Fco/4 Type 2 compensation is appropriate. Having plotted the line ABCD, and confirmed the type of compensation necessary, compensation component values can be determined.
At Fco, the line ABCD shows a gain of -27.5dB and a slope of -20dB/decade. In order for the total open loop gain to be 0dB with a -20dB/decade slope at this frequency, the compensated error amp gain at Fco must be +27.5dB with a 0dB slope. This is the line FG on the plot below.
Since open loop DC gain should be as high as possible to minimize errors, a zero is placed at F and to minimize high frequency gain and switching interference a pole is placed at G.

The zero at F should be no higher than Fco/4 and the pole at G no lower than 4*Fco. The equations to set the gain and the pole and zero locations allow Shutdown:

$$Rs = \frac{10^{\frac{A}{20}}}{gm} \text{ where } A = \text{gain at Fco (in dB)}$$

$$Cs = \frac{1}{2\pi \cdot Fz1 \cdot Rs}$$

$$Cp = \frac{1}{2\pi \cdot Fp1 \cdot Rs}$$

For this example, this results in the following values.

$$Rs = \frac{10^{\frac{27.5}{20}}}{0.8} = 29.6k\Omega \approx 30k\Omega$$

$$Cs \approx \frac{1}{6 \cdot 25 \cdot 10^{3} \cdot 30 \cdot 10^{3}} = 0.22nF$$

$$Cp \approx \frac{1}{6 \cdot 400 \cdot 10^{3} \cdot 30 \cdot 10^{3}} = 14pF \text{ (unecessary due to EA rolloff)}$$

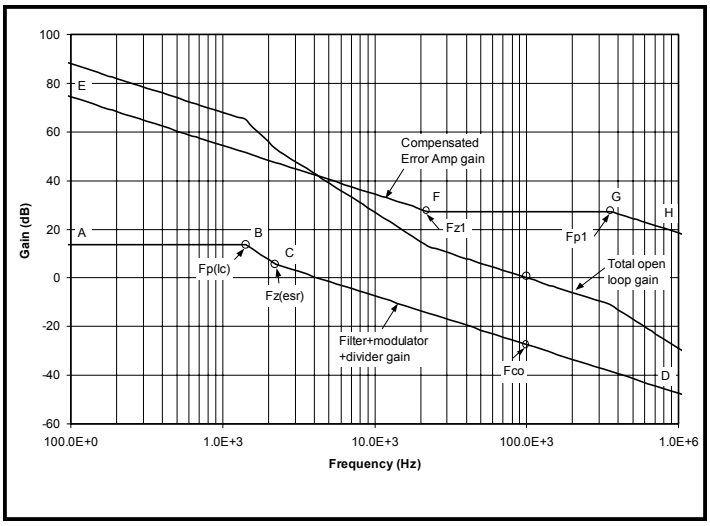


Figure 5: Type 2 Error Amplifier Compensation

Mounting Considerations

Description

The MLP18 is a leadless package whose electrical connections are made by lands on the bottom surface of the component. These lands are soldered directly to the PC board. The MLP has an exposed die attach pad, which enhances the thermal and electrical characteristics enabling high power applications. Power handling capability of the MLP package is typically >2x the power of other common SMT packages, such as the TSSOP and SOIC packages. In order to take full advantage of this feature the exposed pad must be physically connected to the PCB substrate with solder.

Thermal Pad Via Design

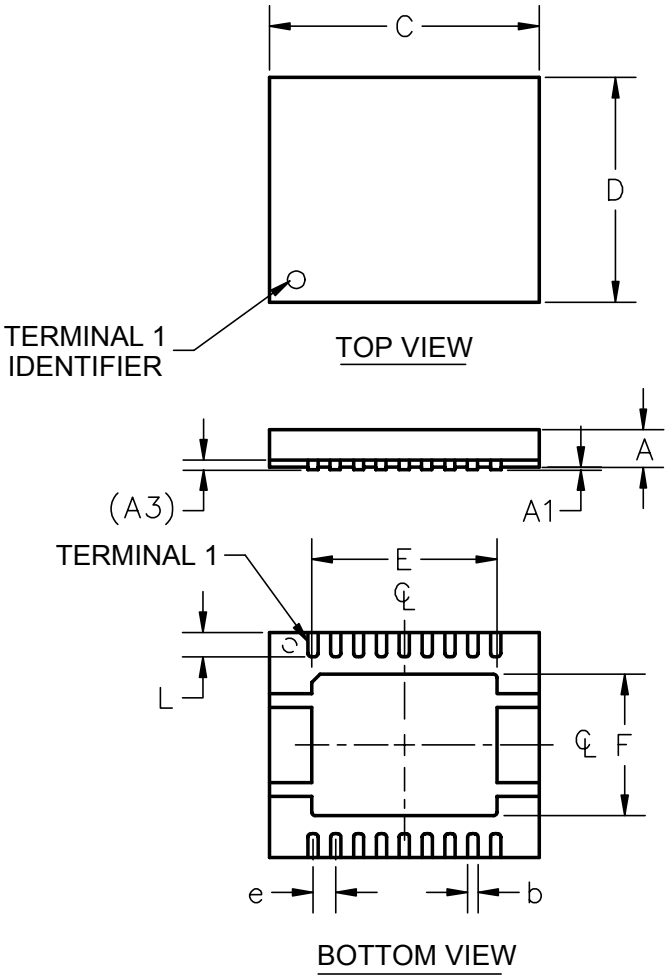
Thermal data for the MLP18 is based on a 4 layer PCB incorporating vias which act as the thermal path to other layers. (Ref: Jedec Specification JESD 51-5). Based on thermal performance, four-layer PCB's with vias are recommended to effectively remove heat from the device. Vias should be 0.3mm diameter on a 1.2mm pitch, and should be plugged to prevent voids being formed between the exposed pad and PCB thermal pad due to solder escaping by capillary action. Plugging can be accomplished by "tenting" the via during the solder mask process. The via solder mask diameter should be 100µm larger than the via diameter.

Two layer boards have less copper and thus typically require an increase in the PC board area for effective heatsinking. The copper area immdiately surrounding the thermal pad connection must not be interupted by routing traces.

Exposed Pad Stencil Design

It is good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination is difficult but the design of the exposed pad stencil is important, a single slotted rectangular pattern is recommended. (If large exposed pads are screened with excessive solder, the device may "float", thus causing a gap between the MLP terminal and the PCB land metalization.) The proposed stencil designs enables out-gassing of the solder paste during reflow as well as controlling the finished solder thickness.

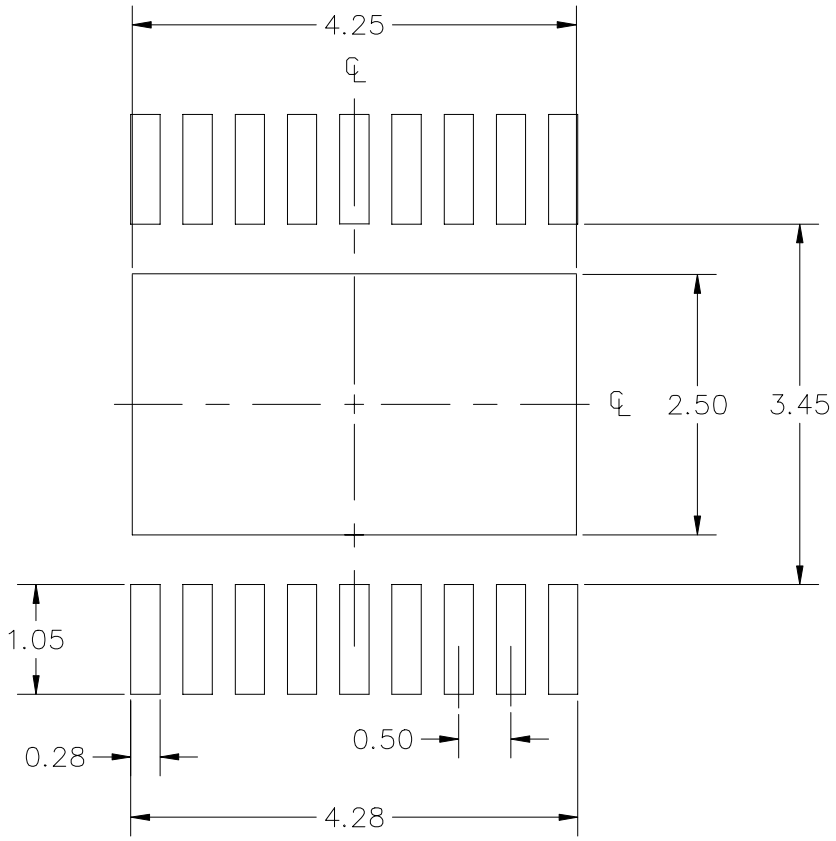
Outline Drawing - MLP-18



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.032	.039	0.80	1.00	–
A1	0	.002	0	0.05	–
A3	–	.008	–	0.20	REF
b	.007	.012	0.18	0.30	–
C	.236		6.00		NOM
D	.197		5.00		NOM
E	.157	.167	4.00	4.25	–
F	.118	.128	3.00	3.25	–
e	.020 BSC		0.50 BSC		–
L	.017	.026	0.45	0.65	–

[1] CONTROLLING DIMENSIONS: MILLIMETERS

Land Pattern - MLP-18



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