NEC Electronics Inc.

μPD42232
TRIPLE-PORT GRAPHICS BUFFER

PRELIMINARY INFORMATION

Description

The μPD42232 is a highly integrated triple-port graphics buffer specifically designed for graphics and image processing applications. The device is configured as 32K words by 8 bits with a serial input/output port and a dual port for random access. Asynchronous operation of the serial port allows the random access port to draw graphics while data is output serially. Serial input and output ports may be configured by 8, 4, 2, or 1 bit(s).

The random access port can be used to form a matrix frame buffer with coexistent 8-bit plane and 1-bit pixel operation. In plane operation, data across the screen in one plane (x and y dimension) is accessed. In pixel operation, data in multiple planes (z dimension) is accessed. In the matrix frame buffer architecture, selection of plane or pixel access is made in a special command cycle. Furthermore, a selectable open-drain connection allows the outputs to be wire-ORed.

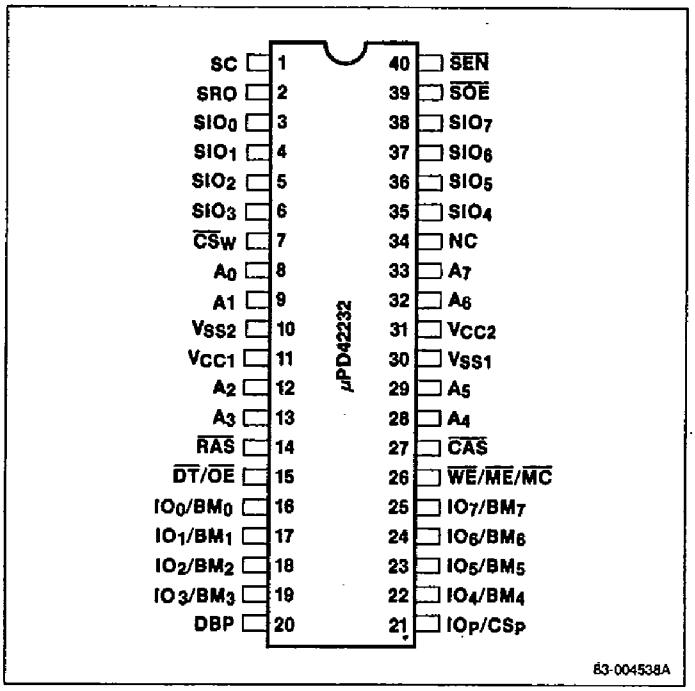
The μPD42232 supports 256 trinomial raster operations, as well as bit, chip or plane writing and reading. Refreshing is accomplished by means of $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and hidden refresh cycles. The device is packaged in a 600-mil, 40-pin plastic shrink DIP and a 400-mil, 40-pin plastic SOJ.

Features

- ☐ Triple-port organization
  - — 32K x 8-bit random access port
    - • 8-bit input/output port for plane access
    - • 1-bit input/output port for pixel access
  - — 128 x 8-bit serial input/output port
- ☐ Ten built-in registers
  - — 256 types of raster operations
  - — Random access of bit, chip, or plane data
  - — Compare function
- ☐ Each of 8 serial data registers configured as a split buffer, allowing for relaxed data transfer timing
- ☐ Bidirectional data transfer between random access storage array and serial data registers
- ☐ $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and hidden refreshing
- ☐ Serial port configuration by 8, 4, 2, or 1 bit(s)
- ☐ Selectable open-drain or three-state random access outputs
- ☐ Fully TTL-compatible inputs and outputs
- ☐ Standard 40-pin plastic shrink DIP and 40-pin plastic SOJ packaging

Pin Configurations

40-Pin Plastic DIP



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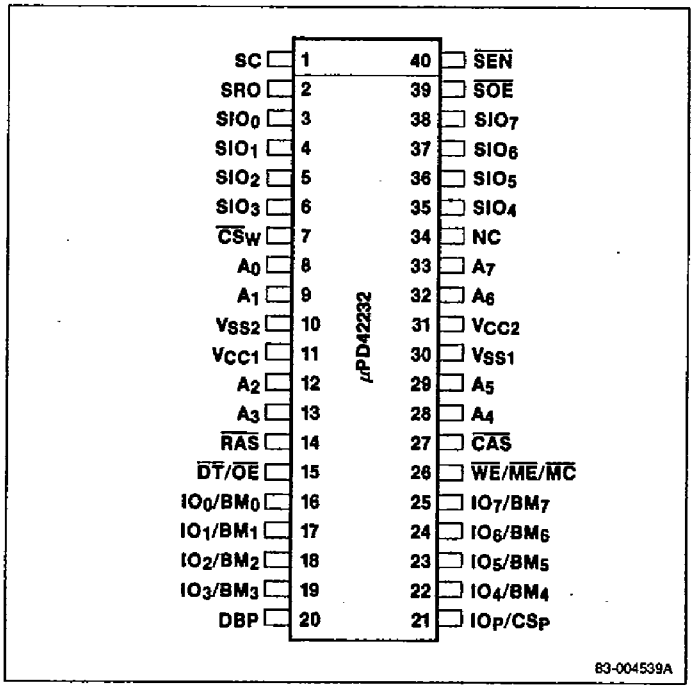
40-Pin Plastic SOJ



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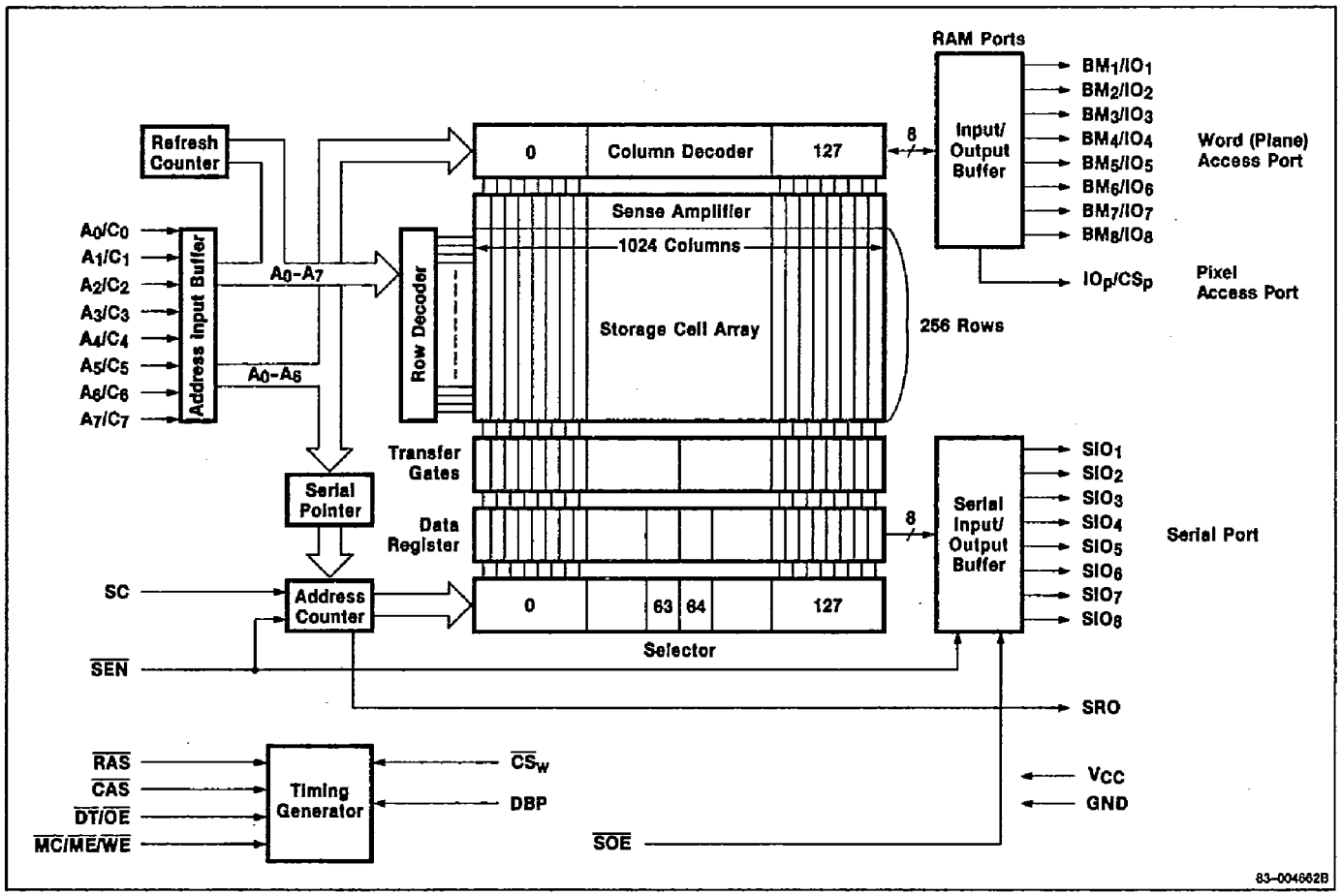
Ordering Information

Part Number	Random Write/Read Cycle Time (min)	Serial Write/Read Cycle Time (max)	$\overline{RAS}$ Access Time (max)	Package
μPD42232CU-12	220 ns	40 ns	120 ns	40-pin plastic shrink DIP
CU-15	260 ns	60 ns	150 ns	
μPD42232LA-12	220 ns	40 ns	120 ns	40-pin plastic SOJ
LA-15	260 ns	60 ns	150 ns	

Pin Identification

Symbol	Function
A_0/C_0-A_7/C_7	Address inputs/command code inputs
BM_0/IO_0-BM_7/IO_7	Bit mask inputs/plane data inputs and outputs
$\overline{CAS}$	Column address strobe
CS_P/IO_P	Chip select mask inputs/pixel data inputs and outputs
$\overline{CS_W}$	Chip select for random access port
DBP	Data bus precharge (selects open-drain output)
$\overline{DT/OE}$	Data transfer control/output enable
$\overline{RAS}$	Row address strobe
SC	Serial clock
$\overline{SEN}$	Serial port enable
SIO_0-SIO_7	Serial data inputs and outputs
$\overline{SOE}$	Serial output enable
SRO	Serial runout output
$\overline{WE}/\overline{ME}/\overline{MC}$	Write enable/mask enable/memory command
V_{SS1}/V_{SS2}	Ground
V_{CC1}/V_{CC2}	+5-volt power supply
NC	No connection

Block Diagram



Example of Matrix Frame Buffer Architecture

The following describes the configuration for an 8-plane, 512 x 512 dot matrix frame buffer using one μPD42232 per plane and an 8-bit CPU interface bus. As can be seen in figure 1, the IO_0 through IO_7 plane access ports on each μPD42232 are connected to DB_0 through DB_7 of the CPU interface bus. Pixel access port IO_P on the first μPD42232 is connected to DB_0. IO_P on the second μPD42232 is connected to DB_1 and so on.

This configuration supports two types of operation, either of which can be selected in a special command cycle:

- Plane—where 8 bits in the same plane are accessed
- Pixel—where 8 bits of the same pixel, 8 planes deep, are accessed

In plane operation, one plane is selected by means of the chip select or plane-mask function, causing the 8 bits of data specified by IO_0 through IO_7 to be accessed. In pixel operation, one pixel (8 bits) of data from the IO_P pin of each chip is accessed using the bit-mask function to select only one of the 8 bits at the specified address.

The example shown in figure 1, where one bit from each chip (plane) in a diagonal line is accessed (IO_O through IO_7), was chosen for the ease of explaining the pixel access function, which was developed to quickly change the color or shade of each pixel. In most applications, a single pixel at the same IO_X bit is updated. Since all eight chips are accessed simultaneously, a pixel update can be accomplished in one write cycle.

Split Buffer Configuration

A split buffer configuration is useful because it greatly relaxes the synchronization of timing between the random access and serial ports during data transfers, making it possible to design a video system where the serial port can be loaded at any time during the display or horizontal retrace period. Furthermore, the ability to perform serial register updates from the random access port during any part of the display time allows the size of the frame buffer to match CRT resolution, reducing the number of data transfers required and making more efficient use of video storage.

Item 1 of figure 2 shows the initial loading of both the lower (L) and upper (U) halves of the split buffer, which is required as part of the initialization sequence. Item 2 indicates that serial read cycles begin executing at location k and continue through location 63. The SRO serial runout pin goes high after locations 63 and 127. Items 3 and 4 show the beginning of serial reading in the right buffer (U), while the left (L) is being reloaded. Full asynchronous operation is provided by the simultaneous reading of one serial buffer while the opposite side is reloaded.

Logic Operation

The μPD42232 is equipped with a function that performs trinomial logic operation for each bit using the internal pattern and destination registers and write data input from the random access port as source data. To select this function, the raster operation code must be set by means of a special command cycle. Once set, it is retained until changed by another special command cycle. In a mask write cycle, this logic operation can be performed in 256 ways using the 8-bit raster operation code register.

The setup and execution of this logic operation takes five cycles (figure 3):

- Loading of pattern or destination register (1 cycle)
- Setting of raster operation code during memory command cycle
  - — Lower 4 bits (1 cycle)
  - — Upper 4 bits (1 cycle)
- Setting of raster operation enable function (1 cycle)
- Execution of raster operation by writing in the mask write cycle (1 cycle)

Figure 1. Pixel Access Using the Matrix Frame Buffer Architecture

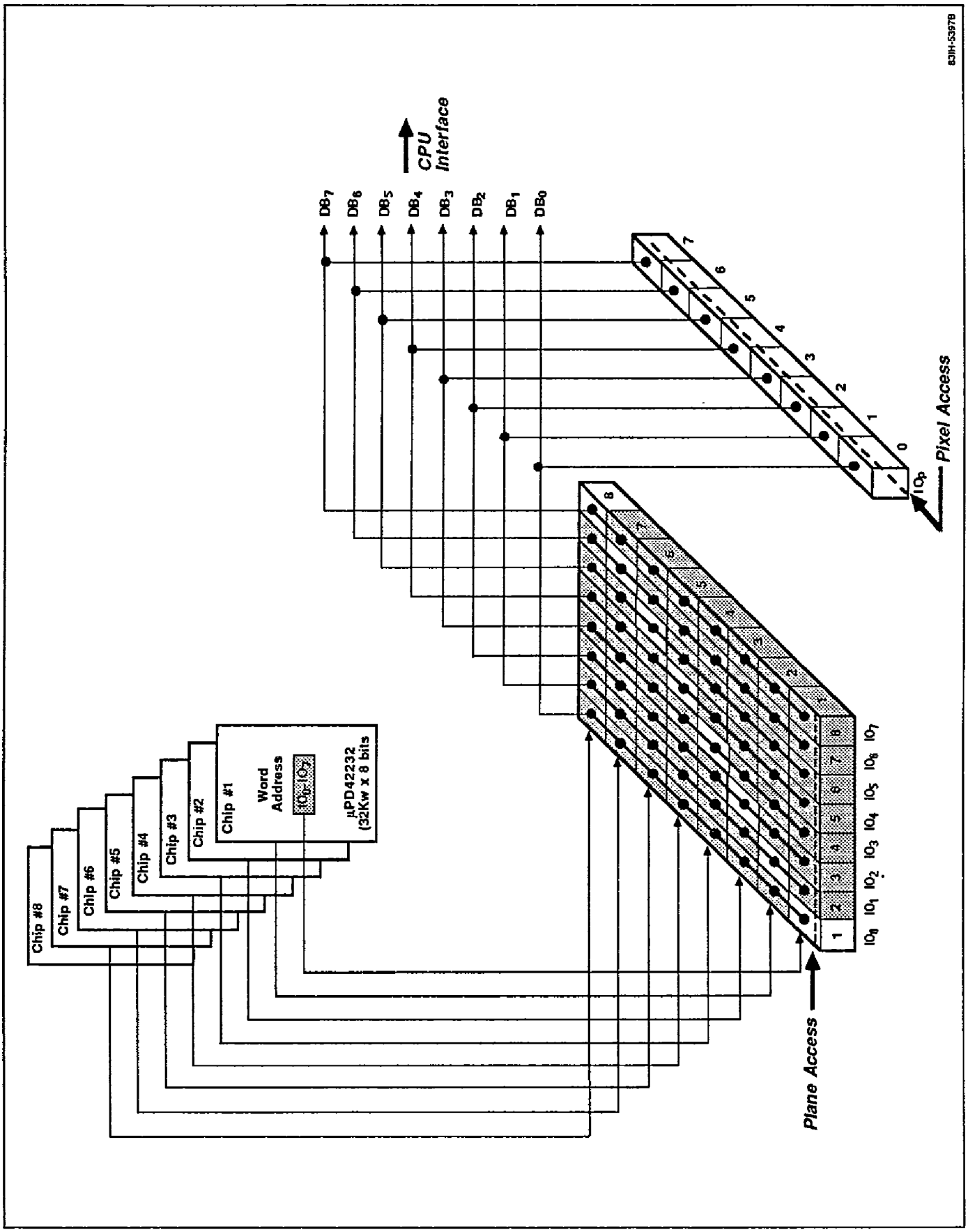


Figure 2. Serial Port Operation in Split Buffer Configuration

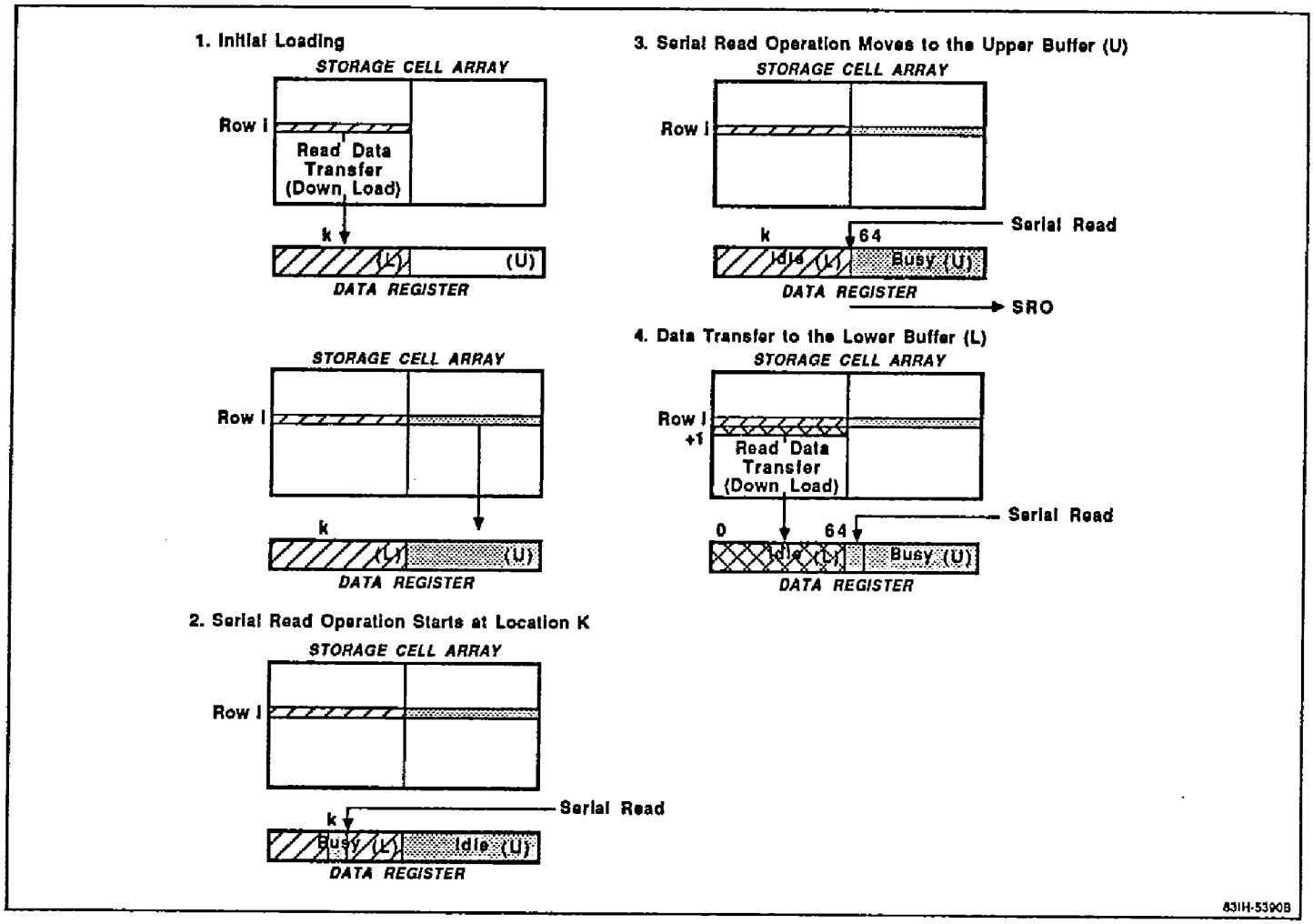


Figure 3. Logic Operation