

**MC34181,2,4**  
**MC35181,2,4**  
**MC33181,2,4**

**LOW POWER, HIGH SLEW RATE, WIDE BANDWIDTH,  
 JFET INPUT OPERATIONAL AMPLIFIERS**

Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4, MC35181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operate at 210  $\mu$ A per amplifier and offer 4.0 MHz of gain bandwidth product and 10 V/ $\mu$ s slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC33181/2/4, MC34181/2/4, MC35181/2/4 series of devices are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 210  $\mu$ A (Per Amplifier)
- Wide Supply Operating Range:  $\pm 1.5$  V to  $\pm 18$  V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/ $\mu$ s
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing:  $-14$  V to  $+14$  V (with  $\pm 15$  V Supplies)
- Large Capacitance Drive Capability: 0 to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection

**ORDERING INFORMATION**

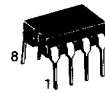
Op Amp Function	Device	Test Temperature Range	Package	
Single	MC34181P	0 to +70°C	Plastic DIP SO-8	
	MC34181D			
	MC33181P	-40 to +85°C	Plastic DIP SO-8	
	MC33181D			
	MC35181U	-55 to +125°C	Ceramic DIP	
Dual	MC34182P	0 to +70°C	Plastic DIP SO-8	
	MC34182D			
	MC33182P	-40 to +85°C	Plastic DIP SO-8	
	MC33182D			
	MC35182U	-55 to +125°C	Ceramic DIP	
Quad	MC34184P	0 to +70°C	Plastic DIP SO-14	
	MC34184D			
	MC33184P	-40 to +85°C	Plastic DIP SO-14	
	MC33184D			
		MC35184L	-55 to +125°C	Ceramic DIP

**LOW POWER  
 JFET INPUT  
 OPERATIONAL AMPLIFIERS**

**SILICON MONOLITHIC  
 INTEGRATED CIRCUITS**



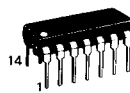
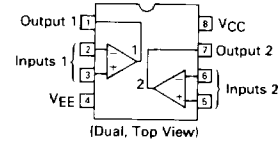
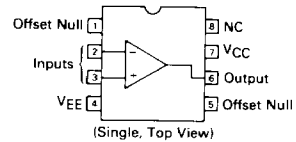
**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 626



**U SUFFIX**  
 CERAMIC PACKAGE  
 CASE 693



**D SUFFIX**  
 PLASTIC PACKAGE  
 CASE 751  
 (SO-8)



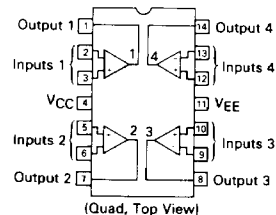
**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 646



**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 632



**D SUFFIX**  
 PLASTIC PACKAGE  
 CASE 751A  
 (SO-14)



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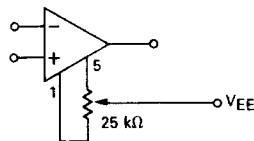
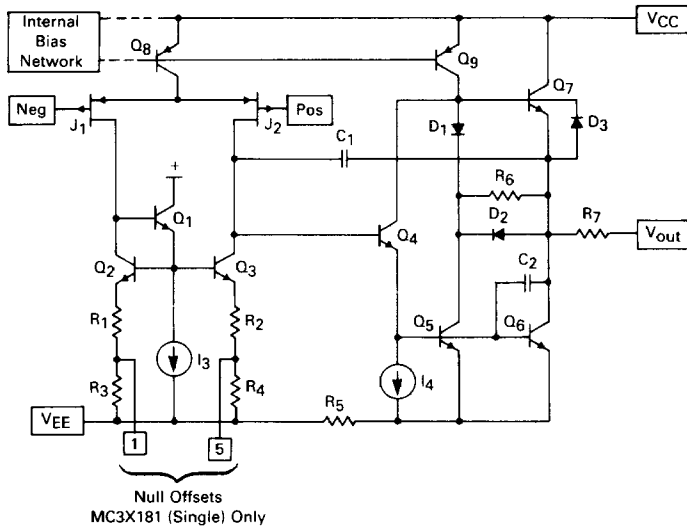
## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from $V_{CC}$ to $V_{EE}$ )	$V_S$	+36	Volts
Input Differential Voltage Range	$V_{IDR}$	Note 1	Volts
Input Voltage Range	$V_{IR}$	Note 1	Volts
Output Short-Circuit Duration (Note 2)	$t_S$	Indefinite	Seconds
Operating Junction Temperature	$T_J$	+160	°C
		+150	
Storage Temperature Range	$T_{stg}$	-65 to +160	°C
		-60 to +150	

### NOTES:

1. Either or both input voltages must not exceed the magnitude of  $V_{CC}$  or  $V_{EE}$ .
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_J$ ) is not exceeded (see Figure 1).

## EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)



MC3X181 Input Offset  
Voltage Null Circuit

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## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = +15 V, V<sub>EE</sub> = -15 V, T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R <sub>S</sub> = 50 Ω, V <sub>O</sub> = 0 V)	V <sub>IO</sub>				mV
Single					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = 0°C to +70°C (MC34181)					
T <sub>A</sub> = -40°C to +85°C (MC33181)					
T <sub>A</sub> = -55°C to +125°C (MC35181)					
Dual					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = 0°C to +70°C (MC34182)					
T <sub>A</sub> = -40°C to +85°C (MC33182)					
T <sub>A</sub> = -55°C to +125°C (MC35182)					
Quad					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = 0°C to +70°C (MC34184)					
T <sub>A</sub> = -40°C to +85°C (MC33184)					
T <sub>A</sub> = -55°C to +125°C (MC35184)					
Average Temperature Coefficient of V <sub>IO</sub> (R <sub>S</sub> = 50 Ω, V <sub>O</sub> = 0 V)	ΔV <sub>IO</sub> /ΔT	—	10	—	μV/°C
Input Offset Current (V <sub>CM</sub> = 0 V, V <sub>O</sub> = 0 V)	I <sub>IO</sub>				nA
T <sub>A</sub> = +25°C					
T <sub>A</sub> = 0°C to +70°C					
T <sub>A</sub> = -40°C to +85°C					
T <sub>A</sub> = -55°C to +125°C					
Input Bias Current (V <sub>CM</sub> = 0 V, V <sub>O</sub> = 0 V)	I <sub>IB</sub>				nA
T <sub>A</sub> = +25°C					
T <sub>A</sub> = 0°C to +70°C					
T <sub>A</sub> = -40°C to +85°C					
T <sub>A</sub> = -55°C to +125°C					
Input Common Mode Voltage Range	V <sub>ICR</sub>	(V <sub>EE</sub> + 4.0 V) to (V <sub>CC</sub> - 2.0 V)			V
Large Signal Voltage Gain (R <sub>L</sub> = 10 kΩ, V <sub>O</sub> = ±10 V)	A <sub>VOL</sub>	25 15	60 —	— —	V/mV
T <sub>A</sub> = +25°C					
T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>					
Output Voltage Swing (V <sub>ID</sub> = 1.0 V, R <sub>L</sub> = 10 kΩ)	V <sub>O+</sub> V <sub>O-</sub>	+13.5 —	+14 -14	— -13.5	V
T <sub>A</sub> = +25°C					
Common Mode Rejection (R <sub>S</sub> = 50 Ω, V <sub>CM</sub> = V <sub>ICR</sub> , V <sub>O</sub> = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R <sub>S</sub> = 50 Ω, V <sub>CM</sub> = 0 V, V <sub>O</sub> = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V <sub>ID</sub> = 1.0 V, Output to Ground)	I <sub>SC</sub>	3.0 8.0	8.0 11	— —	mA
Source					
Sink					
Power Supply Current (No Load, V <sub>O</sub> = 0 V)	I <sub>D</sub>				μA
Single					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>					
Dual					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>					
Quad					
T <sub>A</sub> = +25°C					
T <sub>A</sub> = T <sub>low</sub> to T <sub>high</sub>					

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = +15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = +25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate ( $V_{in} = -10\text{ V to } +10\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ ) $A_V = +1.0$ $A_V = -1.0$	SR	7.0	10	—	$\text{V}/\mu\text{s}$
Settling Time ( $A_V = -1.0$ , $R_L = 10\text{ k}\Omega$ , $V_O = 0\text{ V to } +10\text{ V Step}$ ) To Within 0.10% To Within 0.01%	$t_s$	—	1.1	—	$\mu\text{s}$
Gain Bandwidth Product ( $f = 100\text{ kHz}$ )	GBW	3.0	4.0	—	MHz
Power Bandwidth ( $A_V = +1.0$ , $R_L = 10\text{ k}\Omega$ , $V_O = 20\text{ V}_{p-p}$ , THD = 5%)	$BW_p$	—	200	—	kHz
Phase Margin ( $-10\text{ V} < V_O < +10\text{ V}$ ) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	$\phi_m$	—	67	—	Degrees
Gain Margin ( $-10\text{ V} < V_O < +10\text{ V}$ ) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$	$A_m$	—	6.7	—	dB
Equivalent Input Noise Voltage $R_S = 100\ \Omega$ , $f = 1.0\text{ kHz}$	$e_n$	—	38	—	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 1.0\text{ kHz}$	$i_n$	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Differential Input Capacitance	$C_i$	—	3.0	—	pF
Differential Input Resistance	$R_i$	—	$10^{12}$	—	$\Omega$
Total Harmonic Distortion $A_V = 10$ , $R_L = 10\text{ k}\Omega$ , $2\text{ V}_{p-p} < V_O < 20\text{ V}_{p-p}$ , $f = 10\text{ kHz}$	THD	—	0.04	—	%
Channel Separation ( $R_L = 10\text{ k}\Omega$ , $-10\text{ V} < V_O < +10\text{ V}$ , $0\text{ Hz} < f < 10\text{ kHz}$ )	—	—	120	—	dB
Open-Loop Output Impedance ( $f = 1.0\text{ MHz}$ )	$ Z_o $	—	200	—	$\Omega$

FIGURE 1 — MAXIMUM POWER DISSIPATION versus TEMPERATURE FOR PACKAGE VARIATIONS

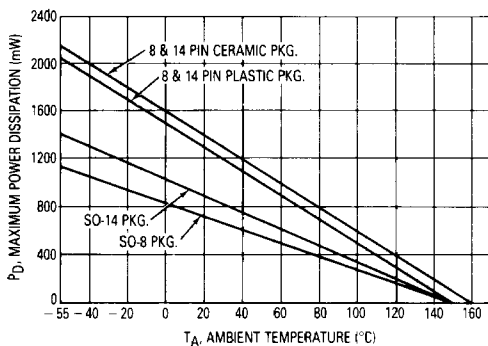
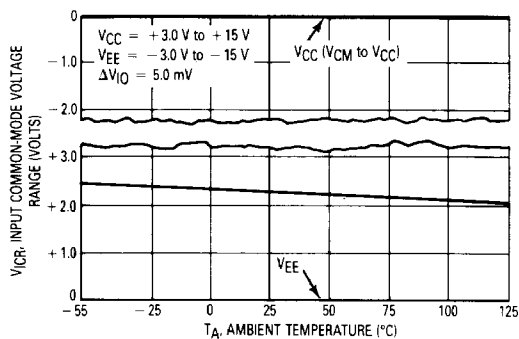
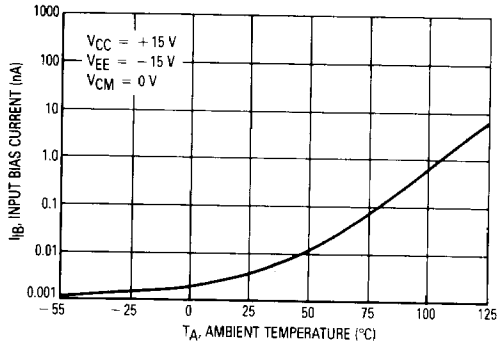


FIGURE 2 — INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

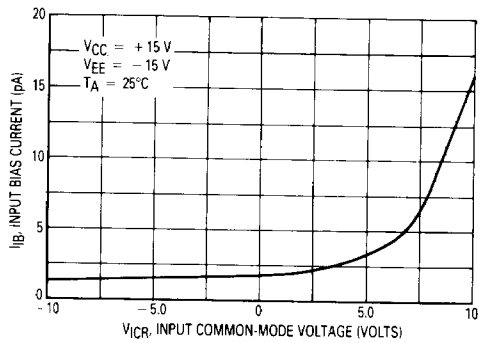


# MC34181,2,4, MC35181,2,4, MC33181,2,4

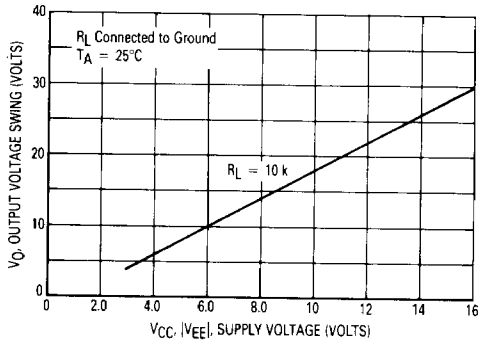
**FIGURE 3 — INPUT BIAS CURRENT versus TEMPERATURE**



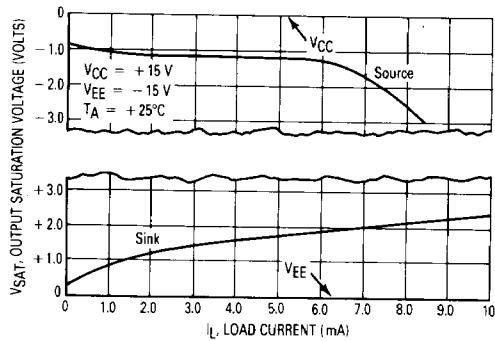
**FIGURE 4 — INPUT BIAS CURRENT versus INPUT COMMON-MODE VOLTAGE**



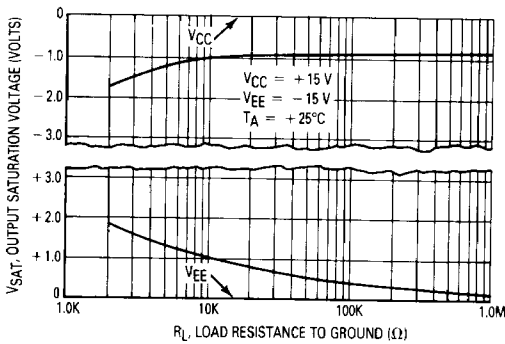
**FIGURE 5 — OUTPUT VOLTAGE SWING versus SUPPLY VOLTAGE**



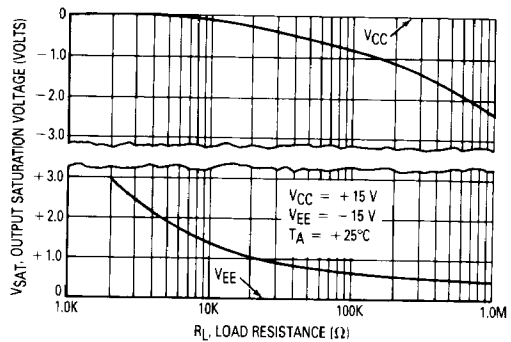
**FIGURE 6 — OUTPUT SATURATION VOLTAGE versus LOAD CURRENT**



**FIGURE 7 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO GROUND**

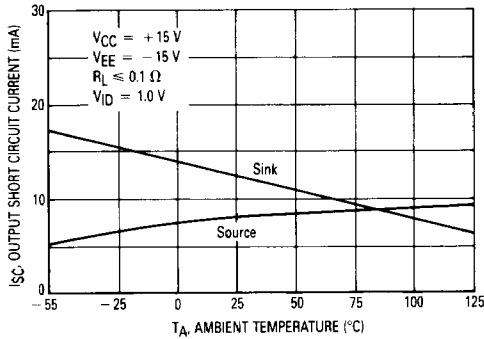


**FIGURE 8 — OUTPUT SATURATION VOLTAGE versus LOAD RESISTANCE TO  $V_{CC}$**

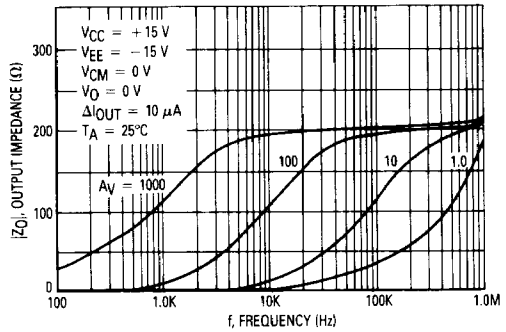


# MC34181,2,4, MC35181,2,4, MC33181,2,4

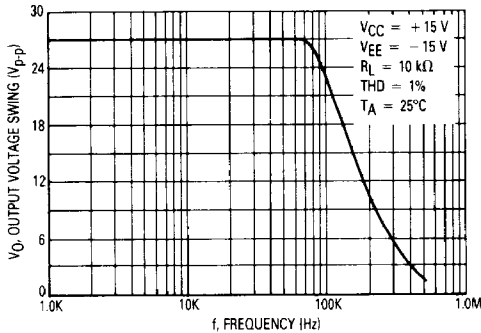
**FIGURE 9 — OUTPUT SHORT CIRCUIT CURRENT versus TEMPERATURE**



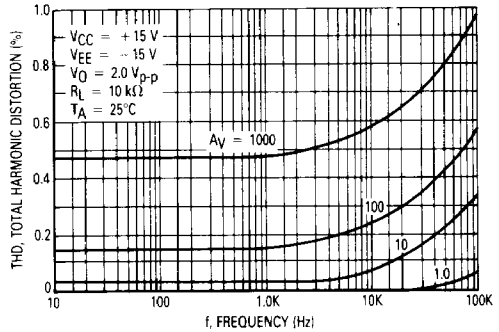
**FIGURE 10 — OUTPUT IMPEDANCE versus FREQUENCY**



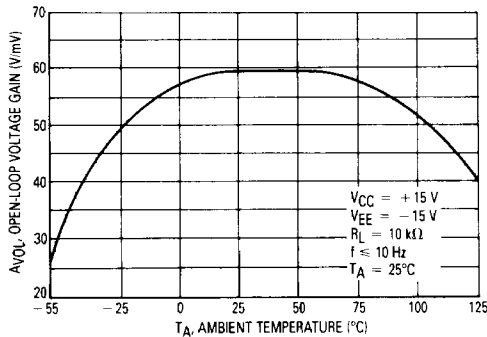
**FIGURE 11 — OUTPUT VOLTAGE SWING versus FREQUENCY**



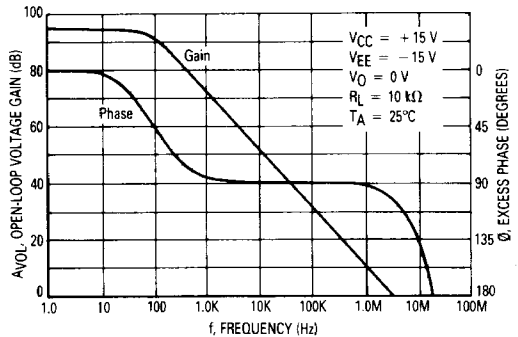
**FIGURE 12 — OUTPUT DISTORTION versus FREQUENCY**



**FIGURE 13 — OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE**

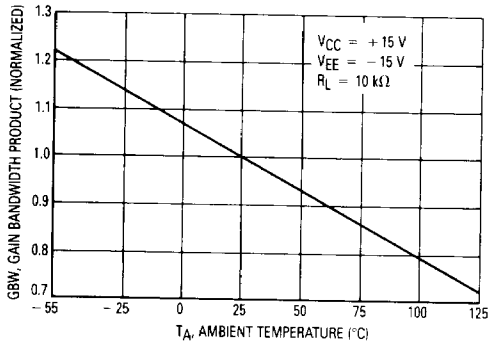


**FIGURE 14 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY**

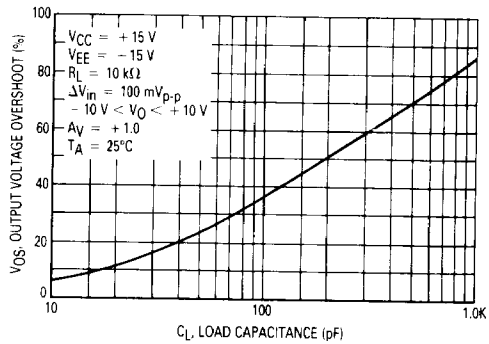


# MC34181,2,4, MC35181,2,4, MC33181,2,4

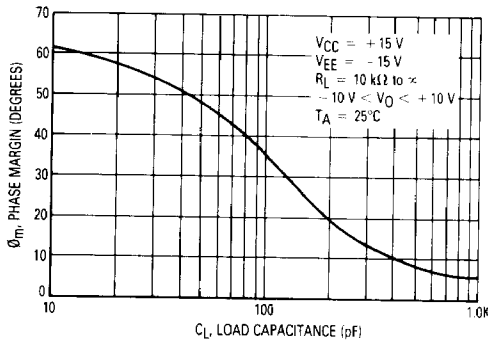
**FIGURE 15 — NORMALIZED GAIN BANDWIDTH PRODUCT versus TEMPERATURE**



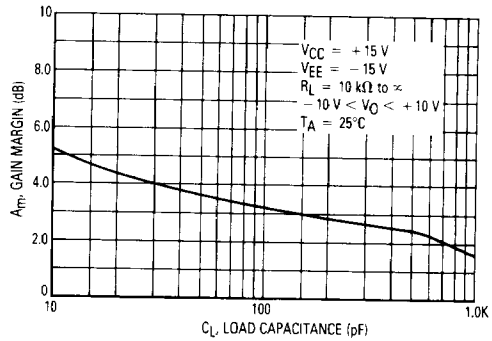
**FIGURE 16 — OUTPUT VOLTAGE OVERSHOOT versus LOAD CAPACITANCE**



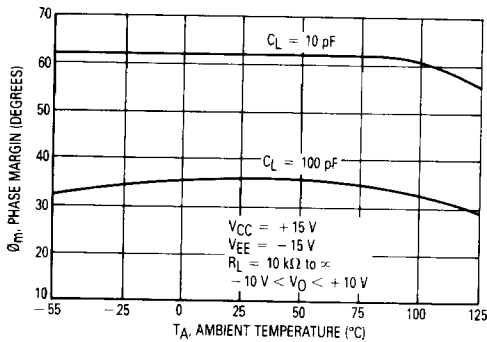
**FIGURE 17 — PHASE MARGIN versus LOAD CAPACITANCE**



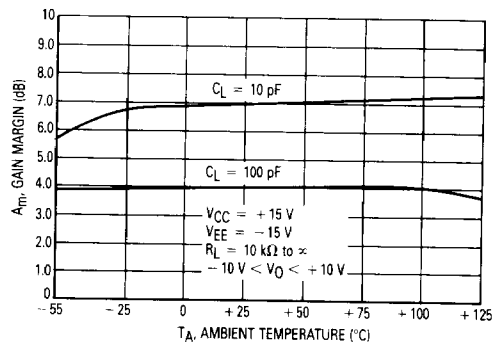
**FIGURE 18 — GAIN MARGIN versus LOAD CAPACITANCE**

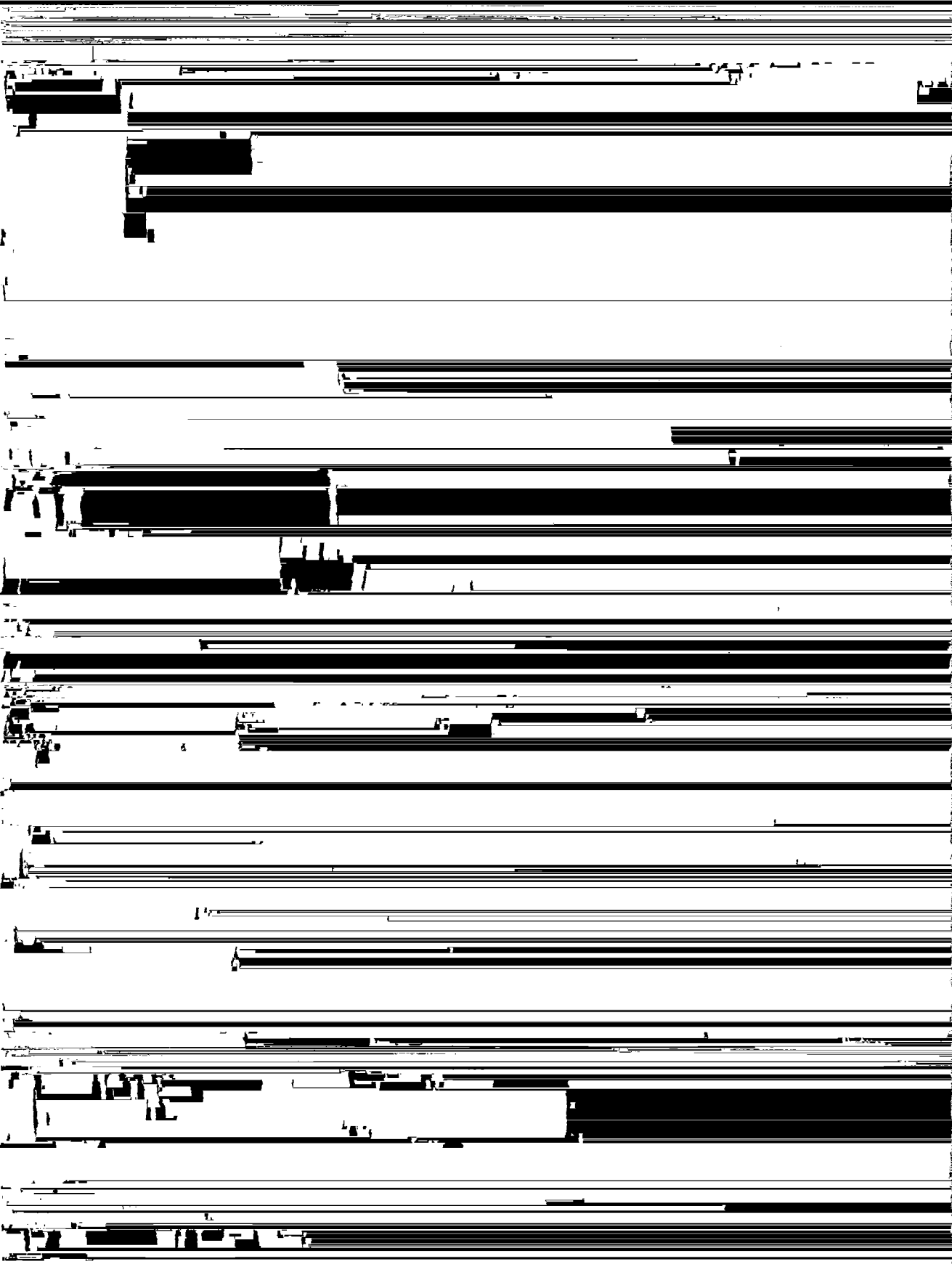


**FIGURE 19 — PHASE MARGIN versus TEMPERATURE**



**FIGURE 20 — GAIN MARGIN versus TEMPERATURE**







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FIGURE 27 — CHANNEL SEPARATION versus FREQUENCY

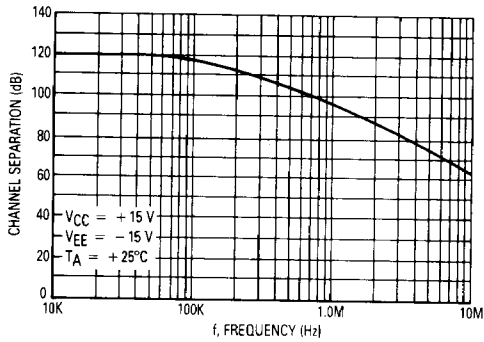


FIGURE 28 — TRANSIENT RESPONSE

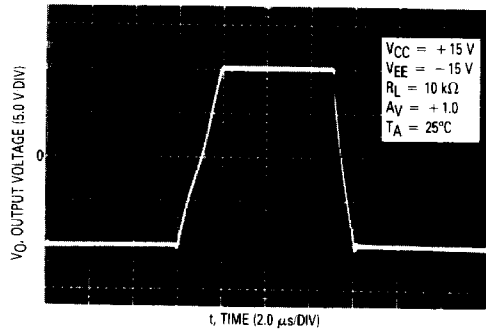
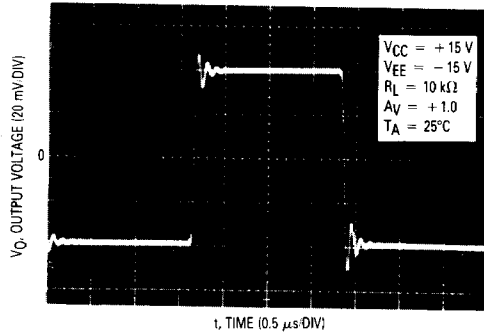


FIGURE 29 — SMALL SIGNAL TRANSIENT RESPONSE



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