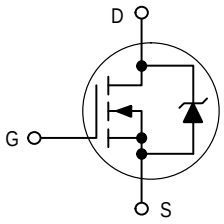
Product Preview

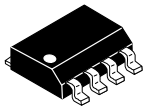
TMOS V™
SO-8 for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MMDF2N06V

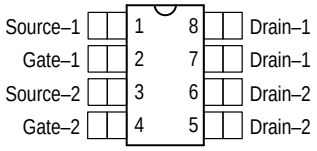
DUAL TMOS MOSFET
3.3 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.115 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 751–05, Style 11
SO–8



Top View

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage, (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.3 0.5 9.9	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.0	W
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.3 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	54	mJ
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

2N06V

(1) Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2N06V1	7″	12mm embossed tape	500
MMDF2N06V2	13″	12mm embossed tape	2500

This document contains information on a new product. Specifications and information herein are subject to change without notice.
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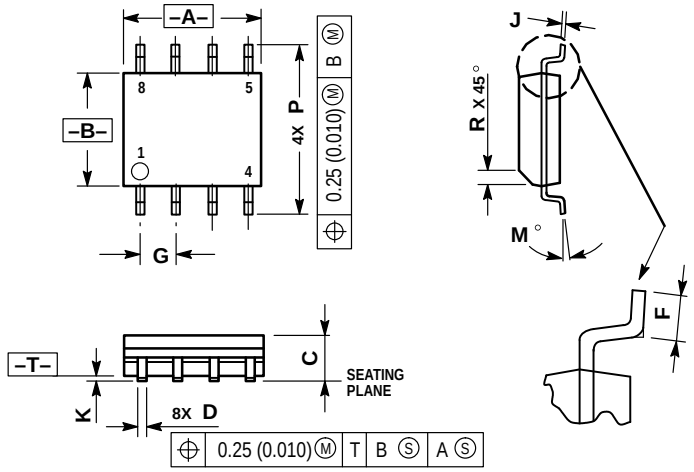
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	66	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.8	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.3 Adc)		$R_{DS(on)}$	—	0.106	0.115	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 3.3 Adc)		$V_{DS(on)}$	—	—	0.5	Vdc
(V_{GS} = 10 Vdc, I_D = 1.7 Adc, T_J = 150°C)			—	—	0.4	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.7 Adc)		g_{FS}	4.0	7.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	370	520	pF
Output Capacitance		C_{oss}	—	110	150	
Transfer Capacitance		C_{rss}	—	25	50	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 3.3 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	7.0	10	
Turn–Off Delay Time		$t_{d(off)}$	—	34	70	
Fall Time		t_f	—	18	40	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 3.3 Adc, V_{GS} = 10 Vdc)	Q_T	—	15	20	nC
		Q_1	—	3.0	—	
		Q_2	—	4.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 3.3 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.2	Vdc
	(I_S = 3.3 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.64	—	
Reverse Recovery Time	(I_S = 3.3 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	39	—	ns
		t_a	—	33	—	
		t_b	—	6.0	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.075	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0 °	7 °
P	5.80	6.20
R	0.25	0.50

CASE 751–05
SO–8
ISSUE P

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

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