

## NC7WZ240 TinyLogic™ UHS Dual Inverting Buffer with 3-STATE Outputs

### General Description

The NC7WZ240 is a Dual Inverting Buffer with independent active LOW enables for the 3-STATE outputs. The Ultra High Speed device is fabricated with advanced CMOS technology to achieve superior switching performance with high output drive while maintaining low static power dissipation over a broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65V to 5.5V  $V_{CC}$  operating range. The inputs and outputs are high impedance when  $V_{CC}$  is 0V. Inputs tolerate voltages up to 5.5V independent of  $V_{CC}$  operating range. Outputs tolerate voltages above  $V_{CC}$  when in the 3-STATE condition.

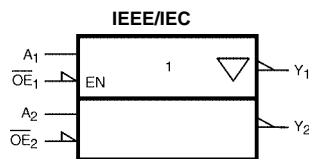
### Features

- Space saving US8 surface mount package
- Ultra High Speed;  $t_{PD}$  2.3 ns typ into 50 pF at 5V  $V_{CC}$
- High Output Drive;  $\pm 24$  mA at 3V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range; 1.65V–5.5V
- Matches the performance of LCX when operated at 3.3V  $V_{CC}$
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Outputs are overvoltage tolerant in 3-STATE mode
- Patented noise/EMI reduction circuitry implemented

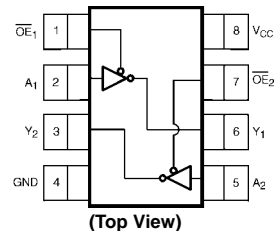
### Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ240K8X	MAB08A	WZ40	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Enable Inputs for 3-STATE Outputs
$A_n$	Inputs
$Y_n$	3-STATE Outputs

### Function Table

Inputs		Output
$\overline{OE}$	$A_n$	$Y_n$
L	L	H
L	H	L
H	L	Z
H	H	Z

H = HIGH Logic Level  
L = LOW Logic Level  
Z = 3-STATE

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Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 3)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage Operating ( $V_{CC}$ )	1.65V to 5.5V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V	Supply Voltage Data Retention ( $V_{CC}$ )	1.5V to 5.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to +7.0V	Input Voltage ( $V_{IN}$ )	0V to 5.5V
DC Input Diode Current ( $I_{IK}$ )		Output Voltage ( $V_{OUT}$ )	
@ $V_{IN} < 0V$	-50 mA	Active State	0V to $V_{CC}$
DC Output Diode Current ( $I_{OK}$ )		3-STATE	0V to 5.5V
@ $V_{OUT} < 0V$	-50 mA	Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Source/Sink Current ( $I_{OUT}$ )	± 50 mA	Input Rise and Fall Time ( $t_r, t_f$ )	
DC $V_{CC}$ /Ground Current ( $I_{CC}/I_{GND}$ )	± 100 mA	$V_{CC}$ @ 1.8V, 0.15V, 2.5V ± 0.2V	0 ns/V to 20 ns/V
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	$V_{CC}$ @ 3.3V ± 0.3V	0 ns/V to 10 ns/V
Junction Lead Temperature under Bias ( $T_J$ )	+150°C	$V_{CC}$ @ 5.0V ± 0.5V	0 ns/V to 5 ns/V
Junction Lead Temperature ( $T_L$ )		Thermal Resistance ( $\theta_{JA}$ )	250°C/W
(Soldering, 10 seconds)	+260°C		
Power Dissipation ( $P_D$ ) @ +85°C	250 mW		

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

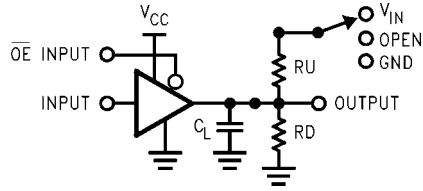
**Note 3:** Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	1.65-1.95 2.3-5.5	0.75 $V_{CC}$ 0.7 $V_{CC}$			0.75 $V_{CC}$ 0.7 $V_{CC}$		V	
$V_{IL}$	LOW Level Input Voltage	1.65-1.95 2.3-5.5		0.25 $V_{CC}$ 0.3 $V_{CC}$		0.25 $V_{CC}$ 0.3 $V_{CC}$		V	
$V_{OH}$	HIGH Level Output Voltage	1.65 2.3 3.0 4.5	1.55 2.2 2.9 4.4	1.65 2.3 3.0 4.5		1.55 2.2 2.9 4.4		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -100 \mu\text{A}$
		1.65 2.3 3.0 4.5	1.29 1.9 2.4 3.8	1.52 2.15 2.80 4.20		1.29 1.9 2.4 3.8		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ $I_{OH} = -16 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$
$V_{OL}$	LOW Level Output Voltage	1.65 2.3 3.0 4.5		0.0 0.0 0.0 0.0		0.10 0.10 0.10 0.10		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 100 \mu\text{A}$
		1.65 2.3 3.0 4.5		0.08 0.10 0.15 0.22	0.24 0.3 0.4 0.55		0.24 0.3 0.4 0.55		V
$I_{IN}$	Input Leakage Current	0-5.5			±0.1		±1	μA	$V_{IN} = 5.5V, \text{GND}$
$I_{OZ}$	3-STATE Output Leakage	1.65-5.5			±0.5		±5	μA	$V_{IN} = V_{IH}$ or $V_{IL}$ $0 \leq V_{OUT} \leq 5.5V$
$I_{OFF}$	Power Off Leakage Current	0.0			1		10	μA	$V_{IN}$ or $V_{OUT} = 5.5V$
$I_{CC}$	Quiescent Supply Current	1.65-5.5			1		10	μA	$V_{IN} = 5.5V, \text{GND}$

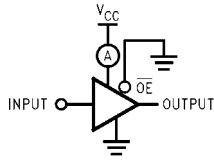
Noise Characteristics										
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		Units	Conditions				
			Typ	Max						
V <sub>OLP</sub> (Note 4)	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0		1.0	V	C <sub>L</sub> = 50 pF				
V <sub>OLV</sub> (Note 4)	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0		1.0	V	C <sub>L</sub> = 50 pF				
V <sub>OHV</sub> (Note 4)	Quiet Output Minimum Dynamic V <sub>OH</sub>	5.0		4.0	V	C <sub>L</sub> = 50 pF				
V <sub>IHD</sub> (Note 4)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C <sub>L</sub> = 50 pF				
V <sub>ILD</sub> (Note 4)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C <sub>L</sub> = 50 pF				
<b>Note 4:</b> Parameter guaranteed by design.										
AC Electrical Characteristics										
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to Y <sub>n</sub>	1.8 ± 0.15	2.0		12.0	2.0	13.0	ns	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S1 = Open	Figures 1, 3
		2.5 ± 0.2	1.0		7.5	1.0	8.0			
		3.3 ± 0.3	0.8		5.2	0.8	5.5			
		5.0 ± 0.5	0.5		4.5	0.5	4.8			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> to Y <sub>n</sub>	3.3 ± 0.3	1.2		5.7	1.2	6.0	ns	C <sub>L</sub> = 50 pF R <sub>D</sub> = 500Ω S1 = Open	Figures 1, 3
		5.0 ± 0.5	0.8		5.0	0.8	5.3			
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew (Note 5)	3.3 ± 0.3			1.0		1.0	ns	C <sub>L</sub> = 50 pF R <sub>D</sub> = 500Ω S1 = Open	Figures 1, 3
		5.0 ± 0.5			0.8		0.8			
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.8 ± 0.15	3.0		14.0	3.0	15.0	ns	C <sub>L</sub> = 50 pF R <sub>D</sub> , R <sub>U</sub> = 500 Ω S1 = GND for t <sub>PZH</sub> S1 = V <sub>I</sub> for t <sub>PZL</sub> V <sub>I</sub> = 2 x V <sub>CC</sub>	Figures 1, 3
		2.5 ± 0.2	1.8		8.5	1.8	9.0			
		3.3 ± 0.3	1.2		6.2	1.2	6.5			
		5.5 ± 0.5	0.8		5.5	0.8	5.8			
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.8 ± 0.15	2.5		12.0	2.5	13.0	ns	C <sub>L</sub> = 50 pF R <sub>D</sub> , R <sub>U</sub> = 500 Ω S1 = GND for t <sub>PZH</sub> S1 = V <sub>I</sub> for t <sub>PZL</sub> V <sub>I</sub> = 2 x V <sub>CC</sub>	Figures 1, 3
		2.5 ± 0.2	1.5		8.0	1.5	8.5			
		3.3 ± 0.3	0.8		5.7	0.8	6.0			
		5.0 ± 0.5	0.3		4.7	0.3	5.0			
C <sub>IN</sub>	Input Capacitance	0		2.5				pF		
C <sub>OUT</sub>	Output Capacitance	5.0		4				pF		
C <sub>PD</sub>	Power Dissipation Capacitance	3.3		10				pF	(Note 6)	Figure 2
		5.0		12				pF		
<b>Note 5:</b> Parameter guaranteed by design. t <sub>OSLH</sub> =  t <sub>PLHmax</sub> - t <sub>PLHmin</sub>  ; t <sub>OSHL</sub> =  t <sub>PHLmax</sub> - t <sub>PHLmin</sub>  .										
<b>Note 6:</b> C <sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I <sub>CCD</sub> ) at no output loading and operating at 50% duty cycle. (See Figure 2.) C <sub>PD</sub> is related to I <sub>CCD</sub> dynamic operating current by the expression: I <sub>CCD</sub> = (C <sub>PD</sub> )(V <sub>CC</sub> )(f <sub>IN</sub> ) + (I <sub>CCstatic</sub> ).										

**AC Loading and Waveforms**



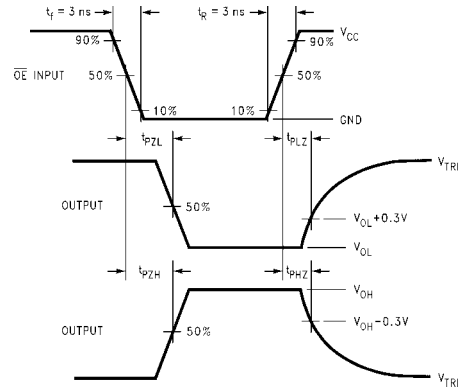
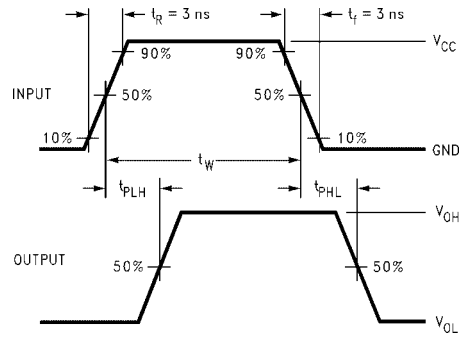
$C_L$  includes load and stray capacitance  
 Input PRR = 1.0 MHz;  $t_w = 500$  ns

**FIGURE 1. AC Test Circuit**



Input = AC Waveform;  $t_r = t_f = 1.8$  ns;  
 PRR = 10 MHz; Duty Cycle = 50%

**FIGURE 2.  $I_{CCD}$  Test Circuit**



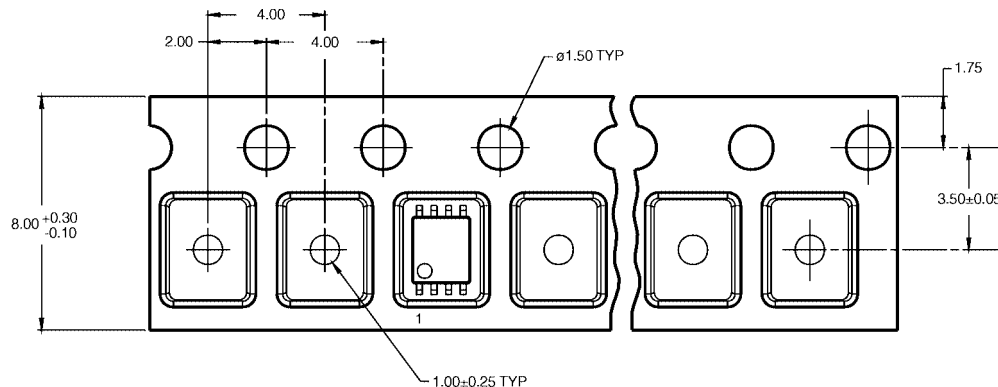
**FIGURE 3. AC Waveforms**

## Tape and Reel Specification

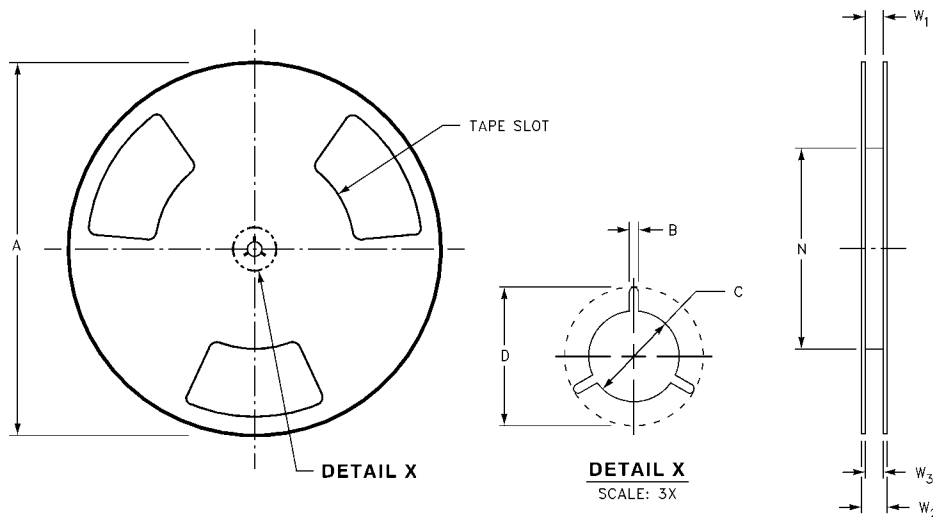
### Tape Format

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)

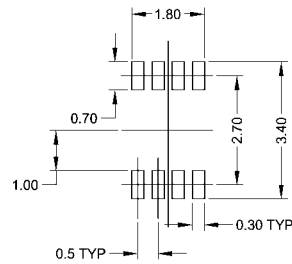
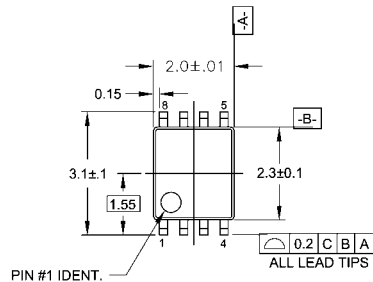


### REEL DIMENSIONS inches (millimeters)

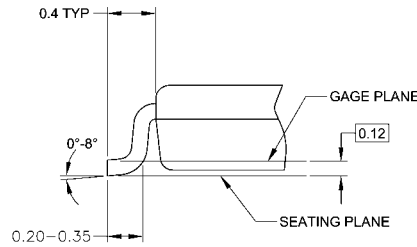
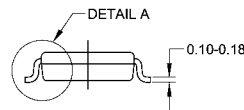
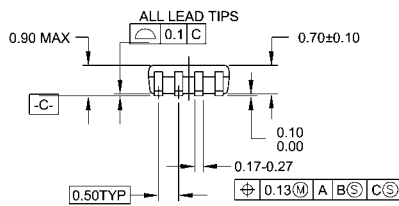


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

**Physical Dimensions** inches (millimeters) unless otherwise noted



**LAND PATTERN RECOMMENDATION**



**DETAIL A**

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide  
Package Number MAB08A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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