# ■ MN102H730F , MN102H73G , MN102H73K

MN102H730F	MN102H73G (under development)	MN102H73K (under development)		
External	128 K	256 K		
10 K	10 K	12 K		
TQFP128-P-1414B *Lead-free	TQFP128-P-1414A *Lead-free			
With main clock operated 58 ns (at 3.0 V to 3.6 V, 34 MHz)				
• RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B • ATC ch.0 to 1 transfer finish • ETC ch.0 to 1 transfer finish • External 0 to 7 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • A/D conversion finish				
Timer counter 0 : 8-bit × 1	/2 of system alook (POSC) frequency; p	nderflow of timer counter 9. TMOIO n		
S	ystem clock (BOSC)	nderflow of timer counter 8; I MolO p		
Interrupt source ······ u	nderflow of timer counter 0			
Timer counter 1 : 8-bit $\times$ 1				
		nderflow of timer counter 8; TM1IO p		
	-			
Timer counter 2 : 8-bit $\times$ 1				
		nderflow of timer counter 8; TM2IO J		
	-			
Timer counter 3 : 8-hit × 1				
Clock source 1/2 of system clock (BOSC) frequency; underflow of timer counter 8; TM3IO I				
	-			
•				
Clock source ····· 1		nderflow of timer counter 9; TM4IO p		
-				
Clock source ····· 1		nderflow of timer counter 9; TM5IO p		
•				
Clock source ····· 1		nderflow of timer counter 9; TM6IO p		
	•			
Clock source ····· 1	/2 of system clock (BOSC) frequency; u	nderflow of timer counter 9; TM7IO p		
	-			
Interrupt source u	-			
Interrupt source u Timer counter 8 : 8-bit × 1 Clock source 1	-			
	External	External  128 K  10 K  TQFP128-P-1414B *Lead-free  TQFP128  With main clock operated  58 ns (at 3.0 V to 3.6 V, 34 MHz)  • RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture A • Timer counter 0 to 9 underflow • Timer counter 0 : 8-bit × 1  Clock source		

### MN102H730F , MN102H73G , MN102H73K $\square$

Timer Counte	r (Continue)	Timer counter 9: 8-bit × 1					
, ,		Clock source 1/2 of system clock (BOSC) frequency; 1/64 of system clock (BOSC) frequency					
		TM9IO pin; timer counter 8 output  Interrupt source underflow of timer counter 9					
		Timer counter 10: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)  Clock source					
		Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B					
		Timer counter 11: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)  Clock source					
		Timer counter 12: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)  Clock source					
		Interrupt sourceunderflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B					
		Timer counter 13: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)  Clock source					
		Timer counter 14: 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input)  Clock source					
Serial Interface	е	Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)  Clock source					
		Serial 2, 3: 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length)  Clock source					
		UART $\times$ 4 (common use with serial 0 to 3)					
		$I^2C \times 2$ (common use with serial 1,3; single master)					
Multiply-and-A	ccumulate	16-bit sign × 16-bit sign + 40-bit sign					
I/O Pins	I/O	Ommon use: 59 (use of full address, address data separate 16-bit mode)     Common use: 76 (use of address 16-bit, address data separate 8-bit mode)					
A/D Inputs		10-bit × 12-ch. (with S/H)					
D/A Outputs		$8$ -bit $\times$ $4$ -ch.					
PWM		16-bit × 5-ch. (timer counter 10 to 14)					
ICR		16-bit × 5-ch. (timer counter 10 to 14)					
OCR		16-bit × 5-ch. (timer counter 10 to 14)					
Notes		Address / data separate bus interface; 8 / 16-bit bus width selectable; burst ROM interface; SRAM interface					

See the next page for electrical characteristics, pin assignment and support tool.

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## **Electrical Characteristics**

#### Supply current

Parameter	Symbol	Symbol Condition		Limit		
	Symbol			typ	max	Unit
Operating supply current	IDDom	VI = VDD or VSS, output open			60+10α*	
	IDDopr	f = 34  MHz , $VDD = 3.3  V$		00+100.*		mA
Supply current at STOP	IDDS	Pin with pull-up resistor is open			70	
	מענו	all other input pins and Hi-Z state input/output		/0	μΑ	
Supply current at HALT	IDDH	pins are simultaneously applied VDD or VSS level	20 L 10 m		30+10α*	mA
	אטעו	f = 34  MHz, $VDD = 3.3  V$ , output open		30+100.**		

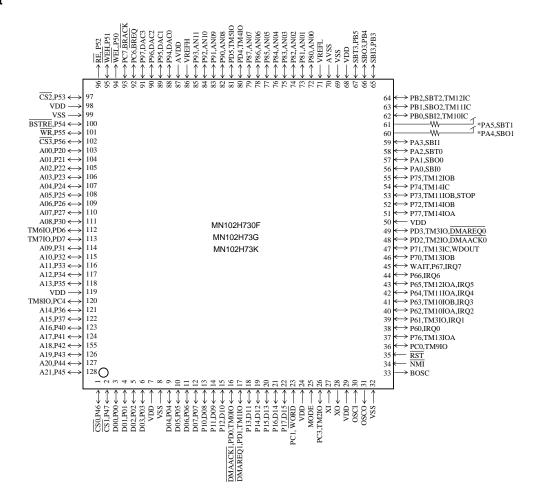
(Ta =  $-40^{\circ}$ C to  $+85^{\circ}$ C , VDD = AVDD = 3.3 V , VSS = AVSS = 0 V) \* " $\alpha$ " depends on products .

 $MN102H73G/73K/730F~\alpha=0$ 

MN102HF73G  $\alpha = 1$ 

MN102HF73K  $\alpha = 2$ 

#### Pin Assignment



#### Support Tool

In-circuit Emulator	PX-ICE102H73-128P1414		
Flash Memory Built-in Type	Type MN102HF73G (under development), MN102HF73K (under development)		
	ROM (× 8-bit)	128 K / 256 K	
	RAM (× 8-bit)	10 K / 12 K	
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)	
	Package	TQFP128-P-1414B *Lead-free	

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