1 PRODUCT OVERVIEW

OVERVIEW

The S3C72F5 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With an up-to-896-dot LCD direct drive capability, 8-bit and 16-bit timer/counter, and serial I/O, the S3C72F5 offers an excellent design solution for a wide variety of applications which require LCD functions.

Up to 39 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the S3C72F5's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The S3C72F5 microcontroller is also available in OTP (One Time Programmable) version, S3P72F5. S3P72F5 microcontroller has an on-chip 16K-byte one-time-programable EPROM instead of masked ROM. The S3P72F5 is comparable to S3C72F5, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 544 × 4-bit RAM (excluding LCD display RAM)
- 16,384 × 8-bit ROM

39 I/O Pins

- I/O: 35 pins
- Input only: 4 pins

LCD Controller/Driver

- 56 segments and 16 common terminals
- 8 and 16 common selectable
- Internal resistor circuit for LCD bias
- All dot can be switched on/off

8-bit Basic Timer

- 4 interval timer functions
- Watch-dog timer

8-bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider
- Serial I/O interface clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock frequency output
- External clock signal divider

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Memory-Mapped I/O Structure

- Data memory bank 15

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32768 Hz
- 4 frequency outputs to BUZ pin
- Clock source generation for LCD

Interrupts

- Four internal vectored interrupts
- Four external vectored interrupts
- Two quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main system oscillation stops)
- Subsystem clock stop mode

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 0.4 – 6 MHz
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6 MHz
- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 100-pin QFP

BLOCK DIAGRAM

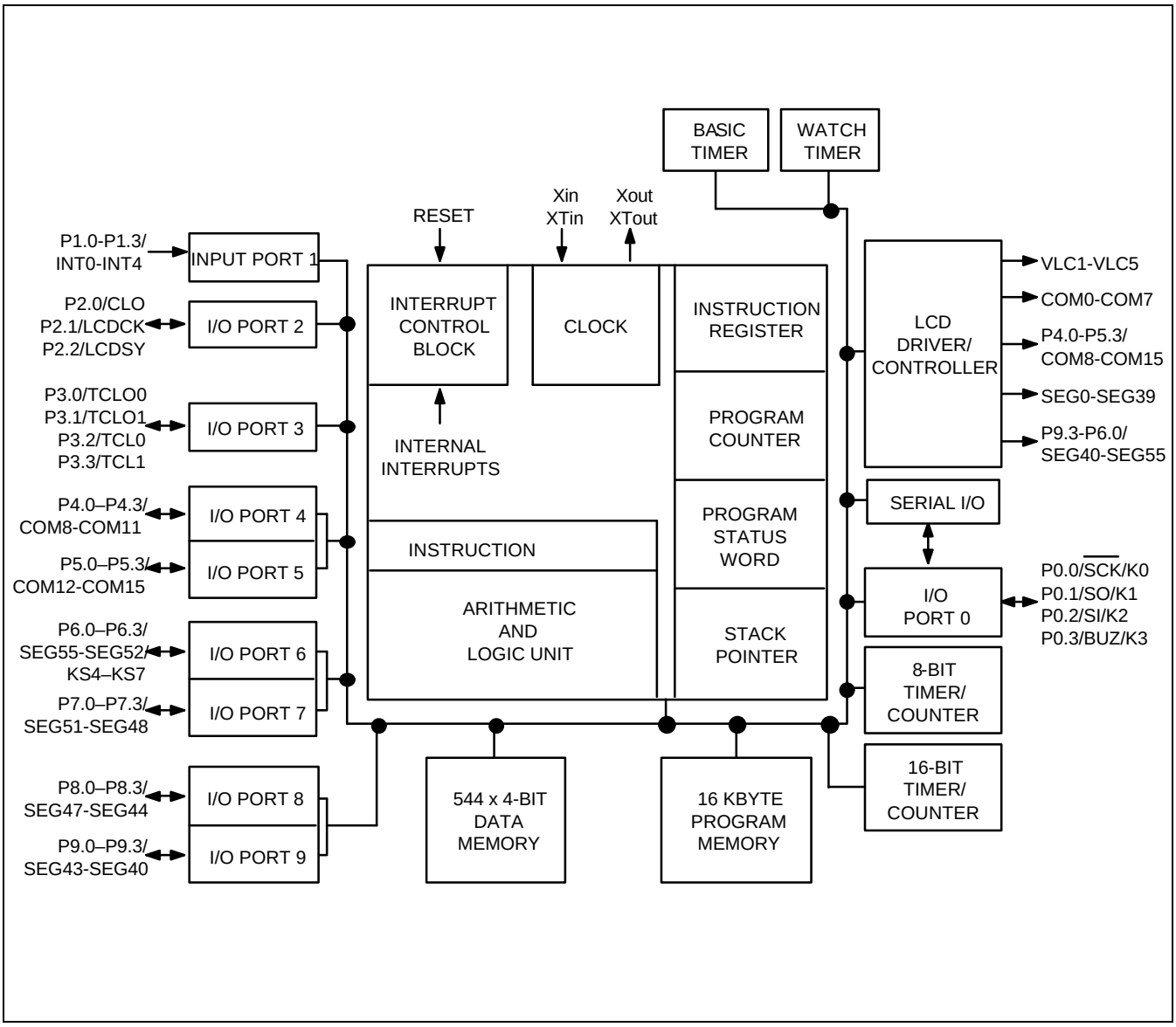


Figure 1-1. S3C72F5 Simplified Block Diagram

PIN ASSIGNMENTS

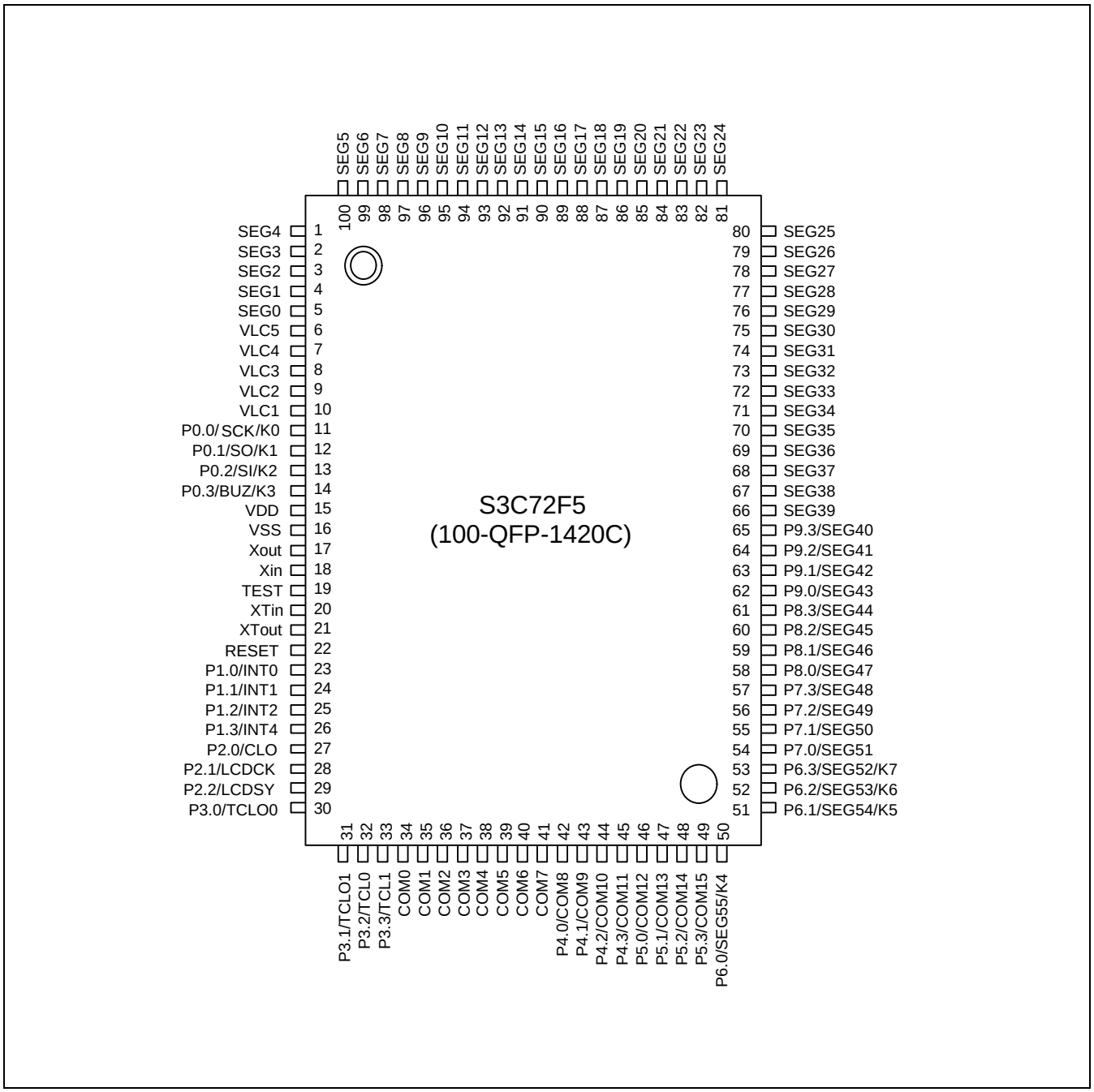


Figure 1-2. S3C72F5 100-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1–1. S3C72F5 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Individual pins are software configurable as input or output. Individual pins are software configurable as open-drain or push-pull output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	11 12 13 14	SCK/K0 SO/K1 SI/K2 BUZ/K3
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test are possible. 4-bit pull-up resistors are assignable by software.	23 24 25 26	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2	I/O	Same as port 0 except that port 2 is 3-bit I/O port.	27 28 29	CLO LCDCK LCDSY
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	30 31 32 33	TCLO0 TCLO1 TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-, 4-bit or 8-bit read/write and test are possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	42–45 46–49	COM8– COM11 COM12– COM15
P6.0–P6.3 P7.0–P7.3	I/O	Same as P4, P5.	50–53 54–57	SEG55/K4– SEG52/K7 SEG51– SEG48
P8.0–P8.3 P9.0–P9.3	I/O	Same as P4, P5.	58–61 62–65	SEG47– SEG44 SEG43– SEG40
SCK	I/O	Serial I/O interface clock signal.	11	P0.0/K0
SO	I/O	Serial data output.	12	P0.1/K1
SI	I/O	Serial data input.	13	P0.2/K2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz or 16 kHz frequency output for buzzer signal.	14	P0.3/K3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	23, 24	P1.0, P1.1

Table 1–1. S3C72F5 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
INT2	I	Quasi-interrupt with detection of rising or falling edges.	25	P1.2
INT4	I	External interrupt with detection of rising or falling edges.	26	P1.3
CLO	I/O	Clock output .	27	P2.0
LCDCK	I/O	LCD clock output for display expansion.	28	P2.1
LCDSY	I/O	LCD synchronization clock output for display expansion.	29	P2.2
TCLO0	I/O	Timer/counter 0 clock output.	30	P3.0
TCLO1	I/O	Timer/counter 1 clock output.	31	P3.1
TCL0	I/O	External clock input for timer/counter 0.	32	P3.2
TCL1	I/O	External clock input for timer/counter 1.	33	P3.3
COM0–COM7	O	LCD common signal output.	34–41	–
COM8–COM11	I/O		42–45	P4.0–P4.3
COM12–COM15			46–49	P5.0–P5.3
SEG0–SEG39	O	LCD segment signal output.	5–1, 100–66	–
SEG40–SEG43	I/O		65–62	P9.3–P9.0
SEG44–SEG47			61–58	P8.3–P8.0
SEG48–SEG51			57–54	P7.3–P7.0
SEG52–SEG55			53–50	P6.3/K7–P6.0/K4
K0–K3	I/O	External interrupt. The triggering edge is selectable.	11–14	P0.0–P0.3
K4–K7			50–53	P6.0–P6.3
V_{DD}	–	Main power supply.	15	–
V_{SS}	–	Ground.	16	–
RESET	I	Reset signal.	22	–
V_{LC1}–V_{LC5}	–	LCD power supply.	10–6	–
X_{in}, X_{out}	–	Crystal, Ceramic or RC oscillator pins for system clock.	18, 17	–
XT_{in}, XT_{out}	–	Crystal oscillator pins for subsystem clock.	20, 21	–
TEST	I	Test signal input. (must be connected to V_{SS})	19	–

NOTE: Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.

Table 1–2. Overview of S3C72F5 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.1, P0.3	SO/K1, BUZ/K3	I/O	Input	E-1
P0.0, P0.2	SCK/K0, SI/K2	I/O	Input	E-2
P1.0–P1.3	INT0–INT2, INT4	I	Input	A-3
P2.0–P2.2	CLO, LCDCK, LCDSY	I/O	Input	E
P3.0–P3.1	TCLO0, TCLO1	I/O	Input	E
P3.2–P3.3	TCL0, TCL1	I/O	Input	E-1
P4.0–P4.3 P5.0–P5.3	COM8–COM11 COM12–COM15	I/O	Input	H-13
P6.0–P6.3	SEG55/K4–SEG52/K7	I/O	Input	H-16
P7.0–P7.3	SEG51–SEG48	I/O	Input	H-13
P8.0–P8.3 P9.0–P9.3	SEG47–SEG44 SEG43–SEG40	I/O	Input	H-13
COM0–COM7	–	O	High	H-3
SEG0–SEG39	–	O	High	H-15
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	–	I	–	B
V_{LC1}–V_{LC5}	–	–	–	–
X_{in}, X_{out}	–	–	–	–
XT_{in}, XT_{out}	–	–	–	–
TEST	–	I	–	–

PIN CIRCUIT DIAGRAMS

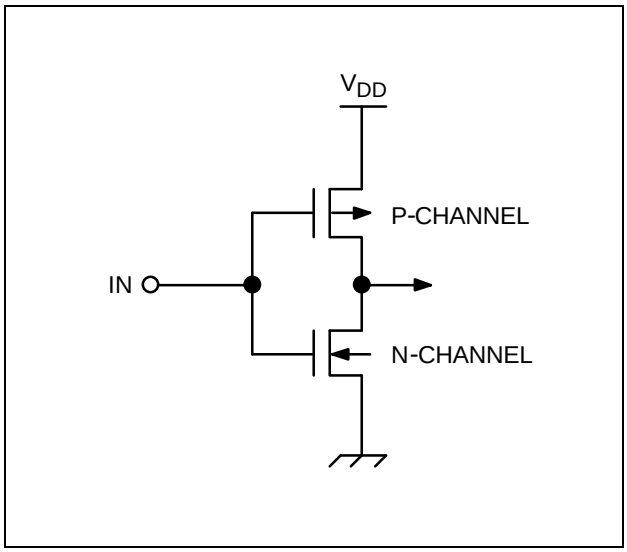


Figure 1-3. Pin Circuit Type A

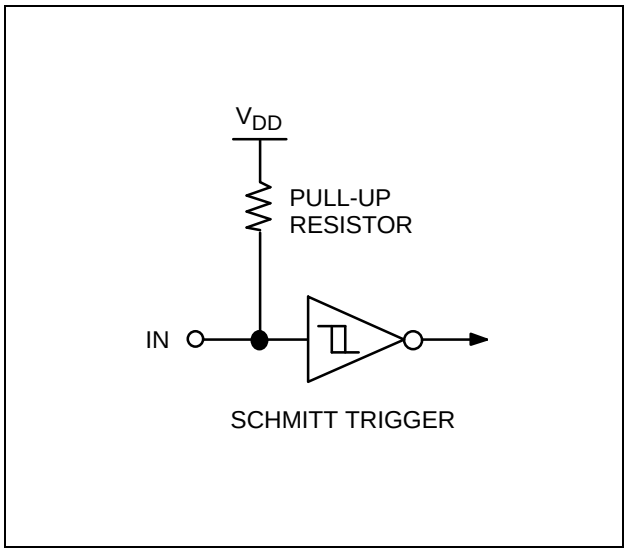


Figure 1-5. Pin Circuit Type B

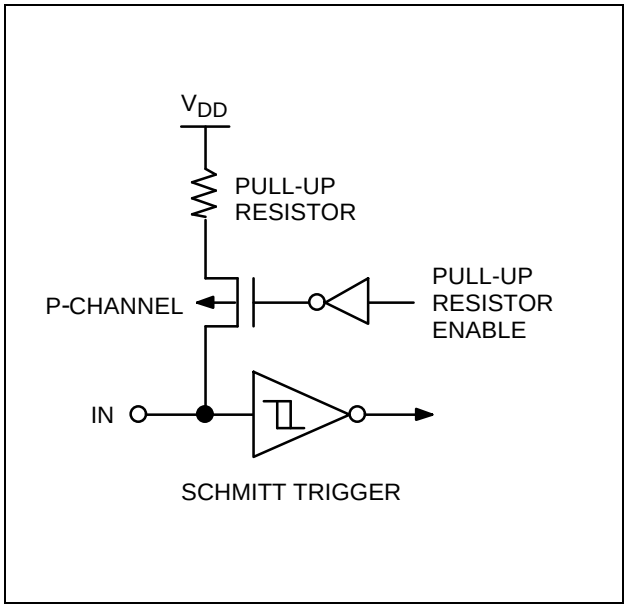


Figure 1-4. Pin Circuit Type A-3

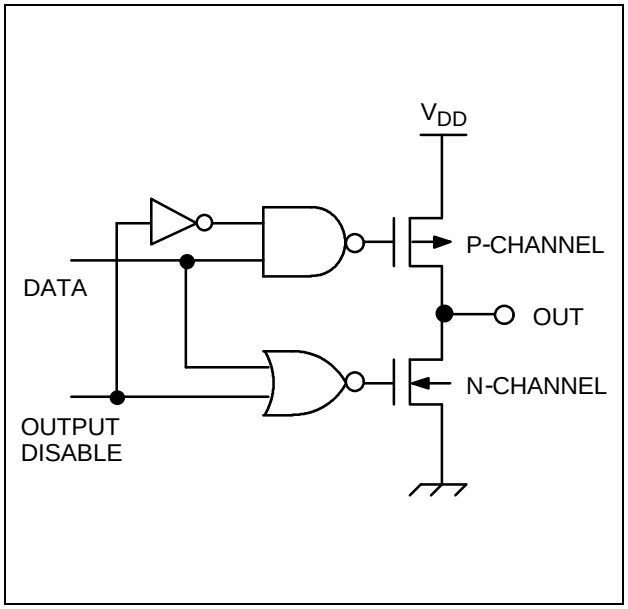
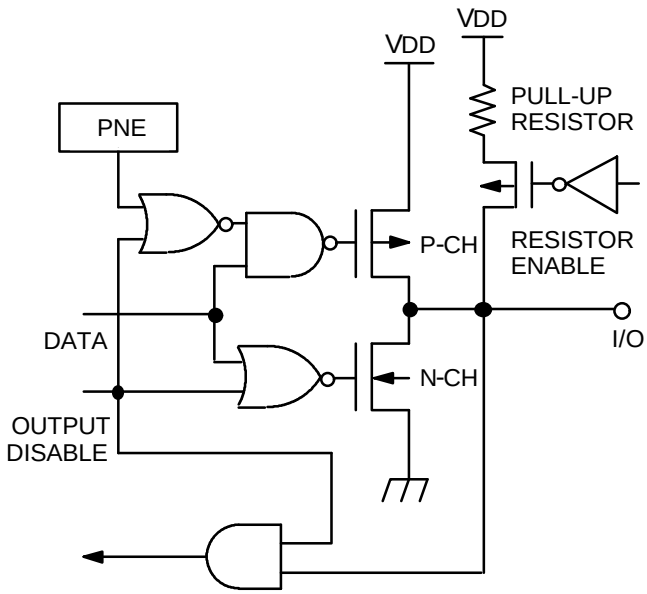
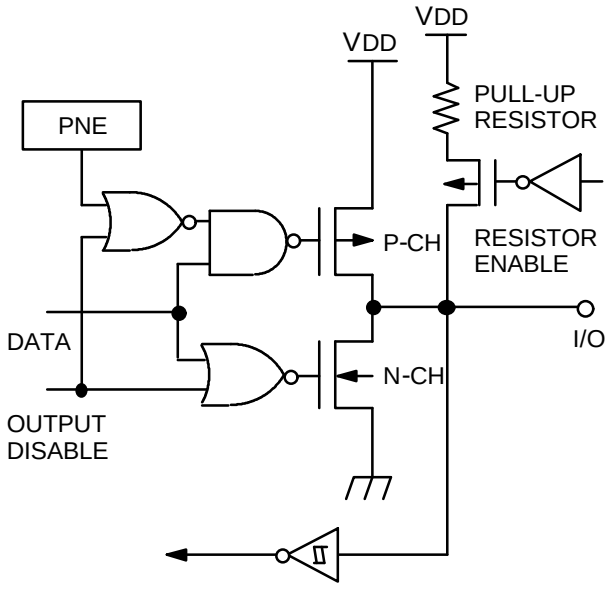


Figure 1-6. Pin Circuit Type C



CIRCUIT TYPE A

Figure 1-7. Pin Circuit Type E



SCHMITT TRIGGER

Figure 1-8. Pin Circuit Type E-1

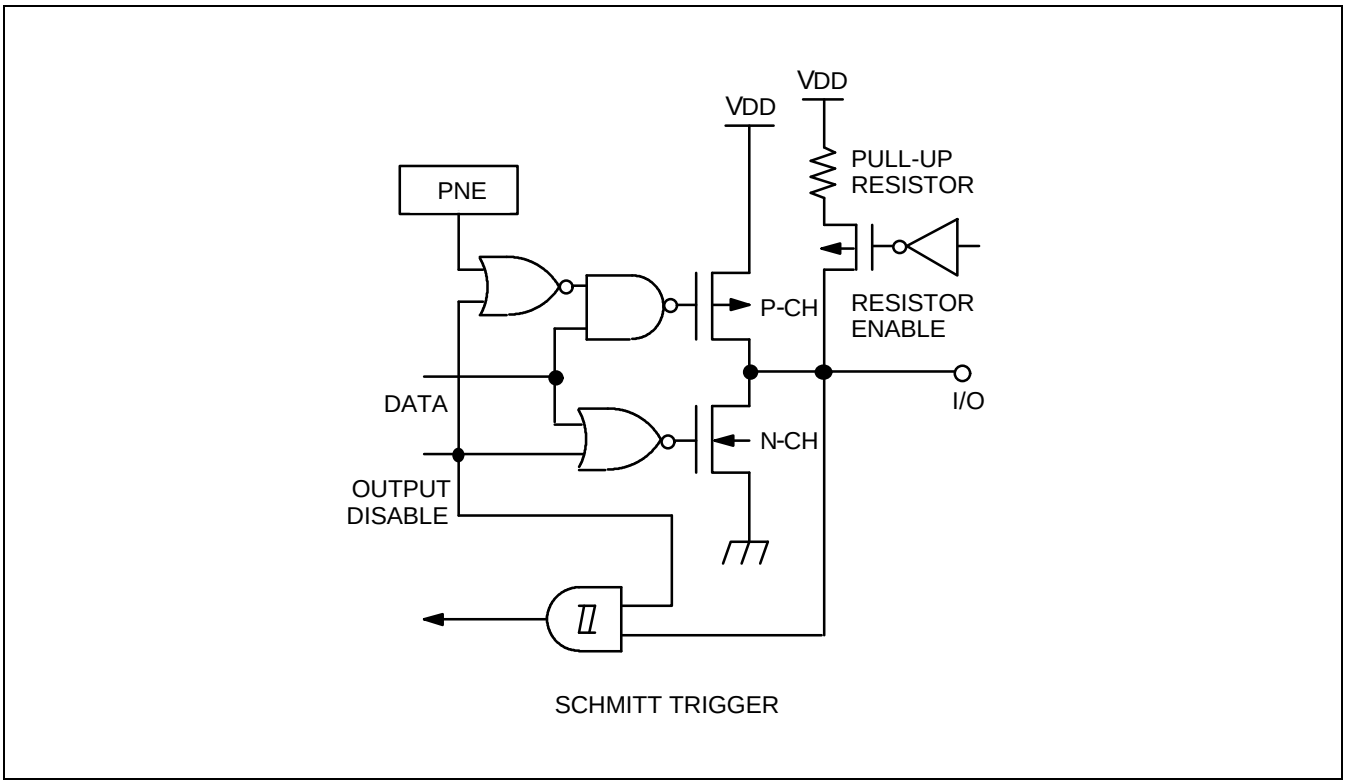


Figure 1-9. Pin Circuit Type E-2

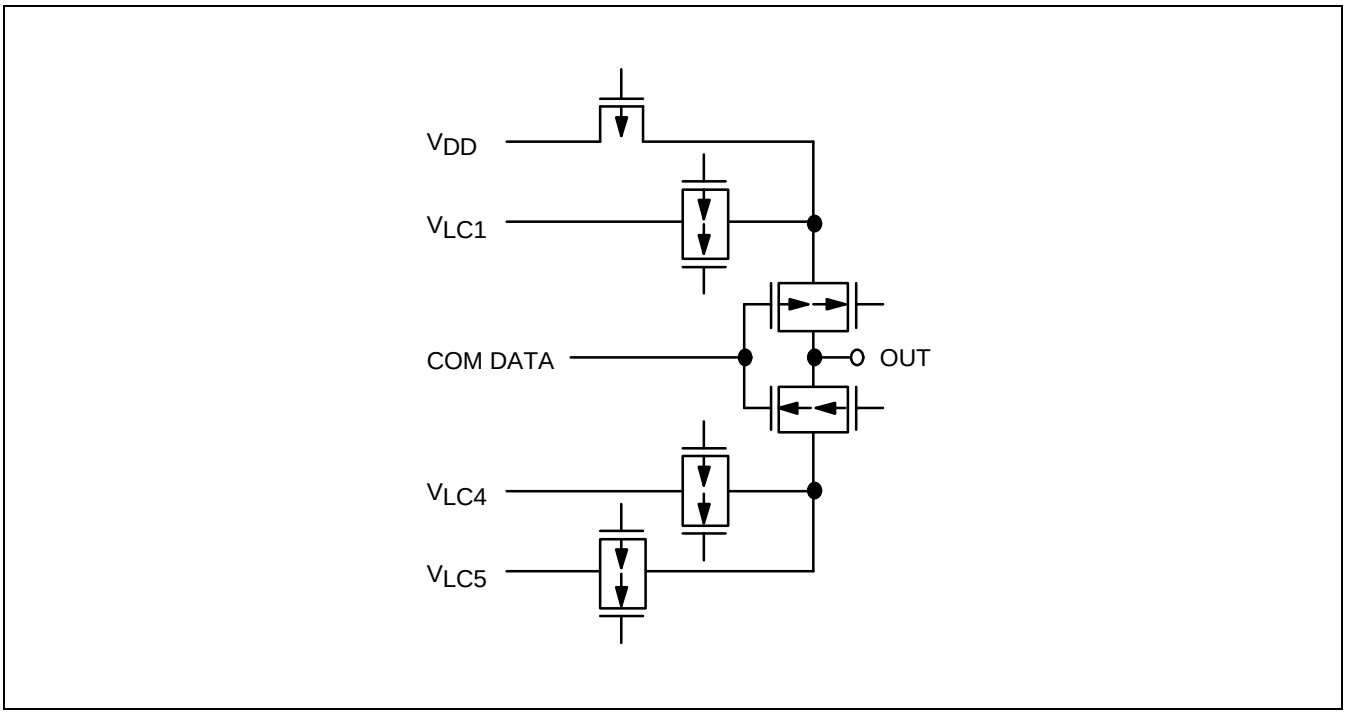


Figure 1-10. Pin Circuit Type H-3

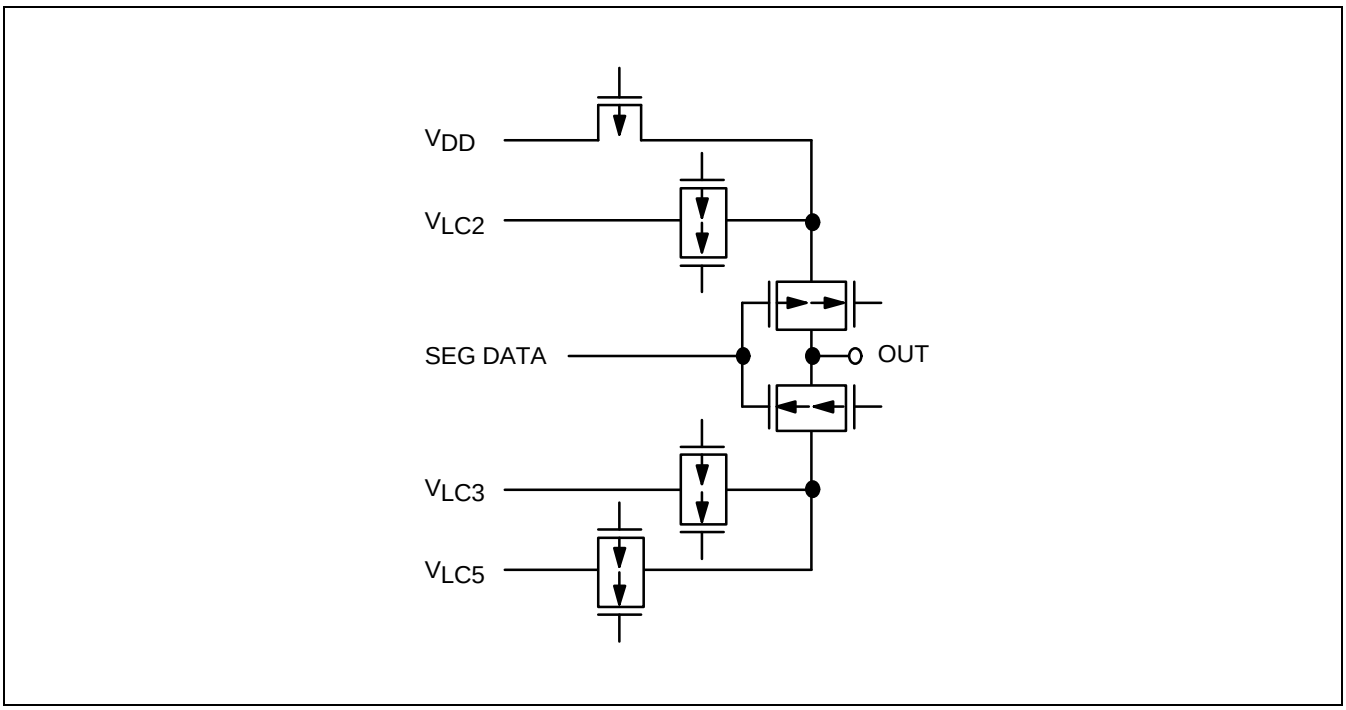


Figure 1-11. Pin Circuit Type H-15

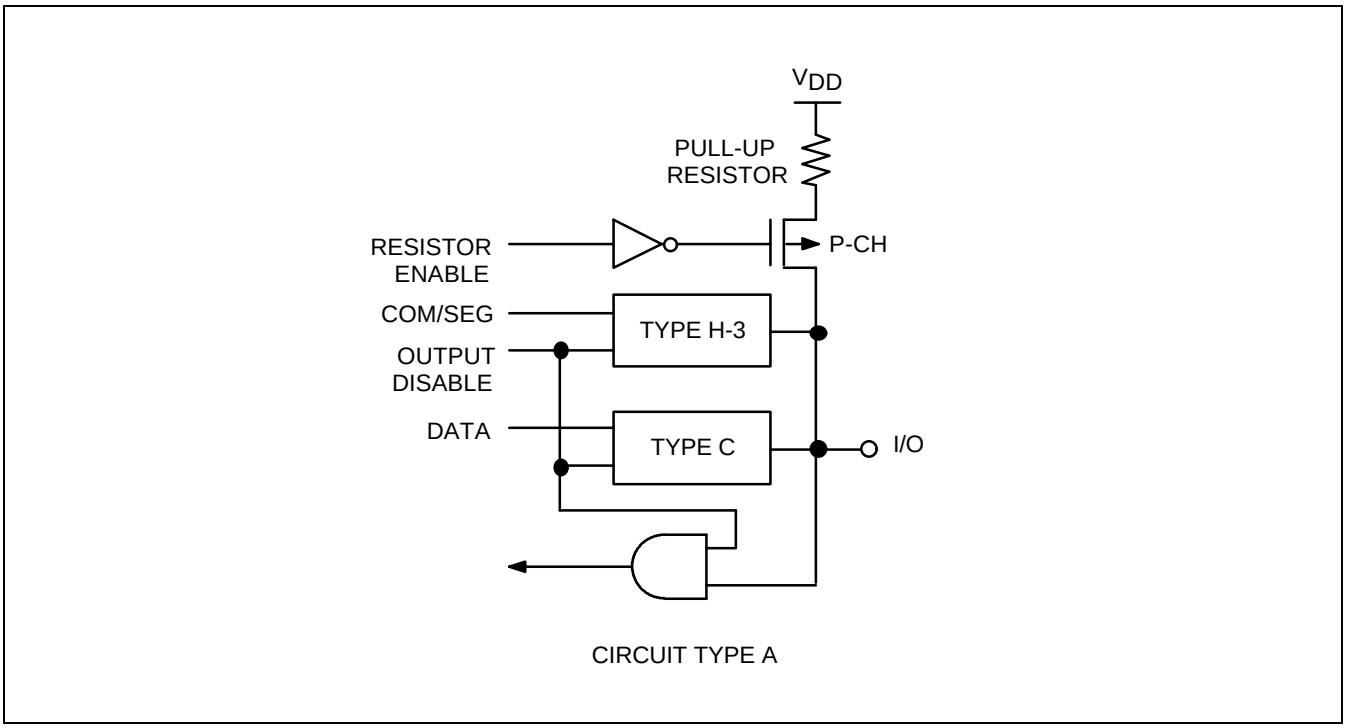


Figure 1-12. Pin Circuit Type H-13

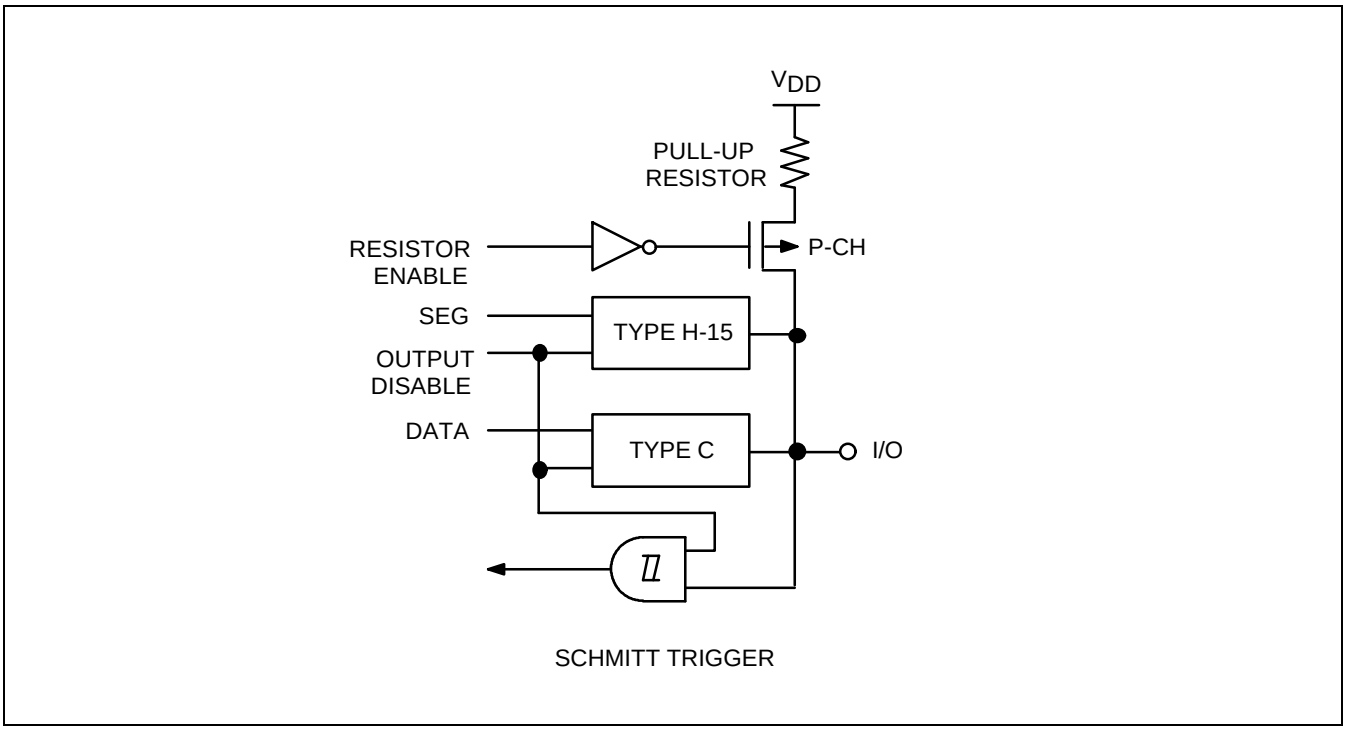


Figure 1-13. Pin Circuit Type H-16

14 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72F5 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{in}
— Clock timing measurement at XT_{in}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 14–1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	Ports 0–9	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 35	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15 (note)	
		Total for ports 0, 2–9	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14–2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH3}	0.7V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, P3.2, P3.3, and RESET	0.8V_{DD}		V_{DD}	
	V_{IH3}	X_{in}, X_{out}, and XT_{in}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, P3.2, P3.3, and RESET			0.2V_{DD}	
	V_{IL3}	X_{in}, X_{out}, and XT_{in}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = – 1 mA Ports 0, 2–9	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 0, 2–9	–	–	2.0	V

Table 14–2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{in}, X_{out}, XT_{in}, and RESET			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V X_{in}, X_{out}, and XT_{in}	–	–	– 3	µA
	I_{LIL2}	V_I = 0 V X_{in}, X_{out}, and XT_{in}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	µA
Pull-Up Resistor	R_{LI}	V_I = 0 V; V_{DD} = 5 V Port 0–9	25	47	100	kΩ
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_I = 0 V; V_{DD} = 5 V, RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	
LCD Voltage Dividing Resistor	R_{LCD}	Ta = 25 °C	25	55	80	kΩ
$\|V_{DD}$-COMi$\|$ Voltage Drop (i = 0–15)	V_{DC}	– 15 µA per common pin	–	–	120	mV
$\|V_{DD}$-SEGx$\|$ Voltage Drop (x = 0–55)	V_{DS}	– 15 µA per segment pin	–	–	120	
V_{LC1} Output Voltage	V_{LC1}	LCD clock = 0 Hz, V_{LC5} = 0 V	$0.8V_{DD}$-0.2	$0.8V_{DD}$	$0.8V_{DD}$+0.2	V
V_{LC2} Output Voltage	V_{LC2}		$0.6V_{DD}$-0.2	$0.6V_{DD}$	$0.6V_{DD}$+0.2	
V_{LC3} Output Voltage	V_{LC3}		$0.4V_{DD}$-0.2	$0.4V_{DD}$	$0.4V_{DD}$+0.2	
V_{LC4} Output Voltage	V_{LC4}		$0.2V_{DD}$-0.2	$0.2V_{DD}$	$0.2V_{DD}$+0.2	

Table 14–2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

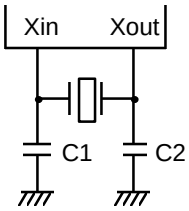
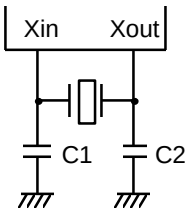
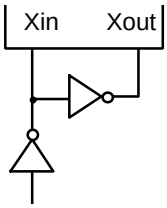
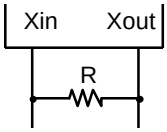
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current	I_{DD1} (2)	V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	–	3.9 2.9	8.0 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.8 1.3	4.0 3.0	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz		1.3 1.2	2.5 1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.44	1.5 1.0	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15.3	30	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			6.4	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT = 0V		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.5	3	
		Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	

NOTES:

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
3. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents.

Table 14–3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range; V_{DD} = 3.0 V.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V_{DD} = 3.0 V	–	–	10	ms
			V_{DD} = 2.0 V to 5.5 V	–	–	30	
External Clock		X_{in} input frequency (1)	–	0.4	–	6.0	MHz
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns
RC Oscillator		Frequency	R = 20 kΩ, V_{DD} = 5 V	–	2	–	MHz
			R = 39 kΩ, V_{DD} = 3 V	–	1	–	

NOTES:

1. Oscillation frequency and X_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 14–4. Recommended Oscillator Constants

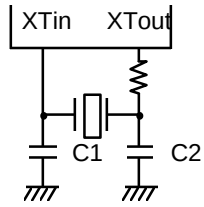
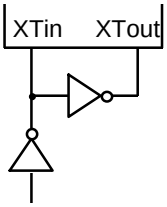
(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 14–5. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 2.0 V to 5.5 V	–	–	10	
External Clock		XT_{in} input frequency (1)	–	32	–	100	kHz
		XT_{in} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{in} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 14–6. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 14–7. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 2.0 V to 5.5 V	0.95		64	
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 2.0 V to 5.5 V			1	
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 2.0 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V; Input	800	–	–	ns
		Internal SCK source; Output	650			
		V_{DD} = 2.0 V to 5.5 V; Input	3200			
		Internal SCK source; Output	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V; Input	325	–	–	ns
		Internal SCK source; Output	$t_{KCY}/2$ – 50			
		V_{DD} = 2.0 V to 5.5 V; Input	1600			
		Internal SCK source; Output	$t_{KCY}/2$ – 150			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V; Input	100	–	–	ns
		V_{DD} = 2.7 V to 5.5 V; Output	150			
		V_{DD} = 2.0 V to 5.5 V; Input	150			
		V_{DD} = 2.0 V to 5.5 V; Output	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V; Input	400	–	–	ns
		V_{DD} = 2.7 V to 5.5 V; Output	400			
		V_{DD} = 2.0 V to 5.5 V; Input	600			
		V_{DD} = 2.0 V to 5.5 V; Output	500			

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

Table 14–7. A.C. Electrical Characteristics (Continued)

(T_A = – 40 _C to + 85 _C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V; Input	–	–	300	ns
		V_{DD} = 2.7 V to 5.5 V; Output			250	
		V_{DD} = 2.0 V to 5.5 V; Input			1000	
		V_{DD} = 2.0 V to 5.5 V; Output			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, K0–K7	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128 / fx as assigned by the IMOD0 register setting.

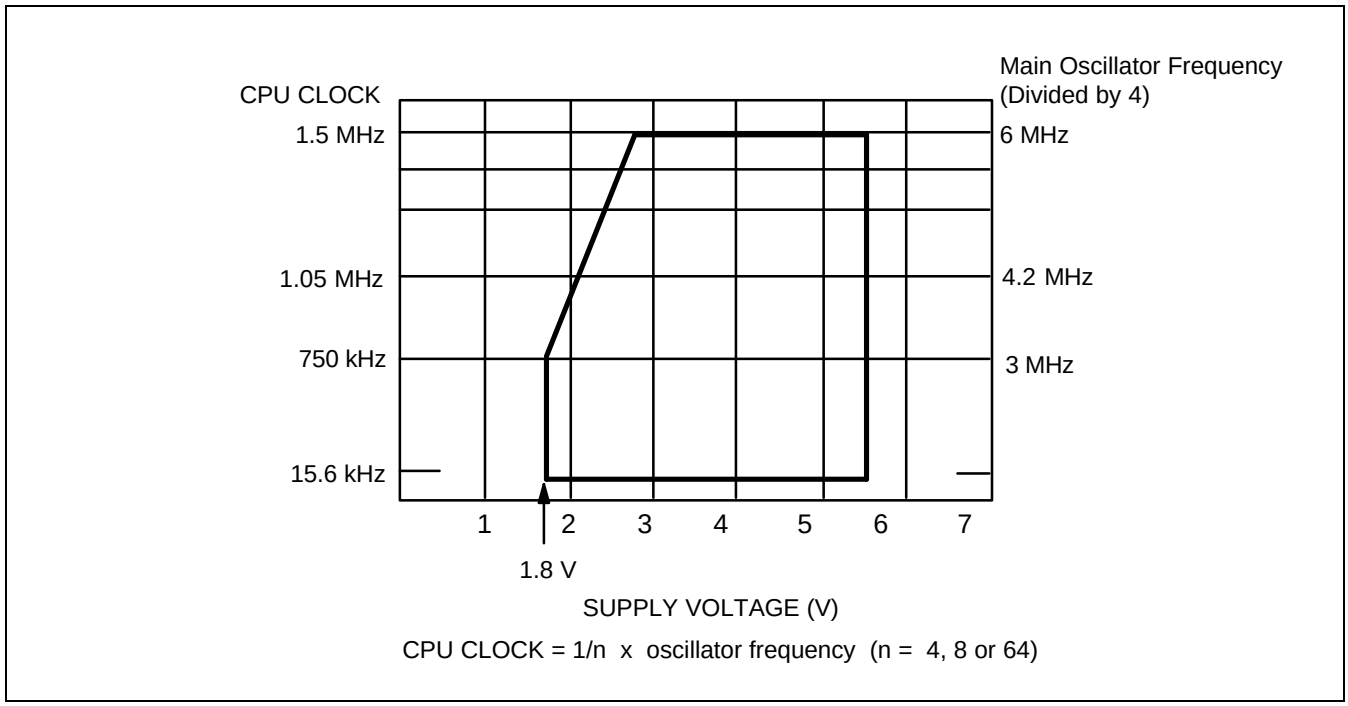


Figure 14–1. Standard Operating Voltage Range

Table 14–8. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

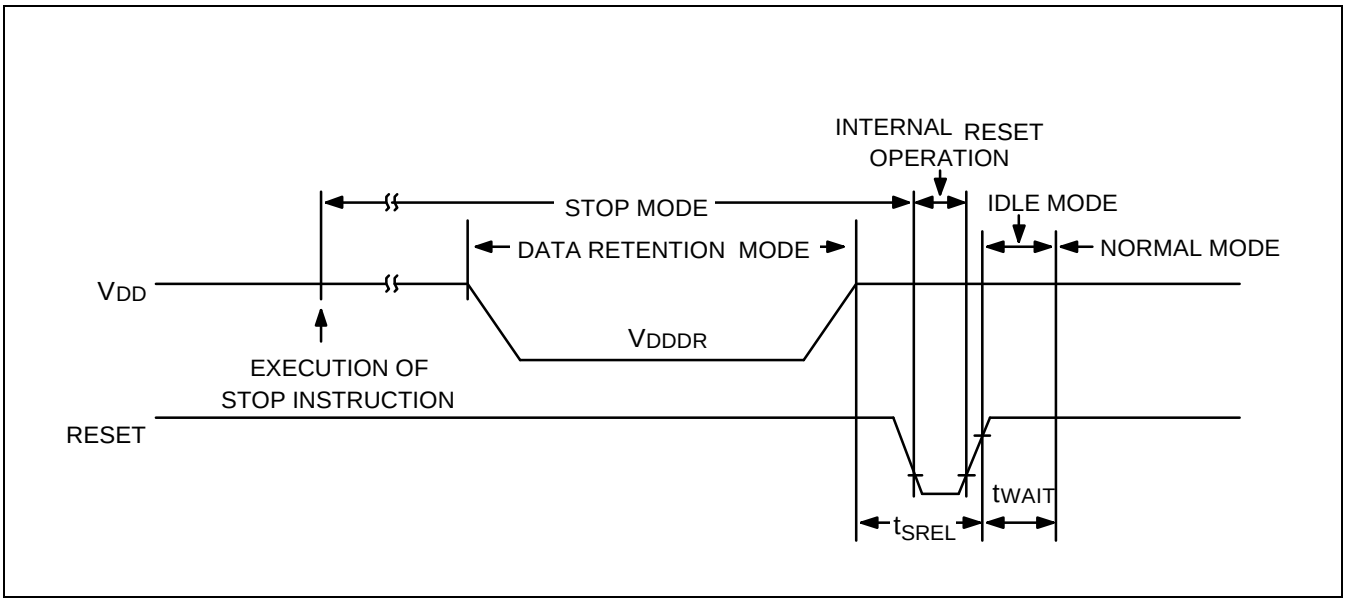


Figure 14–2. Stop Mode Release Timing When Initiated by RESET

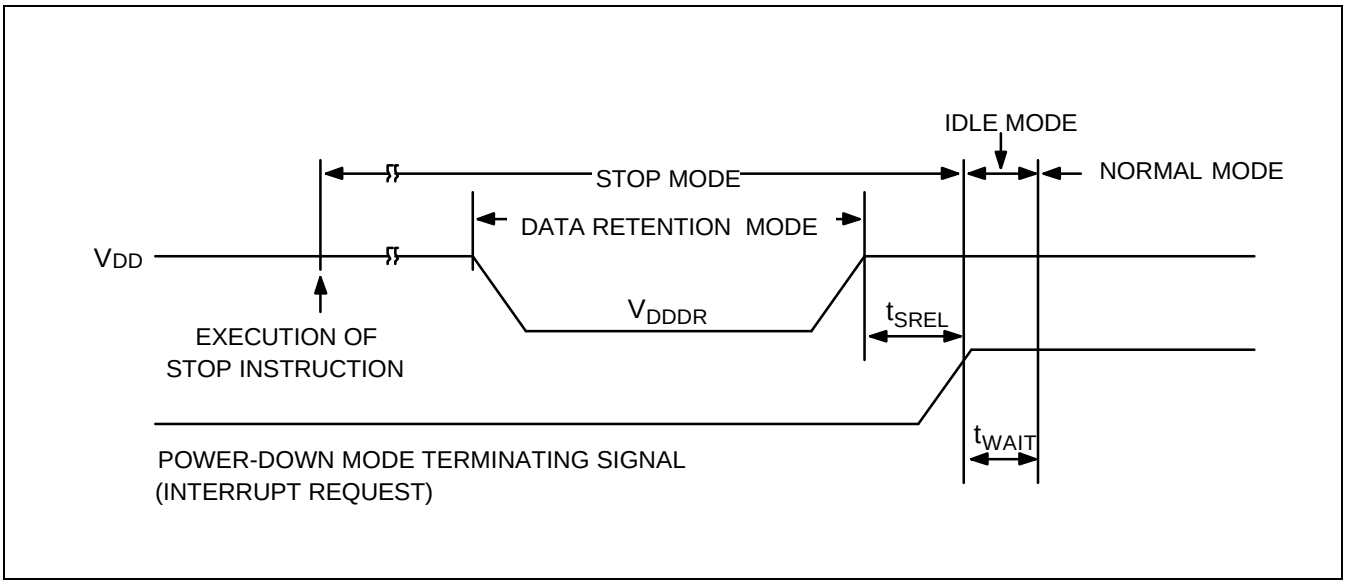


Figure 14–3. Stop Mode Release Timing When Initiated by Interrupt Request

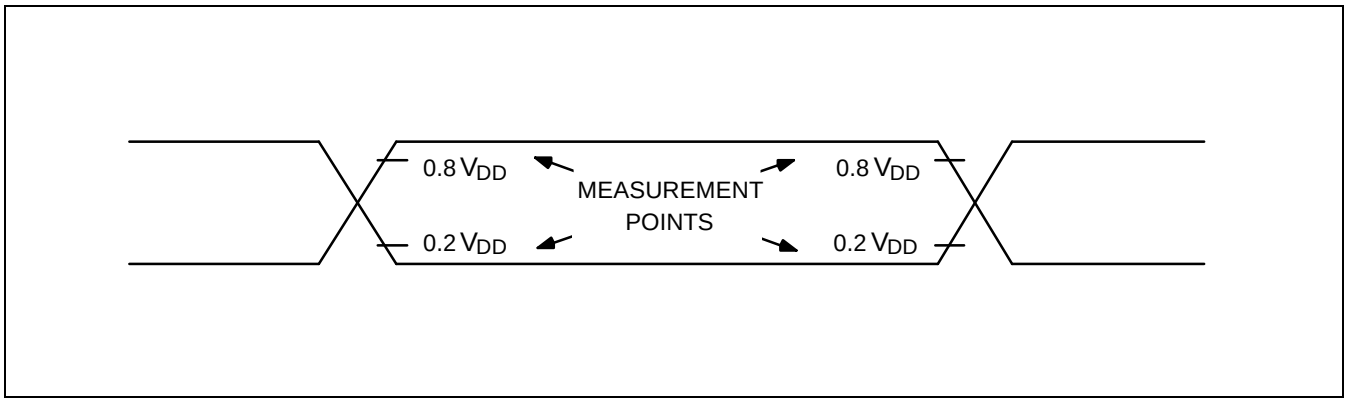


Figure 14–4. A.C. Timing Measurement Points (Except for X_{in} and XT_{in})

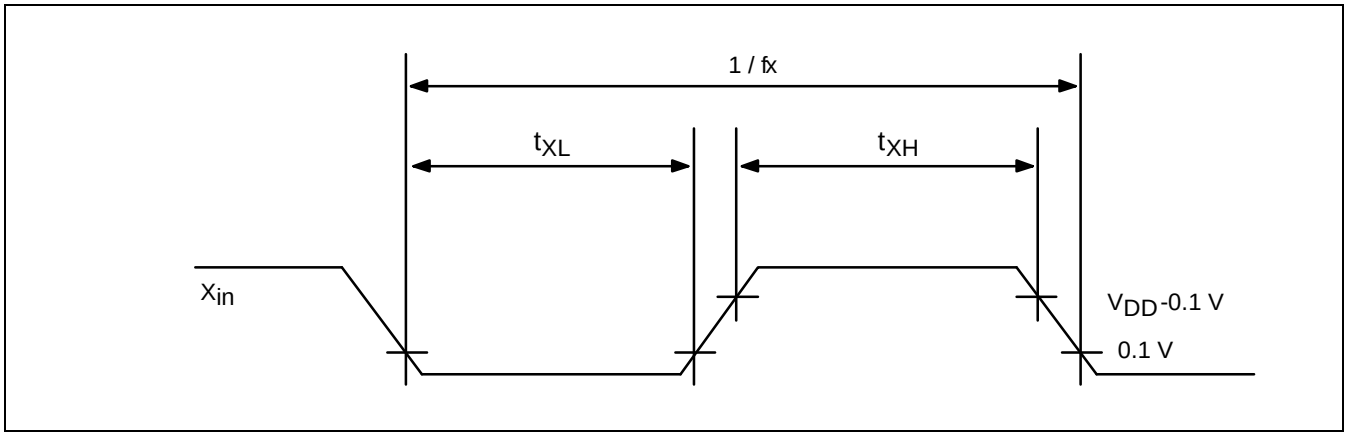


Figure 14–5. Clock Timing Measurement at X_{in}

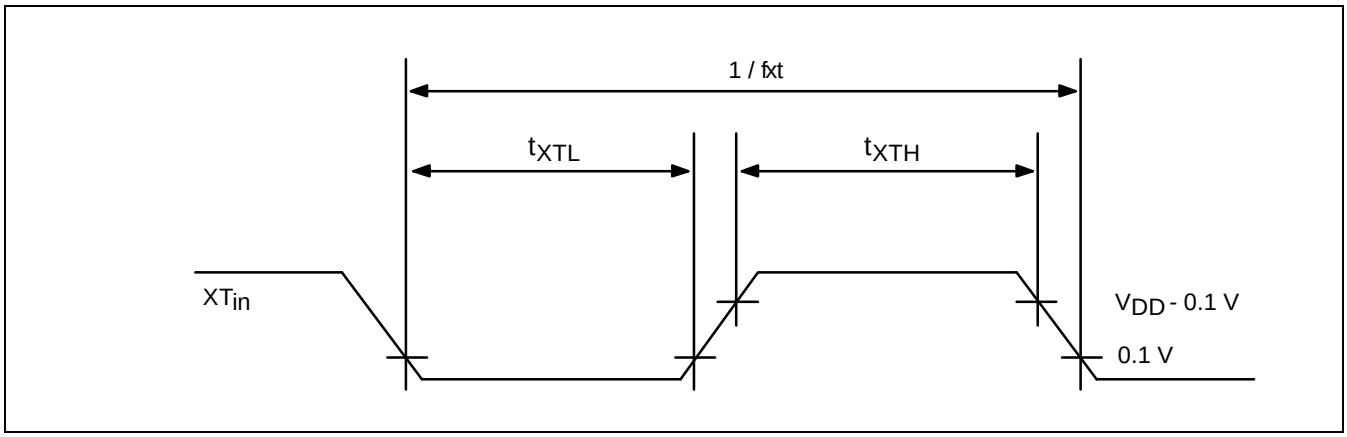


Figure 14–6. Clock Timing Measurement at XT_{in}

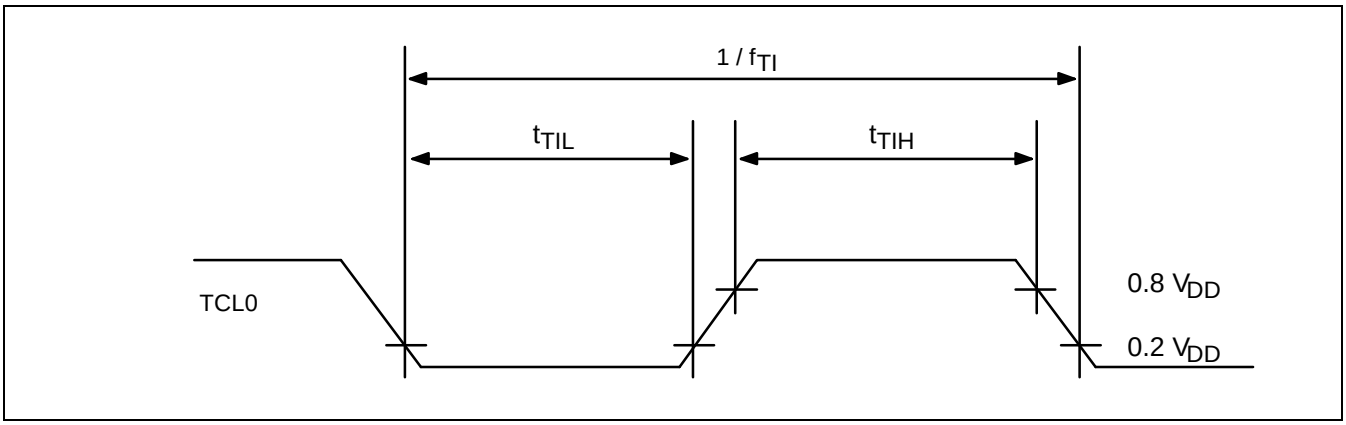


Figure 14–7. TCL Timing

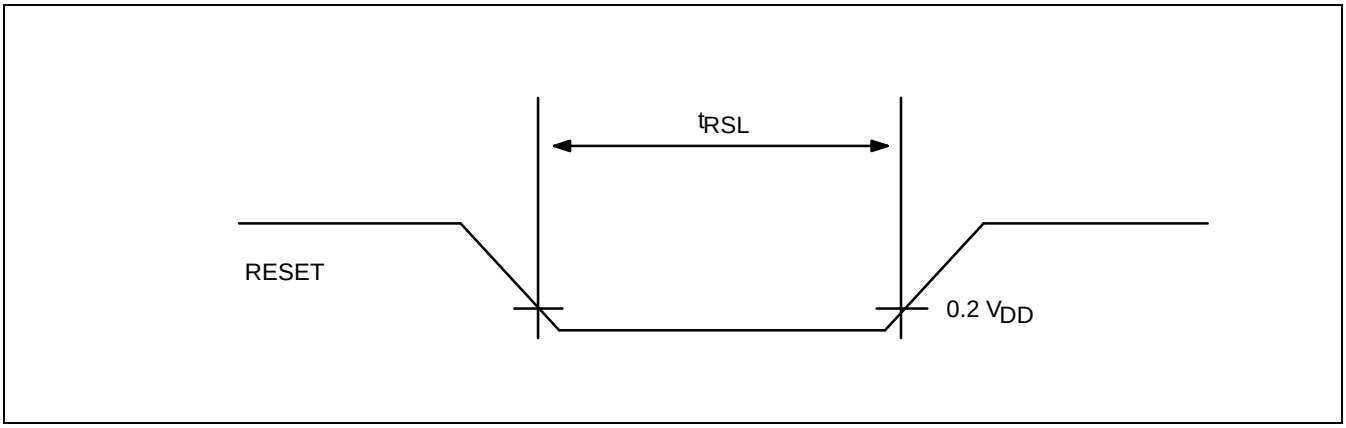


Figure 14–8. Input Timing for RESET Signal

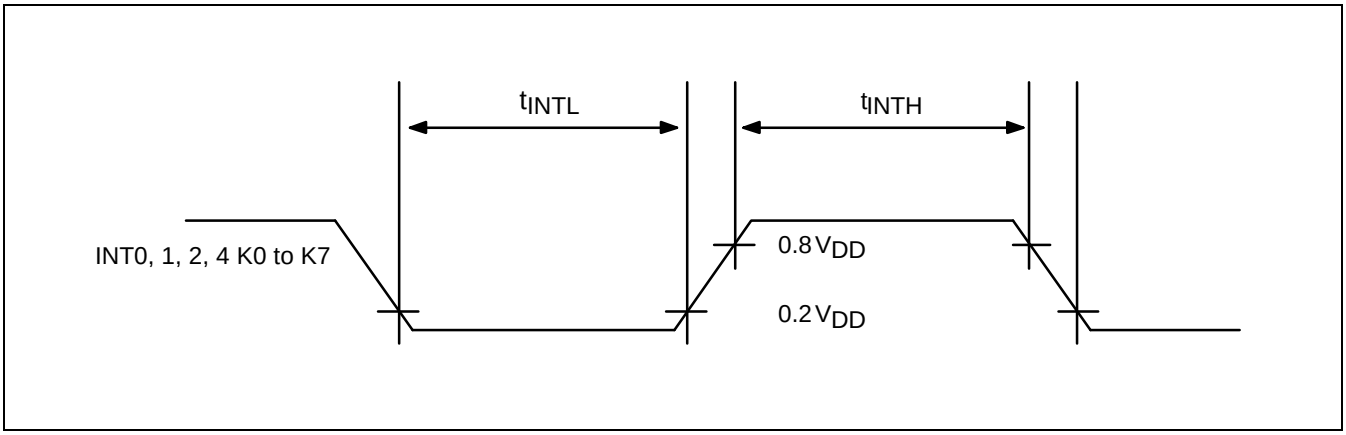


Figure 14–9. Input Timing for External Interrupts and Quasi-Interrupts

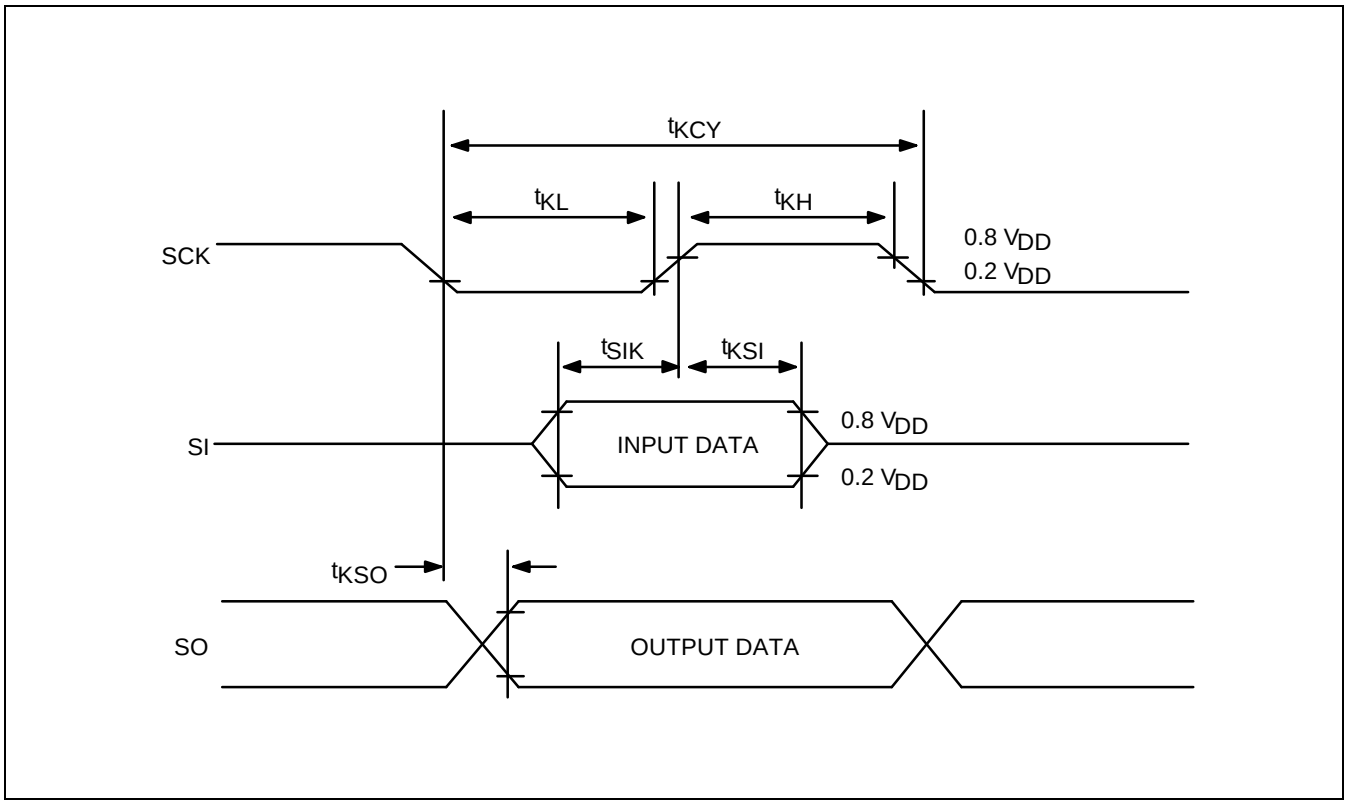


Figure 14–10. Serial Data Transfer Timing

NOTES

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements.

They do not, however, represent guaranteed operating values.

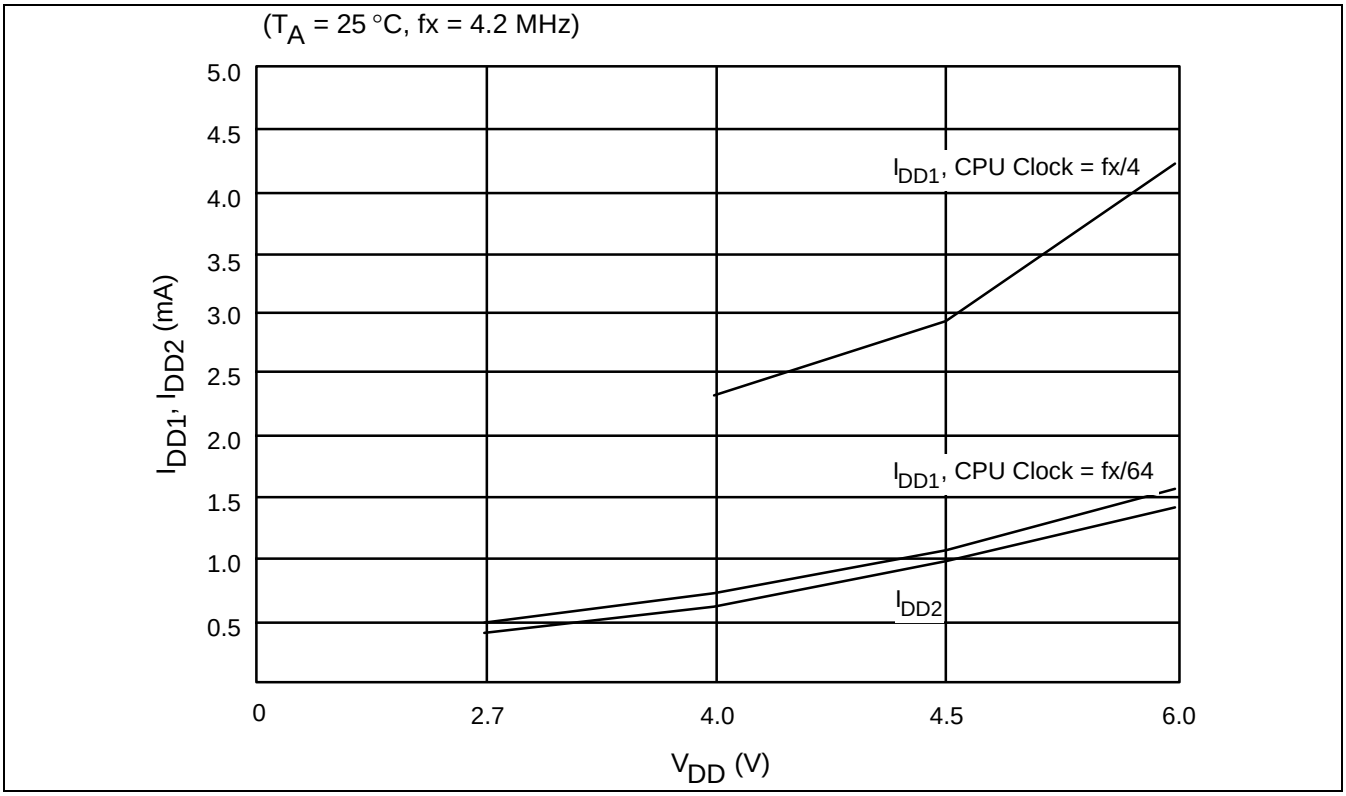


Figure 14–11. I_{DD1}, I_{DD2} VS. V_{DD}

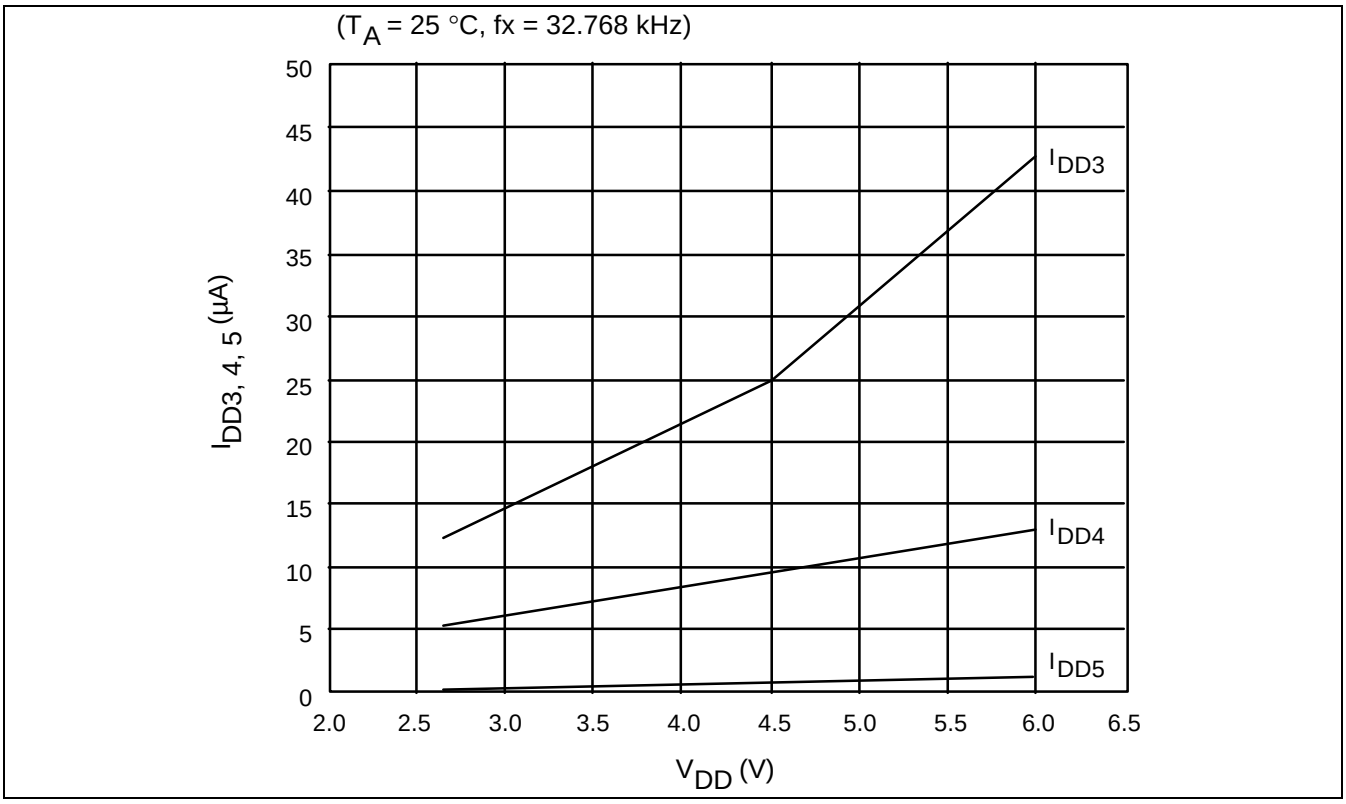


Figure 14–12. I_{DD3}, I_{DD4}, I_{DD5} VS. V_{DD}

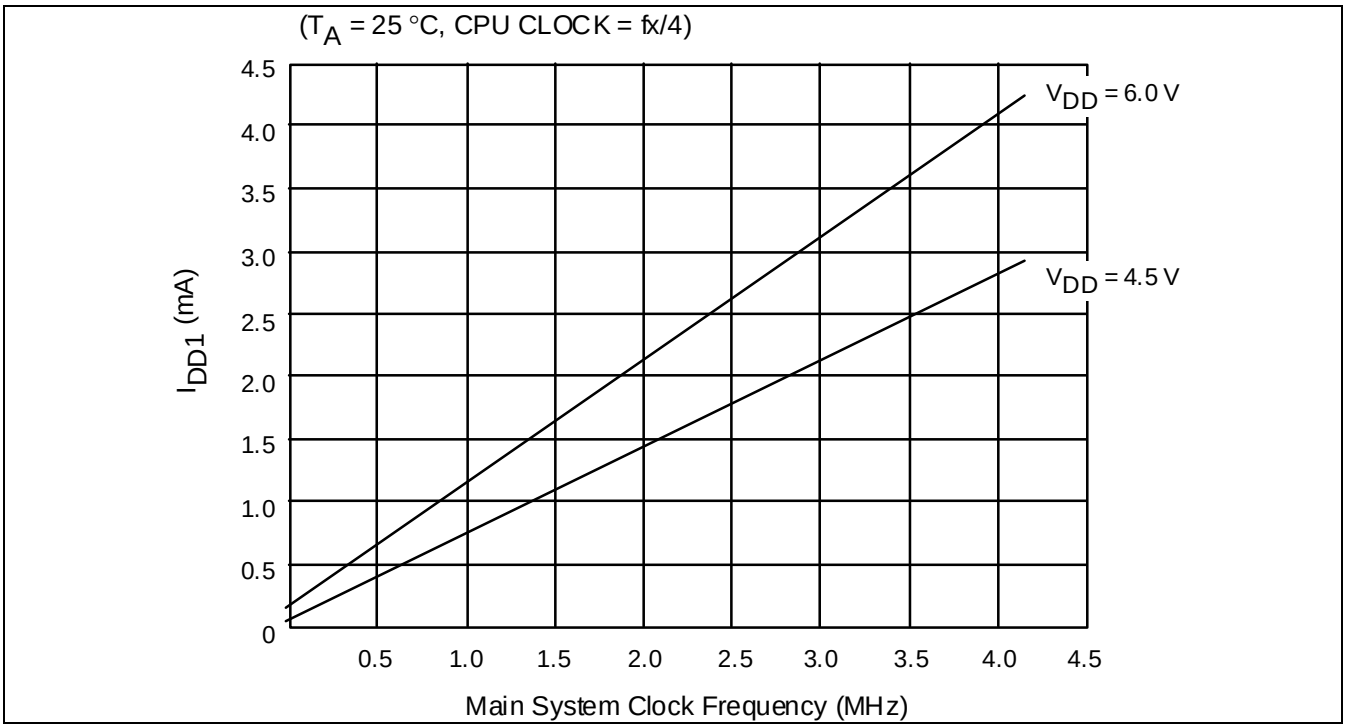


Figure 14–13. I_{DD1} VS. Main System Clock Frequency

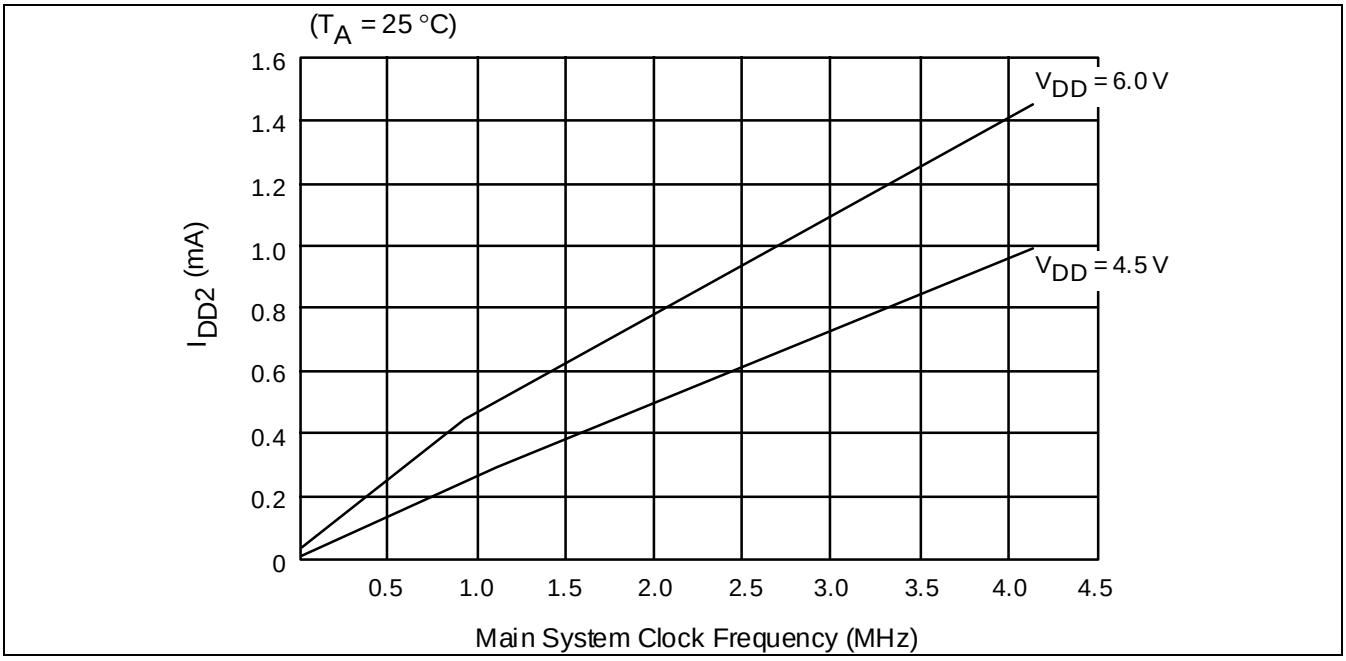


Figure 14–14. I_{DD2} VS. Main System Clock Frequency

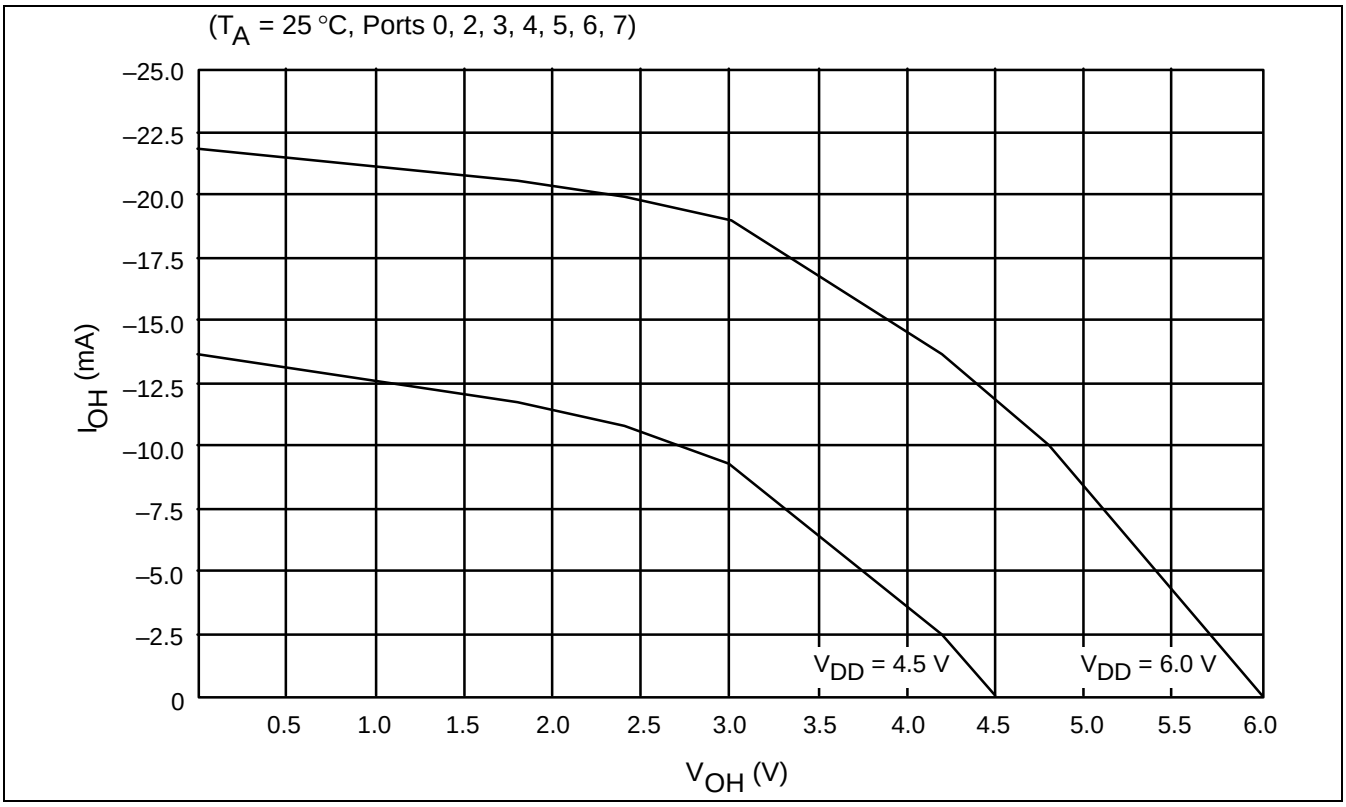


Figure 14–15. I_{OH} VS. V_{OH} (P0, 2, 3, 4, 5, 6, 7)

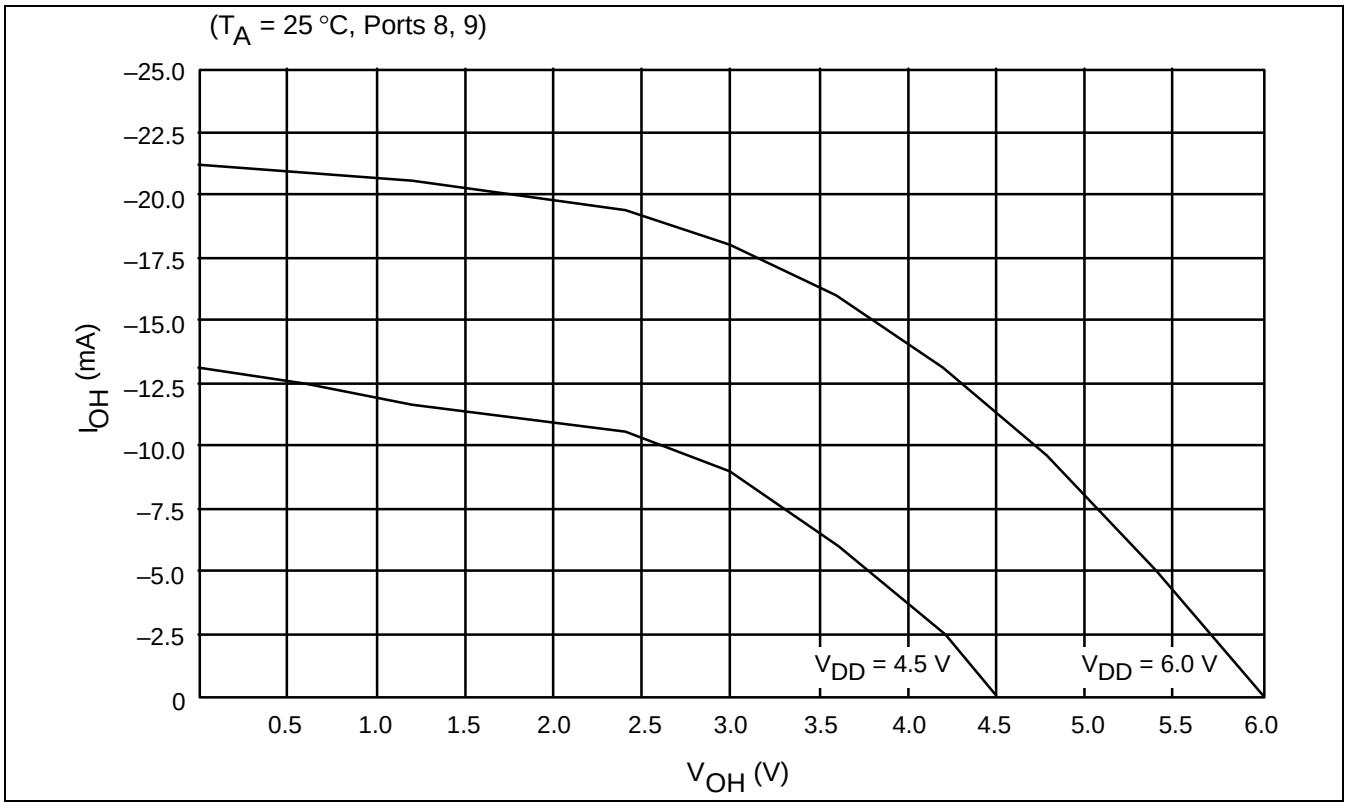


Figure 14–16. I_{OH} VS. V_{OH} (P8, 9)

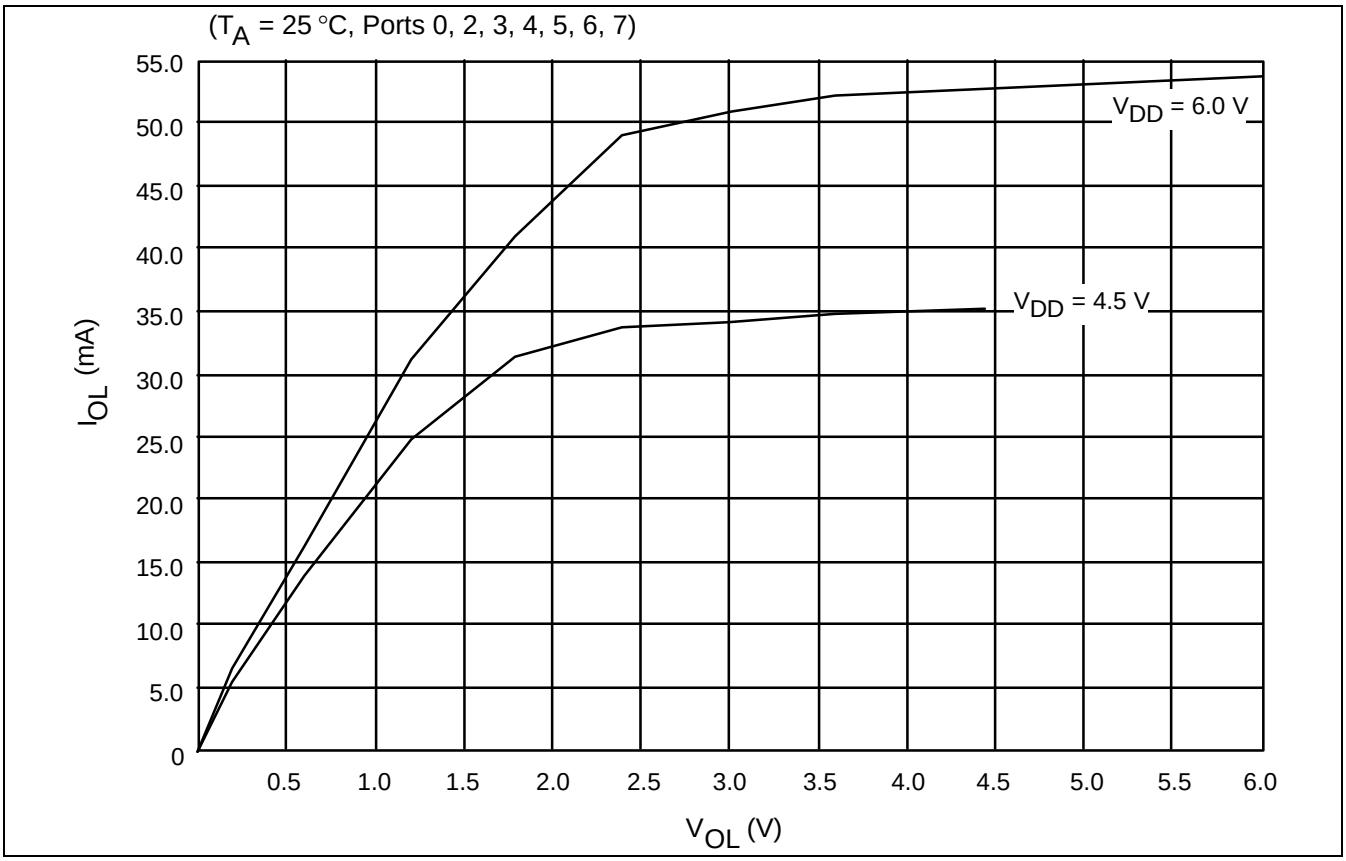


Figure 14–17. I_{OL} VS. V_{OL} (P0, 2, 3, 4, 5, 6, 7)

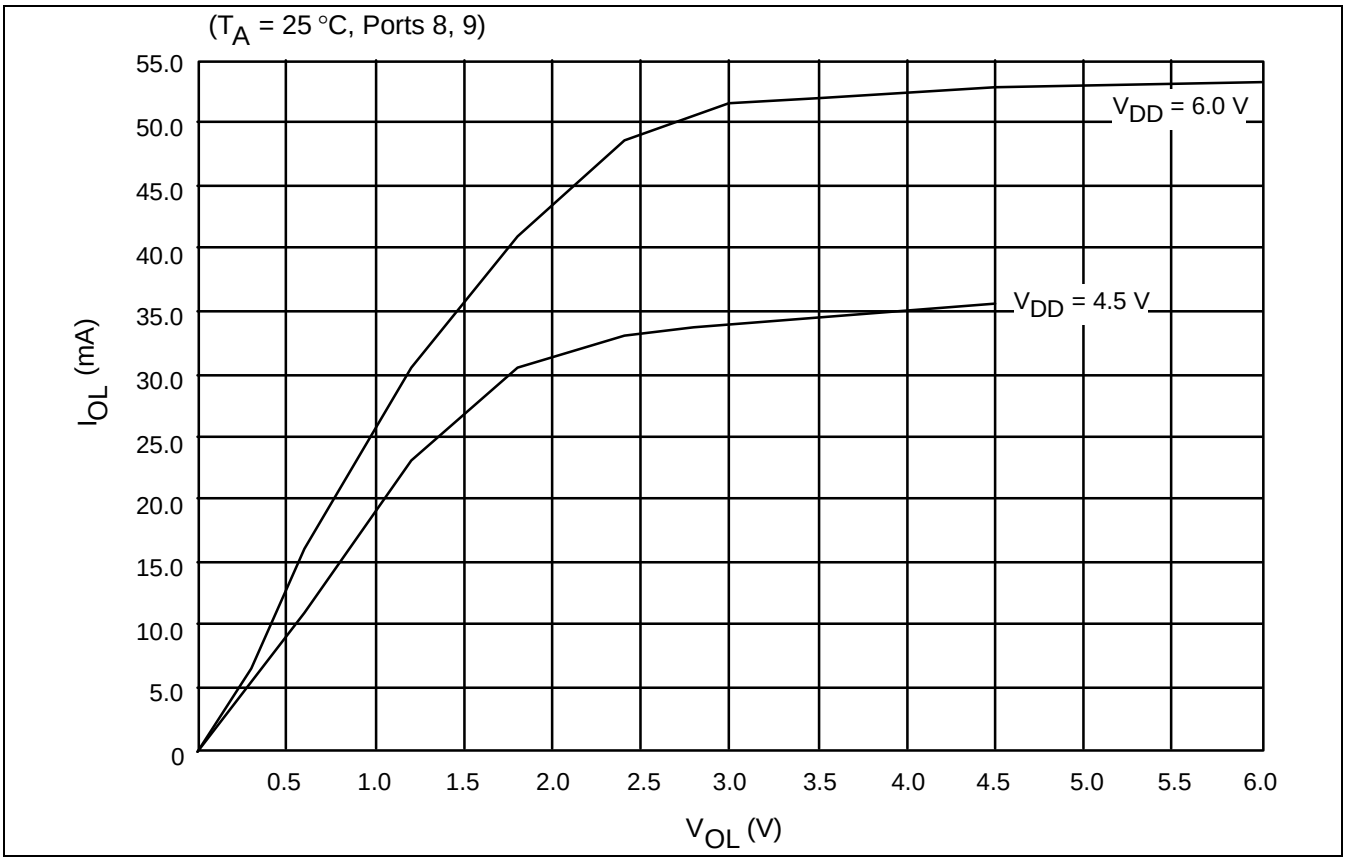


Figure 14–18. I_{OL} VS. V_{OL} (P8, 9)

15 MECHANICAL DATA

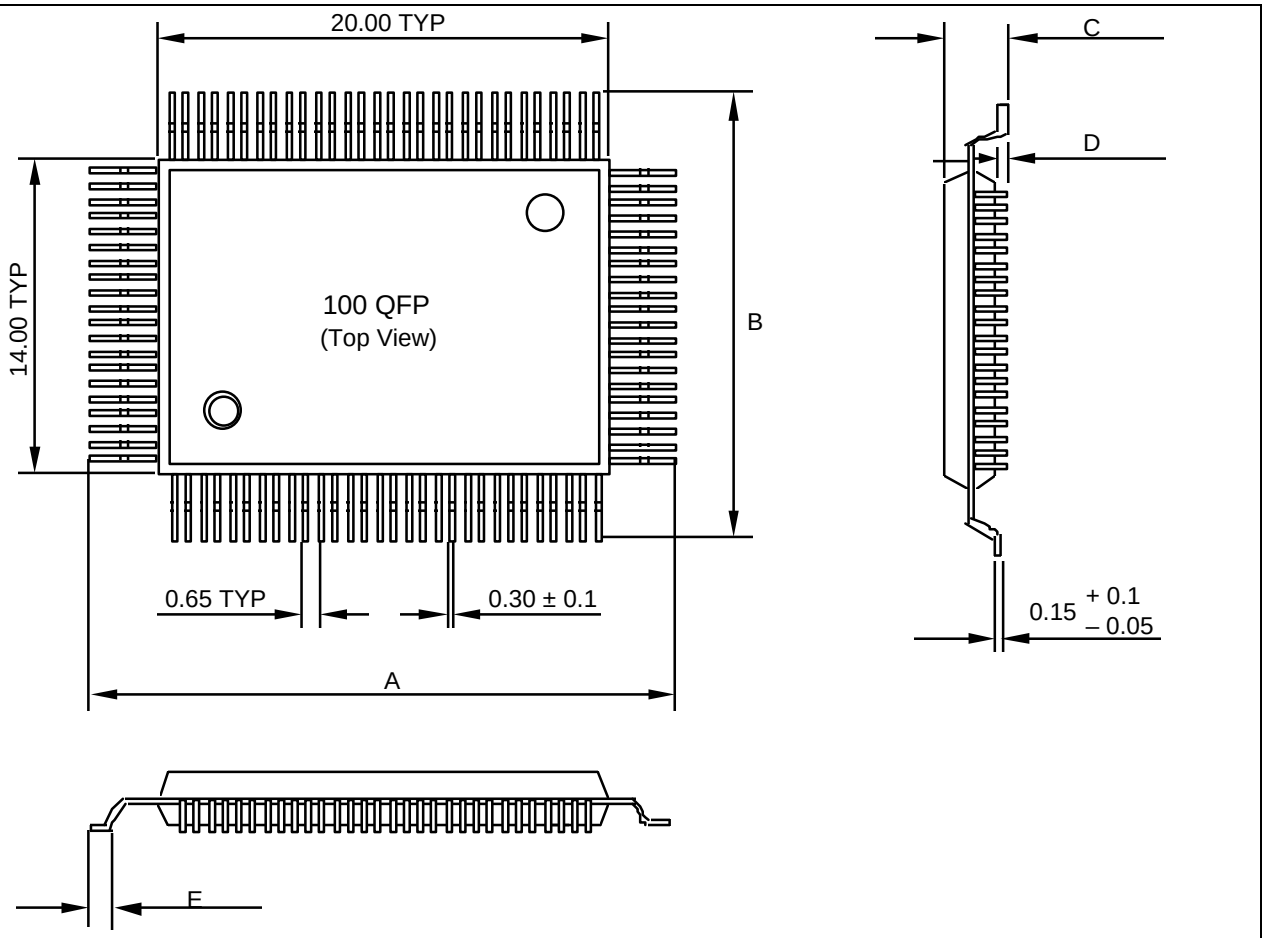
OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimetersD

— Pad diagram

— Pad/pin coordinate data table



Item / Package	A	B	C	D	E
100-QFP-1420A	25.00 ± 0.3	19.00 ± 0.3	2.45 MAX	0.15 + 0.1 – 0.05	1.20 ± 0.2
100-QFP-1420C	23.20 ± 0.3	17.20 ± 0.3	3.00 MAX	0.15 ± 0.1	0.80 ± 0.2

NOTE: Typical dimensions are in millimeters.

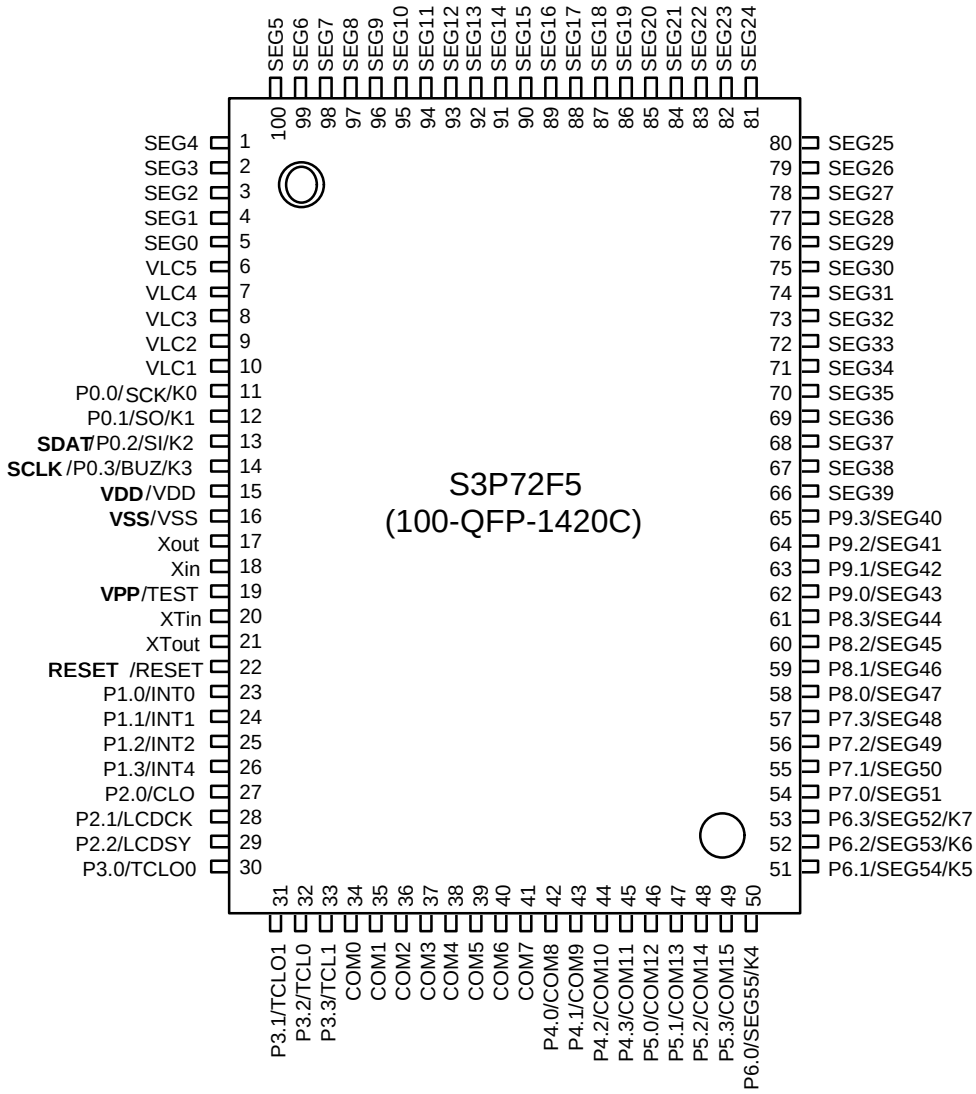
Figure 15–1. 100-QFP Package Dimensions

16 S3P72F5 OTP

OVERVIEW

The S3P72F5 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72F5 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P72F5 is fully compatible with the S3C72F5, both in function and in pin configuration. Because of its simple programming requirements, the S3P72F5 is ideal for use as an evaluation chip for the S3C72F5.



NOTE: The bolds indicate an OTP pin name.

Figure 16–1. S3P72F5 Pin Assignments (100-QFP Package)

Table 16–1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P0.2	SDAT	13	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input / push-pull output port.
P0.3	SCLK	14	I/O	Serial clock pin. Input only pin.
TEST	V_{PP}(TEST)	19	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	22	I	Chip initialization
V_{DD} / V_{SS}	V_{DD} / V_{SS}	15/16	I	Logic power supply pin. VDD should be tied to +5 V during programming.

Table 16–2. Comparison of S3P72F5 and S3C72F5 Features

Characteristic	S3P72F5	S3C72F5
Program Memory	16 Kbyte EPROM	16 Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP}(TEST)=12.5V	
Pin Configuration	100 QFP	100 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the S3P72F5, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16–3 below.

Table 16–3. Operating Mode Selection Criteria

V_{DD}	Vpp (TEST)	REG/MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 16–4. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current	I_{DD1} (2)	V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz	–	3.9 2.9	8.0 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.8 1.3	4.0 3.0	
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz 4.19 MHz		1.3 1.2	2.5 1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.44	1.5 1.0	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	15.3	30	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			6.4	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT = 0V		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.5	3	
		Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	

NOTES:

1. Data includes power consumption for subsystem clock oscillation.
2. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
3. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents.

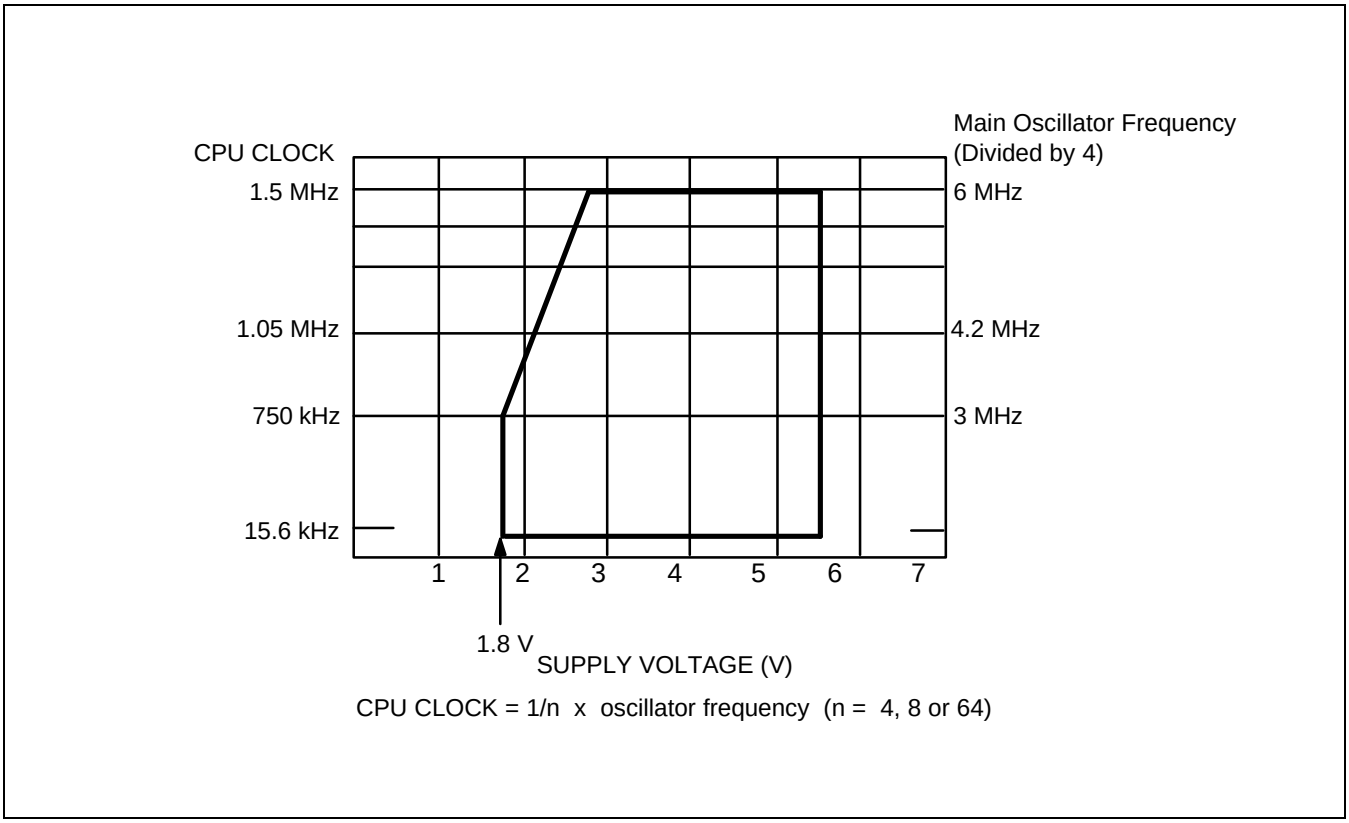


Figure 16–2. Standard Operating Voltage Range