OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
DG445, DG442

March 2000 File Number 3131.3

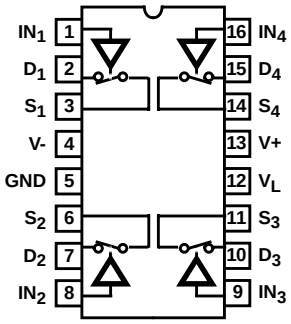
Quad CMOS Analog Switch

The IH5053 analog switch uses an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10µA.

The IH5053 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (1000ns) such that it exceeds the t_{OFF} time (500ns). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching.

Pinout

IH5053 (SBDIP)
TOP VIEW



SWITCH STATES SHOWN FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	SWITCHES
0	Off
1	On

Features

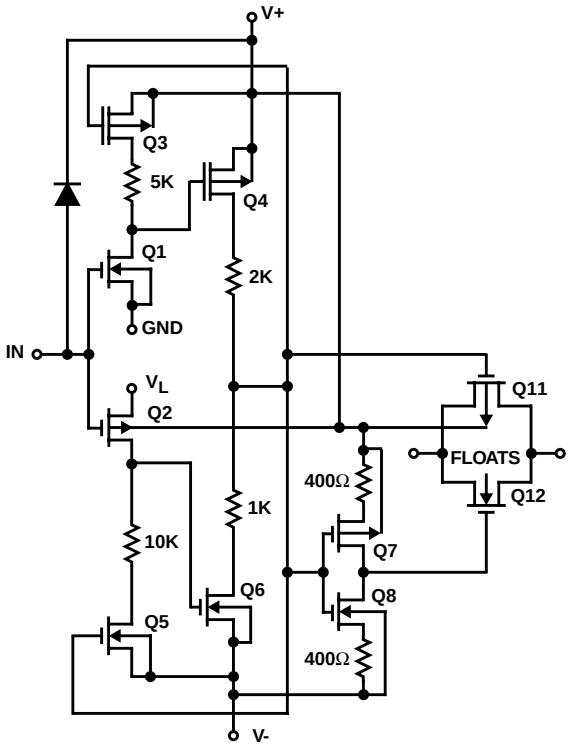
- Switches Greater Than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current . . . . . <10µA
- Break-Before-Make Switching
  - t_{OFF} 500ns
  - t_{ON} 1000ns
- TTL, CMOS Compatible
- 4 Normally Open Switches
- Low $r_{DS(ON)}$ (Typ) 80Ω

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
IH5053CDE	0 to 70	16 Ld SBDIP	D16.3

Schematic Diagram

(1/4 AS SHOWN)



Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <±22V
V_L to V- . . . . . <33V
V_L to V_{IN} . . . . . <30V
V_L to GND . . . . . <20V
V_{IN} to GND . . . . . <20V
Continuous Current (S-D) 30mA
Peak Current IN or OUT (Pulsed 1ms, 10% Duty Cycle, Max) . . . 70mA

Thermal Information

Maximum Junction Temperature . . . . . 175^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Operating Conditions

Temperature Range . . . . . 0^{o}C to 70^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	(NOTES 1, 2) 0^{o}C	25^{o}C	70^{o}C	UNITS
DYNAMIC CHARACTERISTICS					
Turn ON Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 6)	-	1000	-	ns
Turn OFF Time, t_{OFF}		-	500	-	ns
Charge Injection, Q	Figure 7	-	20 (Typ)	-	mV
OFF Isolation, OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF (Figure 4)	-	50 (Typ)	-	dB
Crosstalk, CCRR	One Channel Off (Figure 3)	-	50 (Typ)	-	dB
DIGITAL INPUT CHARACTERISTICS					
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V	-	±10	-	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V	-	±10	-	µA
ANALOG SWITCH CHARACTERISTICS					
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	80	80	100	Ω
Channel-to-Channel, $r_{DS(ON)}$ Match		-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -10V to +10V	-	±10	100	nA
POWER SUPPLY CHARACTERISTICS					
+ Power Supply Quiescent Current, I+		10	10	100	µA
- Power Supply Quiescent Current, I-		10	10	100	µA
+5V Supply Quiescent Current, I_L		10	10	100	µA

NOTES:

1. Typical values are for Design Aid only, not guaranteed nor production tested.
2. Min or Max value unless otherwise specified.

Test Circuits and Waveforms

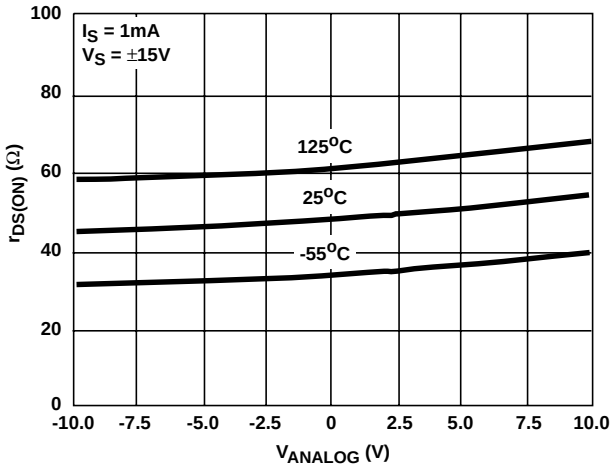


FIGURE 1. $r_{DS(ON)}$ vs ANALOG INPUT VOLTAGE

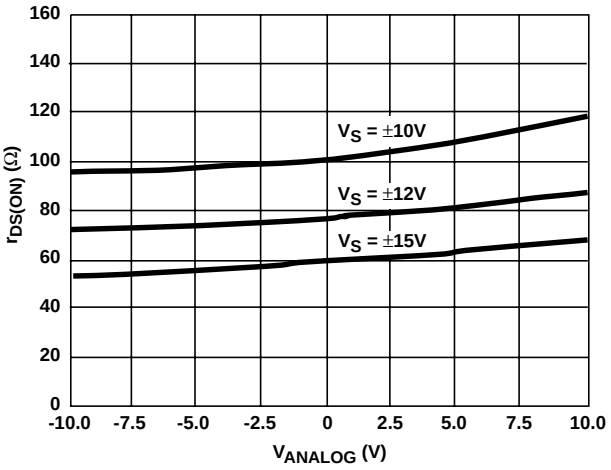


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

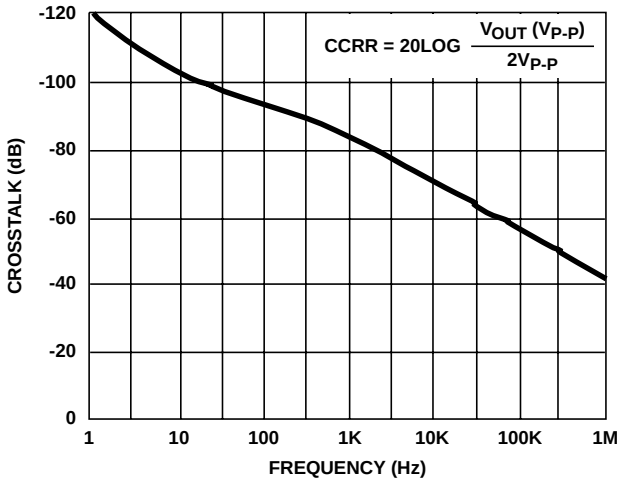


FIGURE 3A. CROSSTALK vs FREQUENCY

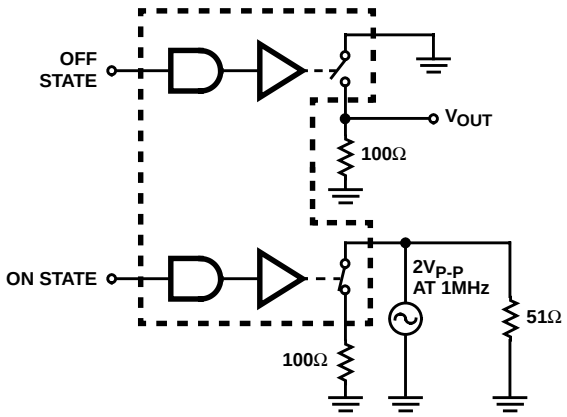


FIGURE 3B. TEST CIRCUIT

FIGURE 3. CROSSTALK

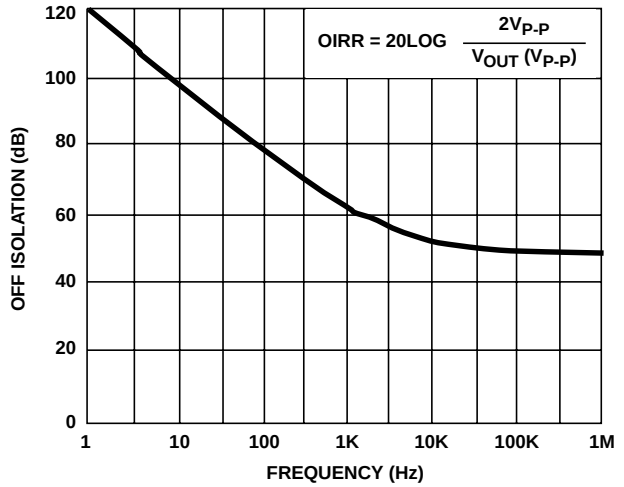


FIGURE 4A. OFF ISOLATION vs FREQUENCY

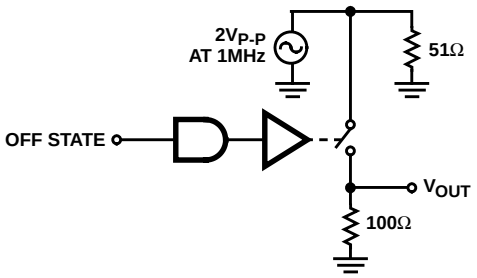


FIGURE 4B. TEST CIRCUIT

FIGURE 4. OFF ISOLATION

Test Circuits and Waveforms (Continued)

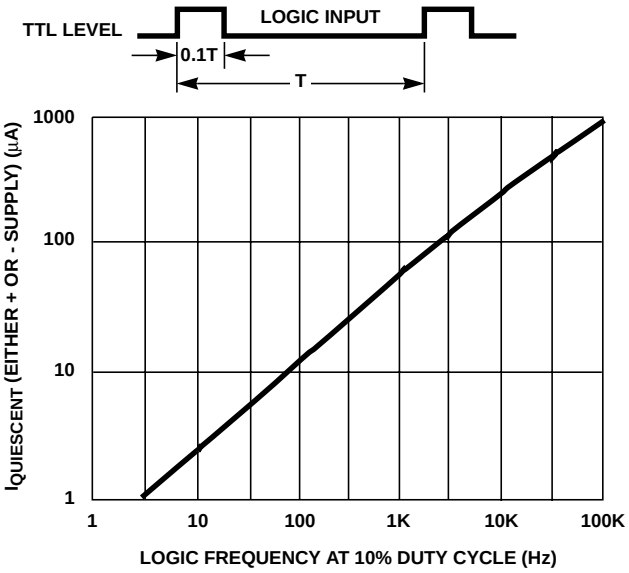


FIGURE 5. SUPPLY CURRENT vs LOGIC FREQUENCY

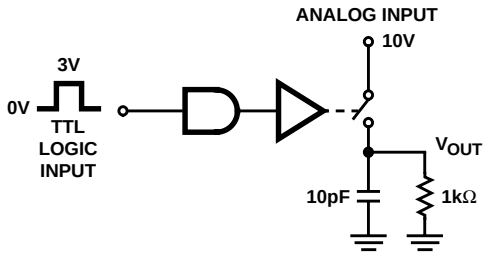


FIGURE 6. t_{ON} AND t_{OFF} TEST CIRCUIT

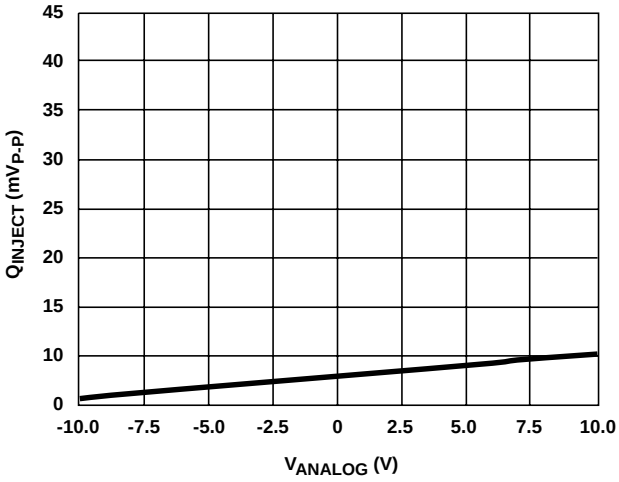


FIGURE 7A. CHARGE INJECTION vs ANALOG INPUT VOLTAGE, C_L = 10nF

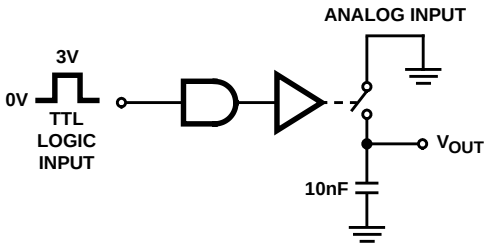


FIGURE 7B. TEST CIRCUIT

FIGURE 7. CHARGE INJECTION

Typical Applications

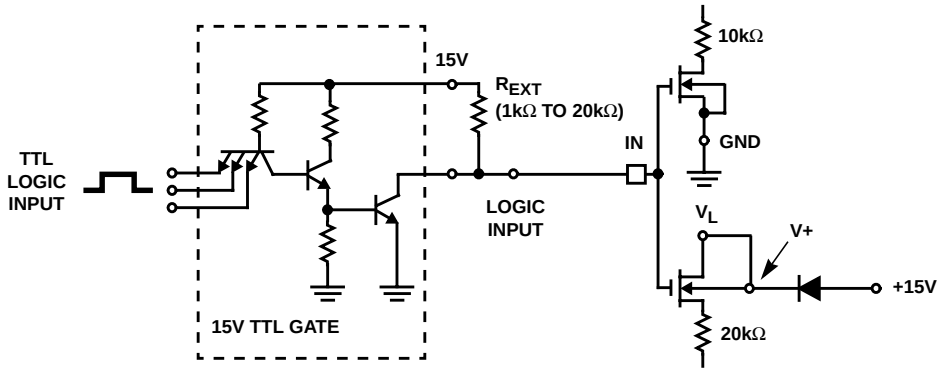


FIGURE 8. +15V OPEN COLLECTOR TTL INTERFACE

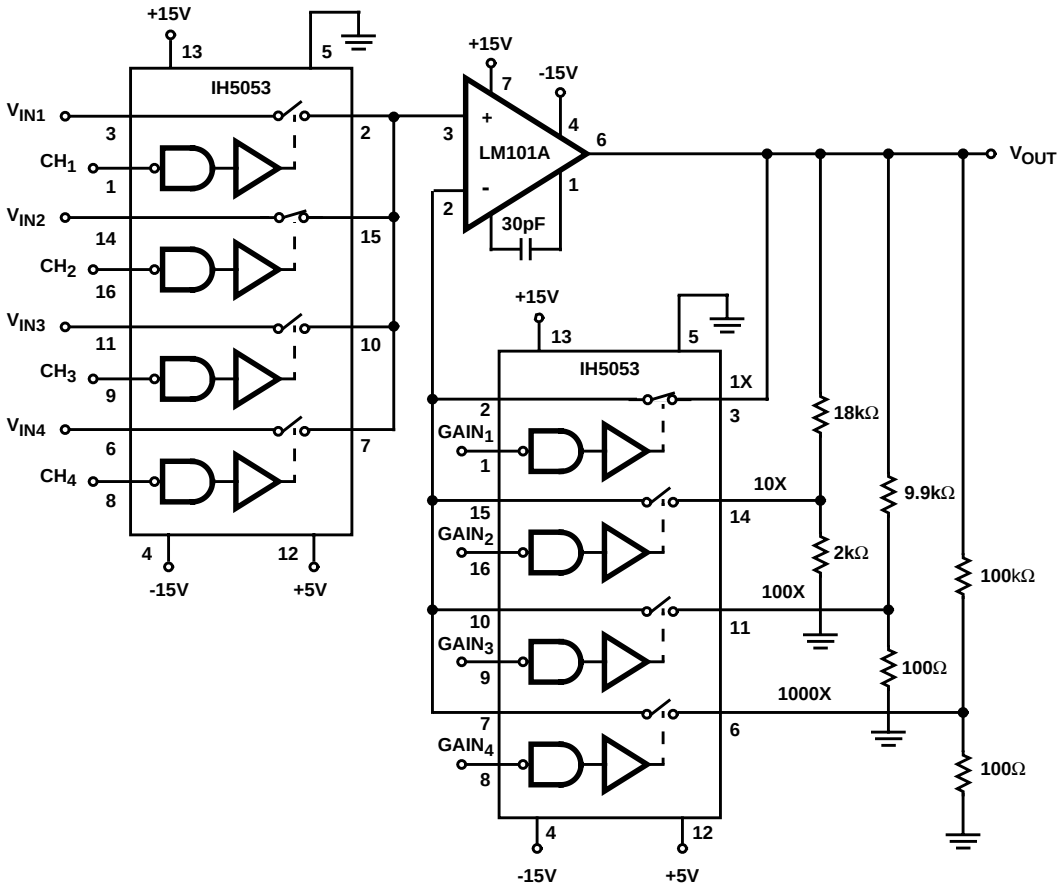


FIGURE 9. ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY