SP8858

1·5GHz Professional Synthesiser

Supersedes March 1997 version, DS3843 - 3.0

DS3843 - 4.1 July 1998

The SP8858 is a single chip synthesiser intended for PLL signal synthesis applications up to 1.5GHz and includes a dual modulus prescaler (÷N/N+1), programmable A, M and R dividers, digital phase detector, charge pump and lock detect circuits.

The SP8858 is a development of the SP8853 synthesiser with low residual phase noise, increased dynamic range above 1GHz and an improved high gain phase detector design that eliminates the dead-band.

The low prescaler modulus, programmable to either 16/17 or 8/9, together with the 15-bit M counter and 13-bit reference counter make this device ideal for a diverse range of high performance applications.

The nominal phase detector gain is set by a reference current into pin 24 and the gain can be varied over a 4:1 range when the device is programmed. The dividers, the phase detector sense, the prescaler modulus and the data buffer control logic are also programmable using the three wire serial interface. An alternative 22-bit control word for the A and M dividers and phase detector gain can be stored so allowing fast frequency hopping and bandwidth switching by simply toggling the logic level on pin 13 (F1/F2). In addition, the A counter of the 'active' buffer can be programmed with only 6 bits, allowing fast hopping to adjacent channels.

A simple exclusive - or lock detect circuit is also provided, the sensitivity of which is determined by an external capacitor.

FEATURES

- Low Residual Phase Noise (see Reference 1)
- Operation to 1·5GHz over Full Temperature Range
- High Input Sensitivity
- Improved Linear Digital Phase Detector
- Programmable Charge Pump Current: 10µA to 2 mA
- On-chip ÷16/17 or ÷8/9 Dual Modulus Prescaler
- Three-wire Serial Data Interface
- 13-bit Reference Counter
- 15-bit M Counter
- Stores an Alternative Programming Word
- Facility to Program A counter Only
- Power Saving Standby Mode

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−0·3V to +7V
Storage temperature	−65°C to +150°C
Operating temperature	−55°C to +125°C
Prescaler input voltage	2·5V p-p

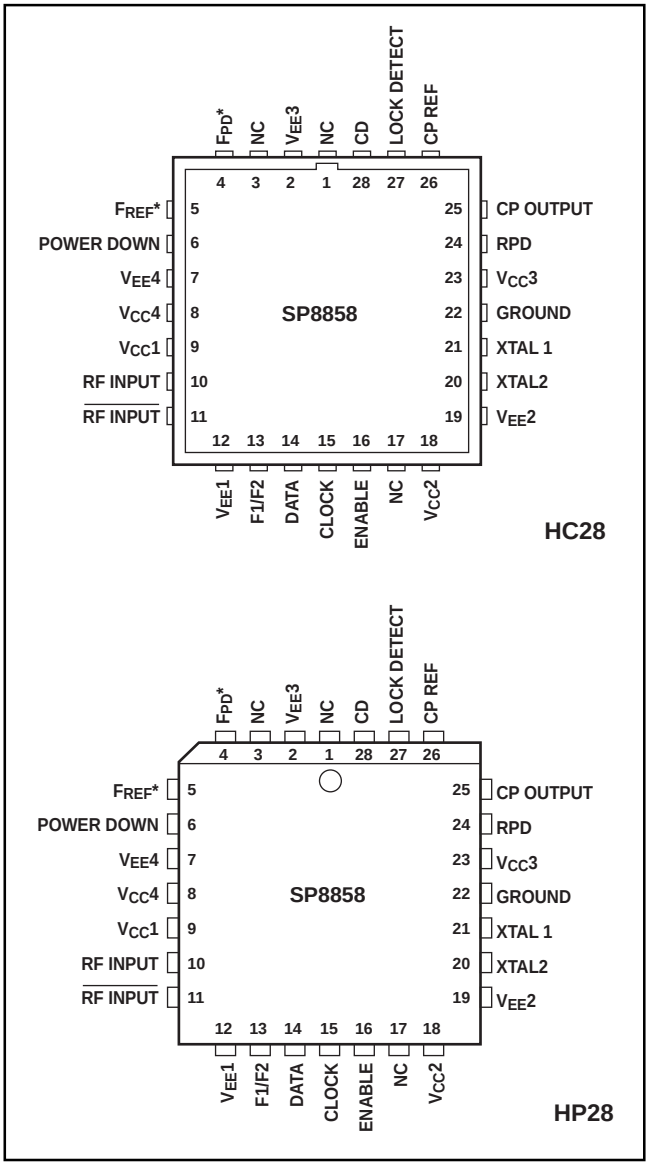


Fig. 1 Pin connections (top view)

ORDERING INFORMATION

SP8858 IG HCAR −40°C to +85°C (Industrial grade)
SP8858 MG HCAR −55°C to +125°C (Military grade)
SP8858 IG HPAS −40°C to +85°C (Industrial grade)

Pin	Description
4	F_{PD} = M divider output pulses = RF input frequency ÷ (MN + A) when SENSE bit in the programming word = '0'. When SENSE bit = 1, this pin is F_{REF} = R divider output pulses = reference input frequency ÷ R. (see Data Entry and Control description and Fig. 6).
5	F_{REF} = R divider output pulses when SENSE bit in the programming word = '0'. When SENSE bit = 1, this pin is F_{PD} = M divider output pulses (see Data Entry and Control description and Fig. 6).
6 (POWER DOWN)	With this pin held high the device is in the power saving standby mode. The serial interface shift register and data buffers remain active at all times so that the device can still be programmed in this mode.
10, 11 (RF INPUT)	Balanced inputs to the RF preamplifier. For single ended operation the signal is AC coupled into pin 11 with pin 10 decoupled to ground or vice-versa.
13 (F1/F2)	The logic level on this input determines which of the two words stored in the internal buffers is used to reload the A and M dividers at the end of the count cycle. With F1/F2 high the F1 buffer is selected.
14 (DATA)	Serial data on this line is clocked into a shift register under control of CLOCK and ENABLE.
15 (CLOCK)	Clocks the data into the shift register.
16 (ENABLE)	Logic high on this pin allows data to be clocked into the shift register and the subsequent falling edge loads the buffer chosen by the LSBs of the programmed word. The clock input is ignored when ENABLE is low.
20 (XTAL 2)	This pin is the input to a buffer amplifier if an external reference signal is provided. Alternatively, the amplifier provides the active element for a reference oscillator if a quartz crystal is connected at this point (see Applications).
21 (XTAL 1)	Leave open circuit if an external reference is used or connect load capacitors for the chosen crystal (see Applications)
24 (RPD)	An external resistor connected between this pin and V_{CC} sets the charge pump output current. A multiplication factor can also be programmed into the device (see Table 3)
25 (CP OUTPUT)	The phase detector output is a single-ended charge pump sourcing or sinking current to the inverting input of an external loop filter.
26 (CP REF)	Connected to the non-inverting input of the loop filter to set the DC bias.
27 (LOCK DETECT)	A current sink into this pin is enabled when the lock detect circuit indicates lock. Used to give external indication of phase lock.
28 (CD)	A capacitor connected to this point determines the lock detect integrator time constant and can be used to vary the sensitivity of the phase lock indicator.
9 ($V_{CC}1$), 12 ($V_{EE}1$)	Pre-amp and prescaler supply.
18 ($V_{CC}2$), 19 ($V_{EE}2$)	Oscillator supply.
23 ($V_{CC}3$), 2 ($V_{EE}3$)	Charge pump supply.
8 ($V_{CC}4$), 7 ($V_{EE}4$)	ECL supply.

Table 1 Pin descriptions

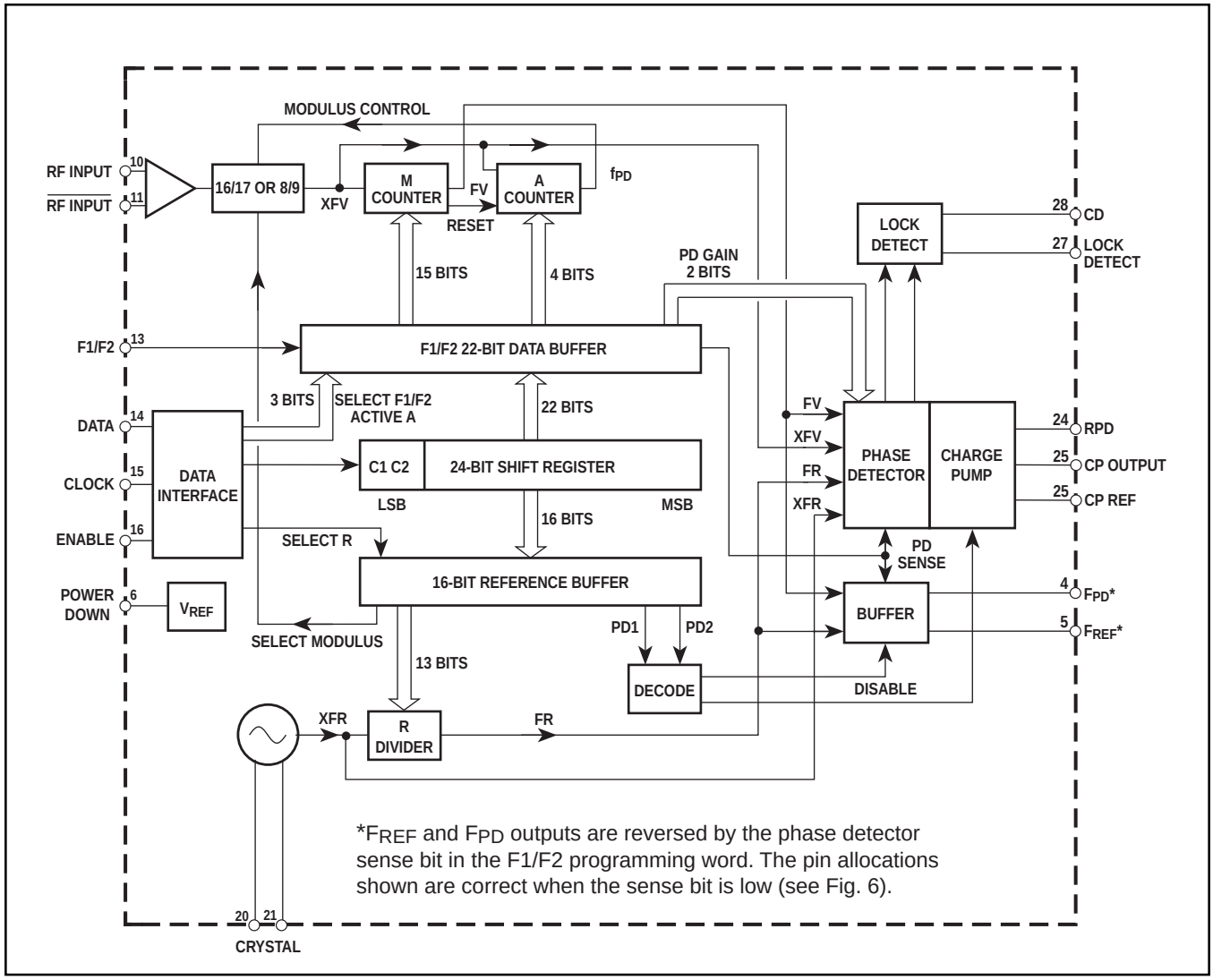


Fig. 2 SP8858 block diagram

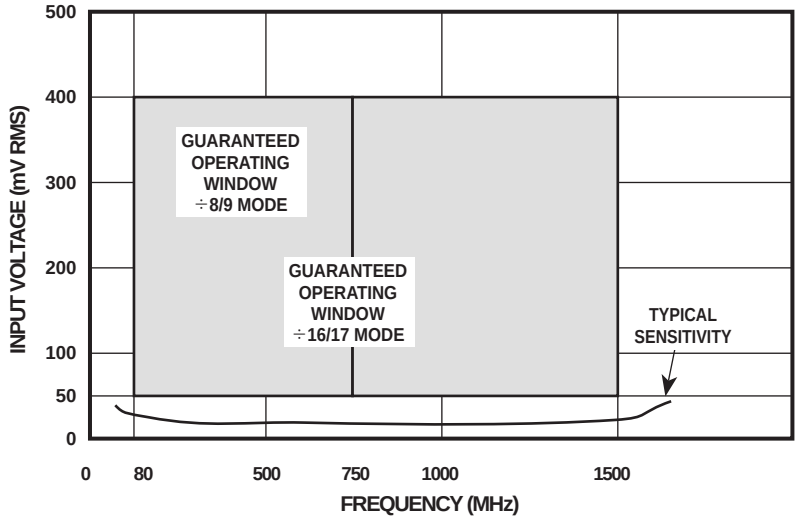


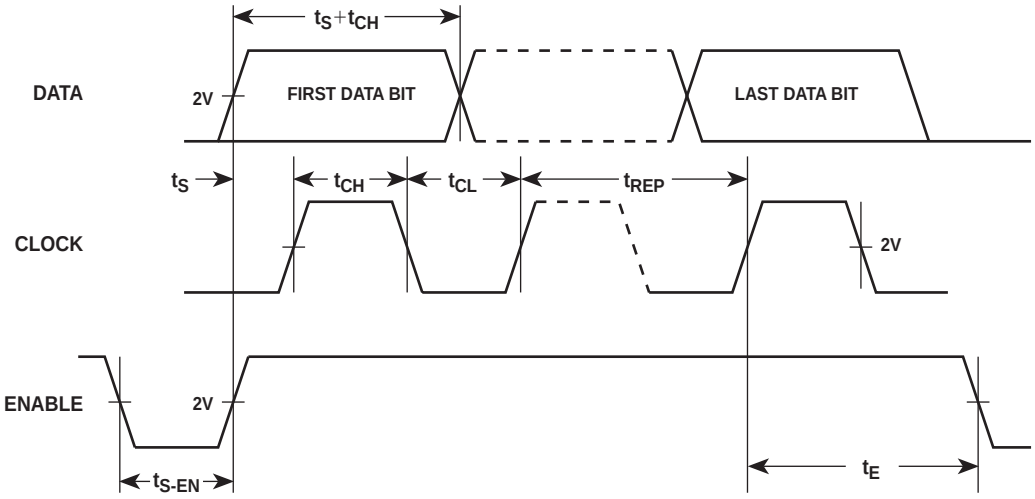
Fig. 3 Typical input characteristics and input drive requirements

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following range of operating conditions unless otherwise stated:
Supply voltage V_{CC} = +4·75V to +5·25V. T_{AMB} = −55°C to +125°C (Military), −40°C to +85°C (Industrial)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8,9,18,23		95	110	mA	
Supply current in power down mode	8		35	45	mA	
Input sensitivity	10,11			50	mVrms	See Fig. 3
Input overload	10,11	400			mVrms	See Fig. 3
RF input division ratio	10,11,4	240		524287		With ÷16/17 selected
		56		262143		With ÷8/9 selected
Comparison frequency	4,5			5	MHz	
Reference oscillator input frequency	20,21	4		40	MHz	See note 1
External reference input voltage	20	50		600	mVrms	
Reference division ratio	20,5	1		8191		
Data clock repetition rate, t_{REP}	15			200	ns	See Fig. 4
Minimum setup time, t_S	14,15	50			ns	See Fig. 4
DATA input high	14	$0{\cdot}6V_{CC}$		V_{CC}	V	
DATA input low	14	V_{EE}		$0{\cdot}3V_{CC}$	V	
CLOCK input high	15	$0{\cdot}6V_{CC}$		V_{CC}	V	
CLOCK input low	15	V_{EE}		$0{\cdot}3V_{CC}$	V	
ENABLE high	16	$0{\cdot}6V_{CC}$		V_{CC}	V	
ENABLE low	16	V_{EE}		$0{\cdot}3V_{CC}$	V	
F1/F2 input high	13	$0{\cdot}6V_{CC}$		V_{CC}	V	F1 buffer selected
F1/F2 input low	13	V_{EE}		$0{\cdot}3V_{CC}$	V	F2 buffer selected
POWER DOWN input high	6	$0{\cdot}6V_{CC}$		$0{\cdot}9V_{CC}$	V	
POWER DOWN input low	6	V_{EE}		$0{\cdot}3V_{CC}$	V	
F1/F2 input current	13			5	µA	V pin 13 = 5·0V
POWER DOWN input current	6			5	µA	V pin 6 = 4·5V
Current into RPD	24	50		500	µA	
Charge pump current	25			2	mA	500µA×4
Charge pump current accuracy	25			±5	%	
Charge pump leakage	25		2	5	µA	Charge pump current = 2mA
LOCK DETECT output voltage when in lock	27			1	V	I pin 27 < 3mA
F_{PD} and F_{REF} output voltage swing	27		0·9			V_{CC} = 5V, external pulldown may be required
LOCK DETECT output resistor	27		50		kΩ	

NOTE 1. The reference frequency range when using a crystal oscillator is 4-20MHz.



t_{REP} = t_{CH} + t_{CL} MIN
t_S = 50ns MIN
t_{CH} = 100ns MIN
t_{CL} = 100ns MIN
t_E = 50ns MIN
t_{S-EN} = [(3+M)N+A]÷RF INPUT (Hz)+50ns
OR 1÷REFERENCE (Hz)+50ns
WHICHEVER IS APPROPRIATE
(SEE DATA ENTRY AND CONTROL)

Fig. 4 DATA, CLOCK and ENABLE timing requirements

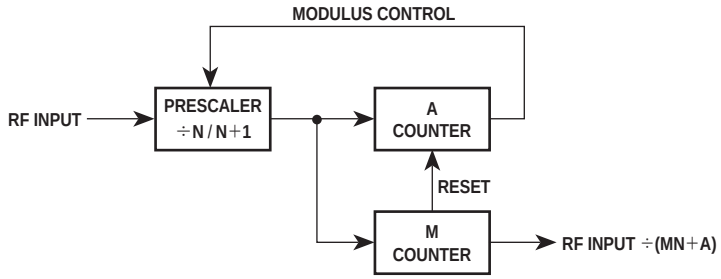


Fig. 5

DESCRIPTION

Prescaler and Dividers

The block diagram of a dual modulus divider arrangement is shown in Fig. 5. The N/N+1 prescaler, together with the A and M dividers, divide the RF input frequency down to the comparison frequency at the phase detector input. The comparison frequency, F_{REF}, sets the resolution of a single loop synthesiser; when A is incremented (or decremented) by one, the loop output frequency automatically increments (or decrements) by F_{REF} Hz. When the dividers are reset, at the end of each count cycle, the modulus of the prescaler is set to N+1 and the input frequency to the A and M dividers is then RFinput ÷(N+1) Hz. The output of the A counter controls the prescaler modulus, which is set to N when A reaches its programmed value. The M divider continues to count at the rate RFinput ÷N until it reaches its programmed value, at which point the dividers are reset and the count cycle starts again. The division ratio of this arrangements is therefore

$$A(N+1) + (M-A)N = MN+A$$

It is evident that for this arrangement to work M must always be programmed greater than or equal to A and A must be able to count to N−1. These restrictions set a minimum count of N^2-N; below this value some division ratios will not be available.

The SP8858 prescaler can be set to ÷8/9 or ÷16/17 mode by setting the appropriate bit of the reference word. The A divider is a 4-bit counter, whilst the M divider is a 15-bit counter. The minimum division ratio, with the 8/9 prescaler, is $8^2-8 = 56$, whilst the maximum division ratio, with the 16/17 prescaler, is $16(2^{15}-1)+(2^4-1) = 524287$.

If the 8/9 prescaler is used the MSB of the A counter must be programmed to 0 and the maximum RF input frequency must be reduced to 750MHz.

Reference Source and Divider

The reference source for the SP8858 is obtained from an on-chip oscillator, stabilised by an external quartz crystal. The oscillator circuit will also function as a buffer amplifier if an external reference is preferred. In the latter case the signal, should be AC coupled into pin 20 (see Fig. 12).

The reference oscillator drives a divider stage, the output of which is the reference signal to the phase comparator. The PLL controls the input voltage to an external VCO so that the divided VCO signal is phased locked to this reference signal. The dynamics of the control loop are determined by the external loop filter.

The 13-bit reference divider is fully programmable and can be set to any ratio between 1 and 8191. The programmed word is stored in the internal reference buffer.

Phase Comparator and Charge Pump

The digital phase detector is sensitive to frequency and phase errors. The basic circuit for a conventional digital phase/frequency detector is based on two D type flip-flops. Initially the flip-flops are reset, each one is then set by the respective pulses of the M and R divider outputs. When both flip-flops have been set they are immediately reset. In this way the output of one flip-flop is a pulse whose width is proportional to phase difference, whilst the second flip-flop is a narrow pulse determined by the time to reset. The phase detector outputs drive a charge pump amplifier. One output controls a constant current source, the other an identical current sink connected to the same node (CP output, pin 25). The SP8858 phase/frequency detector has been modified and improved to provide a linear characteristic, thus eliminating deadband effects.

The phase detector gain is determined by the output current from the charge pump ($\pm I_{OUT}$) which is set by a reference current into pin 24 (RPD). An external transimpedance amplifier is required to provide the voltage drive to the VCO. This requirement is usually performed by the loop filter operational amplifier which is designed to provide a type II third order control loop.

Data Entry and Control

The SP8858 is programmed using the serial data interface. Data is entered into the chip on the DATA pin and clocked into the internal shift register by the positive going edge of the CLOCK signal with the ENABLE pin held high. While ENABLE is high, changes to the shift register will not affect the current count cycle. On the falling edge of ENABLE the data held in the shift register is transferred to one of the three buffers (F1, F2 or reference). Fig. 4 shows the timing requirements for these three signals.

The 2 LSBs of the 24-bit shift register, C1 and C2, determine which of the three buffers is loaded with the data held in the remaining 22 bits as shown in Table 2.

2-bit SR contents		Buffer loaded
C2	C1	
0	0	F1
1	0	F2
0	1	Active A (only the A divider of the active buffer is changed)
1	1	Reference

Table 2

If the F1 buffer (C2 = 0, C1 = 0) is selected the 22 MSBs of the shift register are transferred to it. 19 bits of the buffer provide the data for the A and M dividers; the three remaining bits control the charge pump current multiplication factor and the sense of the phase detector. The F2 buffer performs the same function so that an alternative divider word and/or phase detector gain can be stored.

The CP current can be multiplied by up to four times by programming bits G1 and G2 as shown in Table 3. The maximum charge pump output current is ±2mA.

The reference current can be set by resistor RPD connected between V_{CC} and pin 24 so that:

Ipin 24 = $(V_{CC}-1{\cdot}5)$/RPD
I_{OUT} = G×Ipin 24 (G is multiplication factor)
Phase detector gain, $K_{PD} = I_{OUT}/2\pi$ A/rad

See Applications, Loop Filter Design

F1 or F2 word		Charge pump 1 current (μA)	Charge pump 2 multiplier
G2	G1		
0	0	50	1
1	0	75	1·5
0	1	125	2·5
1	1	200	4

Table 3 Charge pump currents

When the SENSE bit is set to 1 the inputs and clocks to the phase detector flip-flops are reversed. The bit should be set to 1 for a VCO with a positive frequency v. voltage characteristic. The sense bit also swaps the outputs FREF and FPD on pins 4 and 5. Fig. 1 shows the pin-out for SENSE = 0.

The active buffer, i.e. the one that is currently used to update the dividers, is selected at pin 13 (F1/F2). A high on this pin selects F1. The F2 word can be updated while F1 is

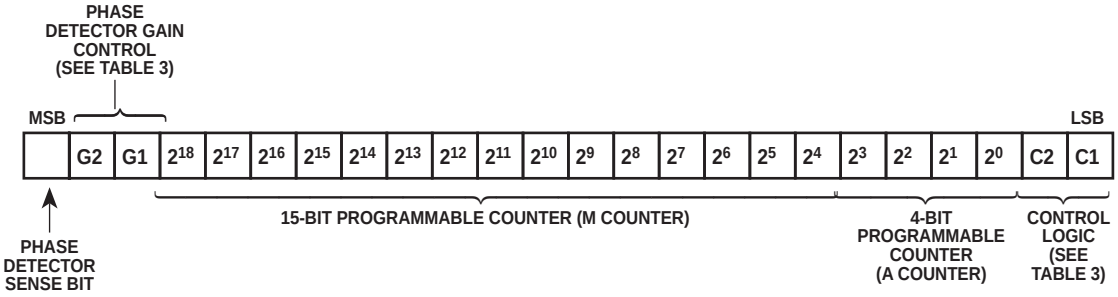


Fig. 6a F1 or F2 word, bit allocation with ÷16/17 selected

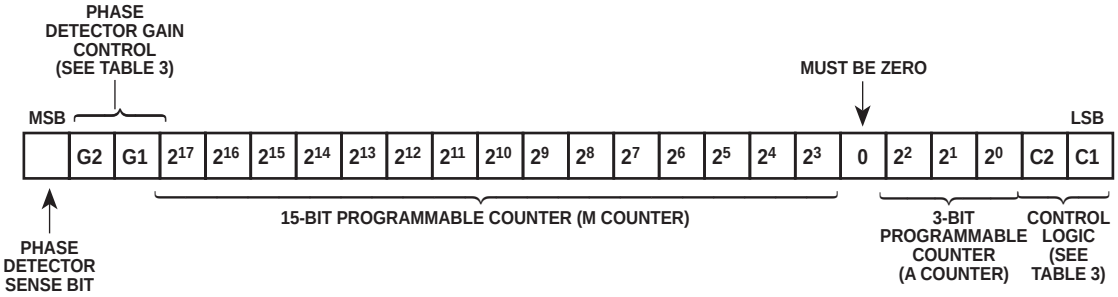


Fig. 6b F1 or F2 word, bit allocation with ÷8/9 selected

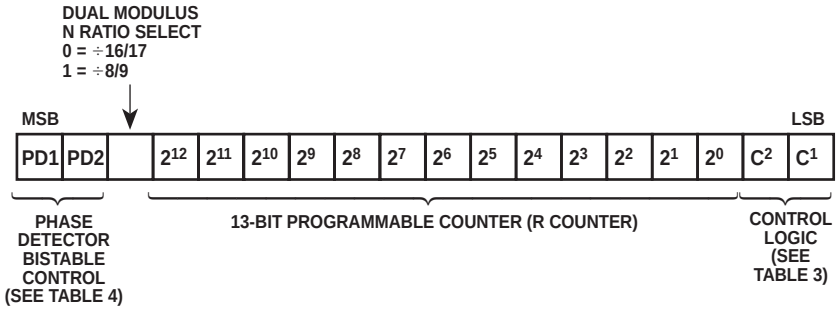


Fig. 6c Reference word bit allocation

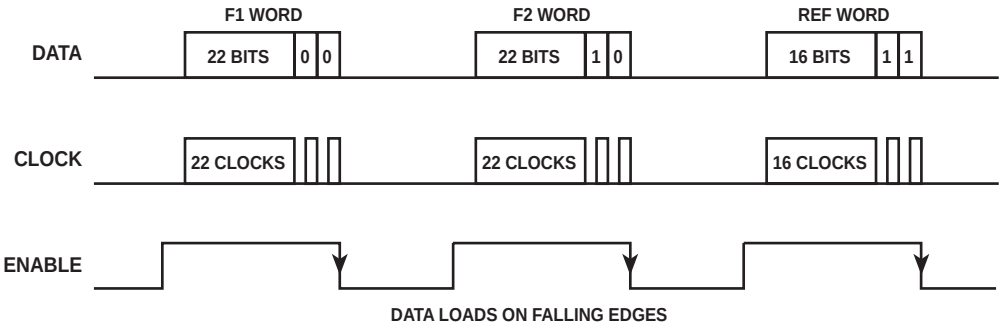


Fig. 6d Data load sequence

Fig. 6 Data formats

controlling the dividers without disrupting the loop (and vice versa). This facility can be used to reduce synthesiser switching time by preparing the non-active buffer prior to the instant of switching and can also be used to modify the open loop gain.

To ensure reliable data is loaded into the dividers the internal control circuits ensure that the buffer data can only be updated if the remaining M count is greater than 3. Given this restriction, the maximum time taken to update the buffer after the negative going ENABLE transition (or after F1/F2 has been toggled) is:

$$[(3+M)\ N+A]/\text{RF input}+50\text{ns}$$

where update time is in seconds and RF input is in Hz.

The time taken to re-program the shift register (F1or F2) is determined by the clock rate and the number of bits required and is equal to:

$$24\times t_{REP}+t_S+t_E \text{ (see Fig. 4)}$$

If the reference buffer is selected (C2 = 1, C1 = 1), only the 16 LSBs of the shift register are used. 13 bits provide the data for the Reference divider. Two bits, PD1 and PD2, control the charge pump and the divider output buffer as shown in Table 4.

PD2	PD1	Result
0	0	F_{REF} and F_{PD} outputs off, charge pump on
0	1	F_{REF} and F_{PD} outputs on, charge pump on
1	0	F_{REF} and F_{PD} outputs on, charge pump off
1	1	F_{REF} and F_{PD} outputs on, charge pump disabled by lock detect

Table 4

The remaining bit of the Reference word is used to select the prescaler modulus. A '1' in this position selects the 8/9 mode. Note that when the 8/9 mode is selected the A divider only requires 3 bits; the 4th bit must be set to '0'.

To ensure reliable data is loaded into the dividers the internal control circuits ensure that the buffer data can only be updated if the remaining R count is greater than 1. Given this restriction, the maximum time taken to update the buffer after the negative going ENABLE transition (or after F1/F2 has been toggled) is:

$$1/F_{REF}+50\text{ns}$$

Only 16 bits are required to program the reference buffer, therefore reference programming time t_{REF} is:

$$t_{REF} = 16\times t_{REP}+t_S+t_E \text{ (see fig. 4)}$$

If the Active A mode is programmed (C2=0. C1=1) only the four A divider bits are updated at the end of the M count. The M divider data, multiplication factor and phase detector sense remain unchanged. This can be used to frequency hop to an adjacent channel with the programming time reduced to:

$$\text{Programming time (Active A)} = 6\times t_{REP}+t_S+t_E$$

The programming details discussed above are summarised in Fig. 6.

Lock Detect

A simple Exclusive-OR phase detector together with an integrator and comparator are used to indicate phase lock.

Capacitor CD on pin 28 sets the integrator time constant and hence the sensitivity of the lock detect function. The comparator controls a current sink connected to pin 27 which can be used together with an external LED or resistor to indicate phase lock.

The lock detect can also be used to disable the charge pump by programming PD1 and PD2 of the reference word (Table 4).

APPLICATIONS

Introduction

This section provides the basic information required to implement a complete digital PLL synthesiser based on the SP8858. A typical circuit is shown in Fig. 12 and is available on a demonstration PCB, including a serial programmer. The demonstration board can be used to evaluate the SP8858 and can be readily adapted by the system/RF designer for a specific application to aid in rapid prototype development.

Users of the SP8853 should consult Appendix A for details of the design changes that are required to replace the SP8853 with the SP8858.

PLL Basics

A system level specification for a stable radio signal will include measures of signal stability such as a single sideband phase noise specification and a spurious output specification.

The power spectrum of the composite RF output signal is influenced by a number of factors:

- Residual phase noise of the dividers
- Active loop filter residual noise
- Feedback divider ratio
- Phase detector gain
- VCO signal phase noise and gain
- Reference signal phase noise
- The closed loop root locations (an under damped loop will cause a noise peak)
- Environmental influences such as EMI and power supply noise

A single-loop synthesiser based around the SP8858 is suitable for the synthesis of highly stable, low phase noise signals provided each of the points above are carefully considered.

The block diagram of a simple PLL is shown in Fig. 7.

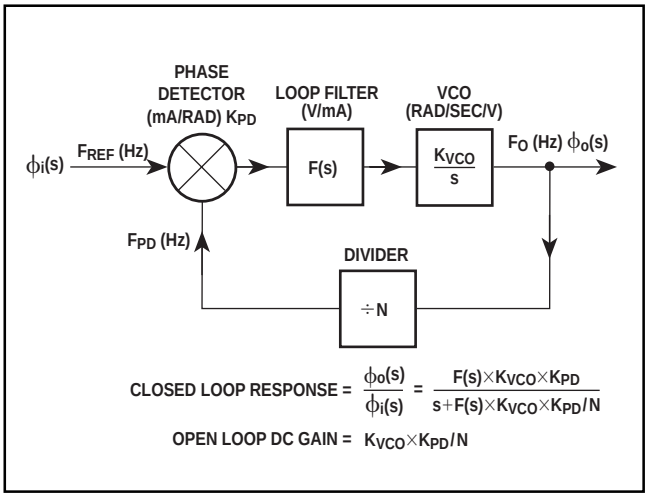


Fig. 7

The basic aim is to phase-lock the VCO signal to a stable reference signal, $\phi i(s)$ and, ideally, set a relatively wide closed loop bandwidth and a high DC loop gain ($K_{PD}\times K_{VCO}/N$). This combination will ensure that the free-running VCO phase noise is attenuated and that both the long-term and the short-term stability of the output signal is determined by the properties of the reference signal. A wide loop bandwidth would also be consistent with the requirement of many synthesiser specifications to change frequency and regain phase lock within a specified time limit. In practice, the following considerations limit the closed loop bandwidth and the DC gain and, consequently, limit the extent to which the ideal system is achieved:

- The divider in the feedback path imposes limitations on the designer because it reduces the DC gain of the loop and also because it unavoidably introduces a measurement error. The contribution to $\phi o(s)$ phase noise power of the $\phi i(s)$ signal, at frequency offsets within the loop bandwidth, is multiplied by N^2 (i.e. increases by 20logN dB); this may impose a specific loop bandwidth for optimum phase noise.
- Physical imperfections in the charge pump and active loop filter circuits force periodic corrections (at the rate of $1/F_{REF}$) when the loop is phase-locked. The resulting disturbance frequency modulates the VCO producing reference sidebands in the output signal spectrum. The closed-loop bandwidth must be much less than F_{REF} for reasonable sideband suppression.

The design of the filter F(s), suitable for any given application, may require careful trade-offs between the requirement to meet the phase noise and the spurious output specification and the settling time specification:

Example 1 In applications where high resolution is required (the resolution is F_{REF} Hz) the imposed closed loop bandwidth (less than F_{REF} Hz) could result in an unacceptably long time to acquire phase lock.
Example 2 If a relatively high feedback division ratio is required the 20logN increase in reference phase noise power, seen at the output, could also impose a relatively narrow closed loop bandwidth and hence a long acquisition time.

The roots of the characteristic equation in the closed loop transfer function, $\phi o(s)/\phi i(s)$, are manipulated through changes to the DC loop gain and the selection of the pole(s) and zero(s) in F(s). Careful mathematical analysis is a prerequisite to successful PLL synthesiser design. If the analysis shows that the simple PLL as shown in Fig.12 is not suitable then there are numerous modifications that can be made to the basic loop and the texts listed in the References should be consulted for more information.

The Mitel Application Note AN194 (Ref. 9) provides specific guidance on noise minimisation and loop filter design for the SP8858 user. The section Loop Filter Design below gives details of the formula that can be used to implement the loop-filter given that the desired second order characteristics are known, i.e. the desired natural loop frequency ω_n and damping factor ζ.

DESIGN IMPLEMENTATION

RF inputs

The availability of a suitable VCO should be considered early in a project because information on the tuning range, the tuning gain in Hz/V and the output noise spectrum is required for the initial mathematical analysis. Variation in the tuning gain over the tuning range should be minimised as this parameter feeds into the closed loop characteristic equation. There is also a trade-off between the requirement for a high tuning gain (which requires the use of a relatively low Q resonator) and phase noise.

The VCO, whether bought in or designed for the application, must also be able to simultaneously drive the SP8858 RF input as well as the input of the next stage in the system. A power splitter and active buffer may be required in some applications. The example in Fig.12 includes a simple resistive power splitter. This type of buffer introduces a 6dB loss but is adequate if the VCO output power is sufficient and if the intention is simply to assess the SP8858 by monitoring the output signal using a 50Ω measurement system.

The SP8858's RF input frequency specification covers the range 80MHz to 1·5GHz and the input impedance varies with frequency; a typical Smith chart is shown in Fig. 8. It is advisable to consider transmission line effects for each individual application and to ensure that the minimum voltage swing at the RF input is within the guaranteed operating range over the full tuning range of the application. The SP8858 incorporates a pre-amplifier at the RF input and the dividers can be seen to operate well below the guaranteed operating range. Fig. 9 shows a typical sensitivity curve as measured on the demonstration board board driven by a 50Ω signal generator (sensitivity is the lowest power level at which the divider operates without mis-counting). The dividers could be more susceptible to spurious interference at low drive levels causing the dividers to mis-count. However, driving the RF input with relatively high levels will ensure greater immunity from interference signals.

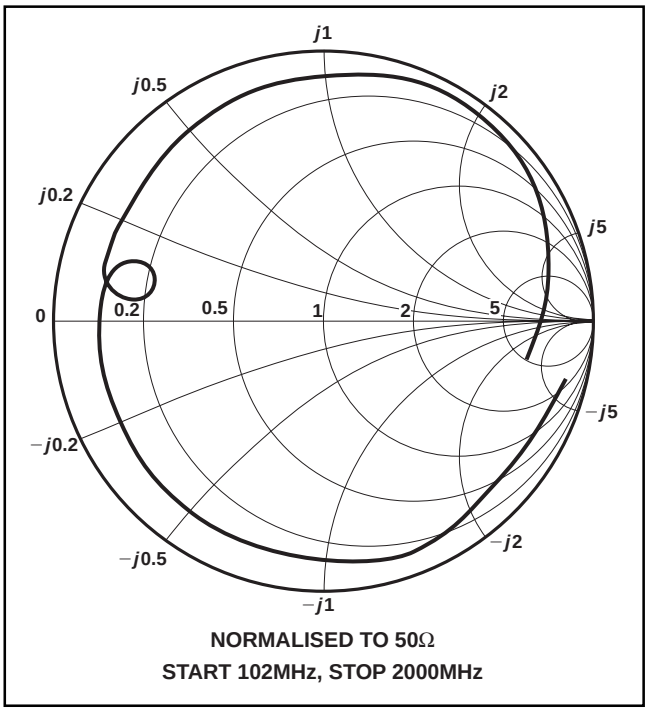


Fig. 8 Demonstration board input impedance

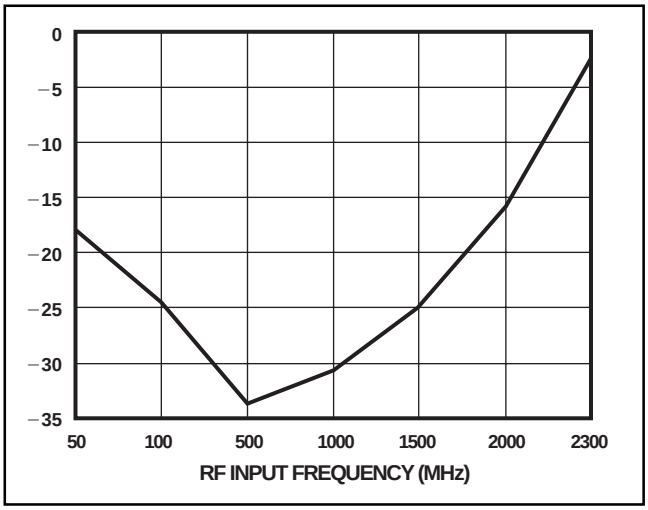


Fig. 9 Typical sensitivity for demo. board at 25°C

Reference Input

When the loop is phase-locked the output signal, Qo(s), takes on the long term stability characteristics of the reference signal. In many applications a crystal stabilised oscillator is adequate as the reference source Qi(s). The VCO output signal is divided down and compared with the reference

signal at the phase detector input. The multiplied reference signal phase noise can set the limit on the achievable close-in phase noise. It is important then that the reference signal is a low phase noise source with good long term stability.

The residual noise of the reference divider is also important because, at some offsets from the carrier, the dividers limit the phase noise reduction that is achievable when the reference signal is divided down to F_{REF}. More detailed advice on phase noise optimisation is given in Ref. 1.

Charge Pump Output

CP OUTPUT (pin 26) and CP REF (pin 5) are connected directly to the inverting and non-inverting input of the loop filter amplifier respectively as shown in Fig. 12. The CP OUTPUT pin will source/sink a current to/from the inverting input equal in magnitude to, or a multiple of, a current reference flowing into RPD (pin 24). The multiplication factor is programmed by two bits (G1 and G2) in the F1 or F2 word (see Data Entry and Control section).

The CP OUTPUT has two stable states. The ON state sourcing or sinking a fixed current and an OFF state in which no current will flow from or into the CP output pin. The proportion of time the charge pump is ON depends on the frequency/phase relationship between the reference signal (divided by R) and the VCO signal (divided by N) at the phase detector input:

- The digital phase detector is sensitive to a frequency difference between the two input signals and will source or sink a constant current for frequency differences.
- When phase-lock is acquired the charge pump current ON/OFF ratio is in direct proportion to the phase difference between the two signals at the phase detector input. Starting from the state 'charge pump OFF' the edge of the leading signal triggers the charge pump into the ON state. The edge of the lagging signal briefly triggers a current at the output which is opposite in sign and equal in magnitude to the current already present before the charge pump returns to the OFF state. When the phase difference reaches zero the input signals simultaneously trigger brief source and sink current pulses which cancel at the output so that zero phase error gives zero output and the deadband is eliminated. The pulse widths are determined by the time taken to reset the internal flip-flops.

In practice, when the loop is phase locked and the charge pump is predominately in the OFF state there are two imperfections to consider:

- The loop filter capacitors discharge during the period of the reference signal.
- A small current leaks into CP OUTPUT in the OFF state at high charge-pump current settings.

A small correction is therefore required each cycle. The resulting disturbance is attenuated by the loop but any residual ripple on the VCO control frequency modulates the VCO causing the characteristic reference sidebands. The magnitude of the sidebands that can be tolerated depends entirely on the application and can be reduced by setting a loop bandwidth very much less than the phase detector comparison frequency (F_{REF}) or by reducing the charge-pump current (the leakage current is negligible for low charge-pump currents).

The charge-pump can be set to source or sink a current for any given phase difference and the SENSE bit in the F1 (or F2) programme word is used to set the appropriate sign for the application. The SENSE bit should be set to 1 for a VCO with a positive frequency versus control voltage characteristic to ensure phase lock.

The actual bias voltage at the CP REF pin varies with the magnitude of the reference current and CP OUT is held at the same voltage by the operational amplifier. A low offset voltage amplifier should be chosen to maintain the match between the reference current into RPD (pin 24) and the actual output current.

The simplest method of setting the reference current is to connect a resistor between RPD and the supply. The voltage at pin 24 is approximately 1·5V but this varies slightly with the magnitude of the current and a simple calculation of Ipin 24 = $(V_{CC}-1{\cdot}5)$/RPD (see Description, Data Entry and Control) is approximate. The voltage at pin 24 will also vary with temperature and the impact of the phase detector gain variations on performance should be assessed in each individual application. If it is considered important to improve the accuracy of the phase detector gain then the use of a constant current source may be more appropriate.

Miscellaneous I/Os

The SP8858 includes simple lock-detect circuit. The output signals from the Reference and RF dividers are used to drive an EXOR type phase detector. The output of this type of detector is logic high if the inputs are at the same voltage level and low if the inputs are polarised. The EXOR gate drives a buffer stage with the output collector loaded with a single 50kΩ on-chip resistor and a capacitor connected externally at pin 28 (CD). The RC serves to integrate the output pulse train from the phase detector. The capacitor voltage must reach a fixed threshold to enable a constant current sink into pin 27.

The inputs POWER DOWN and F1/F2 can either be fixed at the required logic level or controlled by some peripheral circuit. See Table 1 and Fig. 12.

As with any RF design work care must be taken with the power supply layout to and the returns from the IC and the physical position of the PLL on the PCB in relation to potential interference sources. The V_{CC} supply inputs should be connected to a well regulated 5V power supply and locally decoupled; noise on the supply can influence the noise power spectrum of the output signal.

The programming inputs DATA, CLOCK and ENABLE are compatible with standard CMOS and TTL logic and are subject to the timing restrictions shown in Fig. 4.

Loop Filter Design

The linear model of the PLL, as shown in Fig.7, includes an external loop-filter F(s). A filter is required that will:

- Add a zero to the open-loop transfer function thus allowing the designer to manipulate the closed-loop root locations through the appropriate choice of filter components. Without the filter (F(s) = 1) the closed loop is first order with the root locus travelling along the negative real axis with increasing DC gain. In this situation the designer has very little control over the $\phi o(s)/\phi i(s)$ transfer characteristic because the selection of the gain factor $K_{PD}\,K_{VCO}/N$ may, in practice, be limited.
- Introduce a second pole at the origin in order to increase the type number of the loop to type II. This is required to ensure that the steady state error signal tends to zero for a ramp in phase.

In addition, a suitable interface is required to provide the transimpedance function from the charge-pump output to the VCO thus converting the output signal, in the form of current pulses, to the voltage signal required at the VCO input.

The required transfer function is therefore F(s) = (s+a)/s (zero at −a) and the loop filter is implemented using the circuit and formula shown in Fig. 10a. The closed-loop transfer function becomes:

$$\phi o(s)/\phi i(s) = (s\tau_1+1)K_{VCO}K_{PD}/(s^2+s\tau_1 K/C1+K/C1)$$

where $K = K_{VCO}K_{PD}/N$

$\tau_1 = C1R1$

The selection of C1 and R1 is often approached by using the standard representation for the second order characteristic equation: $s^2+2\zeta\omega_n+\omega_n^2$ and selecting the natural-loop frequency and the damping factor ζ to give the desired response. The time constants are calculated using:

$2\zeta\omega_n = \tau_1 K/C1$ and $\omega_n^2 = K/C1$ so that
$C1 = K/\omega_n^2$ and $R1 = 2\zeta\omega_n/K$

Alternatively, the loop filter and formula shown in Fig. 10b can be used to introduce a pole in F(s) at $-1/\tau^2$ which will provide additional roll-off in the closed loop transfer characteristic in order to attenuate the reference sidebands. The closed loop transfer function becomes:

$$\frac{\phi o(s)}{\phi i(s)} = \frac{[s(\tau_1+\tau_2)+1]K_{VCO}K_{PD}}{[C1\tau_2 s^3+C1s^2+K(\tau_1+\tau_2)s+K]}$$

Care must be taken when choosing C2 to ensure that the additional pole does not unduly affect the stability margins of the loop. In practice, a simple and useful rule of thumb is to set the desired second order response as above and then set C2 to be 1/10 of C1. It is advisable when designing third order or higher order loops to use CAD tools to assess stability. Popular analysis tools taken from control theory, such as root locus and Bode diagrams, are useful to aid the design of the closed loop PLL system. AN194 describes these tools in more detail and introduces a loop filter design methodolgy aimed at optimising the phase noise performance.

Loop filter design example

Use the demonstration board to generate a 1GHz signal with a resolution of 500kHz (N = 5000) and reference oscillator frequency of 40MHz. Set natural loop frequency, ω_n, to $2\pi\times10^4$ rad/s and damping factor to 0·7. The MQE001-1016 VCO gain, K_{VCO}, is nominally 25MHz/V. Set the phase detector output current to 2mA so that $K_{PD} = 2\times10^{-3}/2\pi$ A/rad.

Using the above formula, calculate the loop filter R and Cs.

$K = 2\pi\times25\times10^6\times2\times10^{-3}/2\pi\times5000 = 10$
$C1 = 10/(2\pi\times10^4)\times2 \approx 2{\cdot}5\times10^{-9}$
$R1 = 2\times0{\cdot}7\times2\pi\times10^4/10 \approx 8796$
$C2 = C1/10 \approx 0{\cdot}25\times10^{-9}$

Realise the loop filter with C1 = 2·2nF, C2 = 220pF and R1 = 8·2kΩ The single sideband phase noise specturm for this example is shown in Fig. 11.

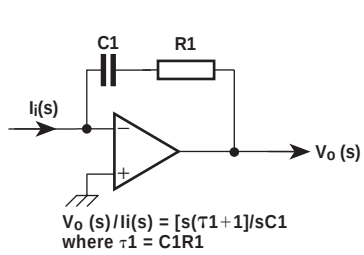


Fig. 10a

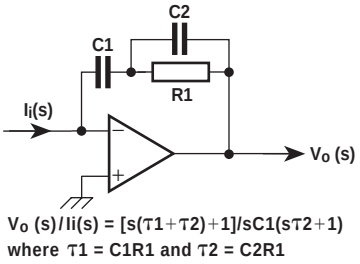


Fig. 10b

Fig. 10 Loop filters

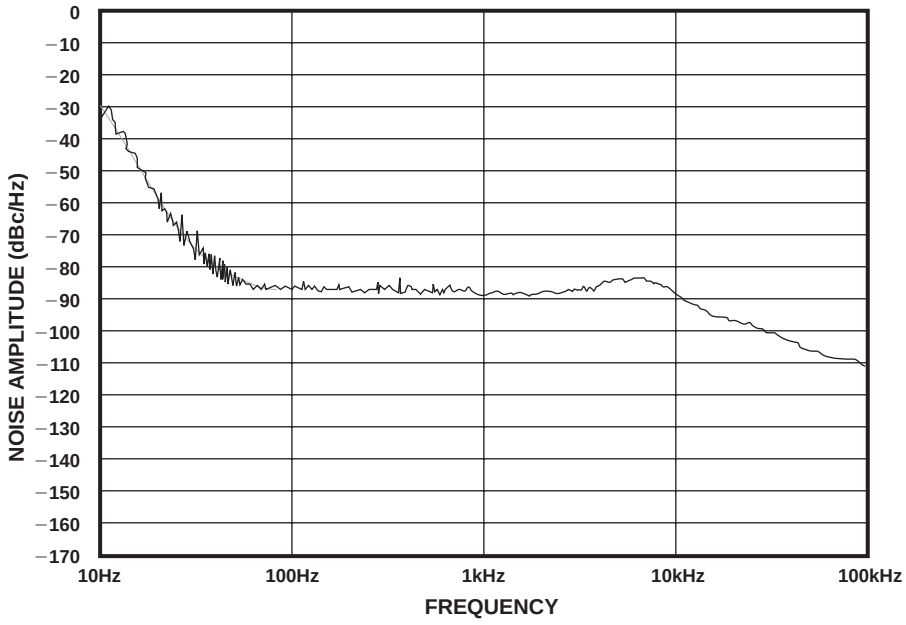


Fig. 11

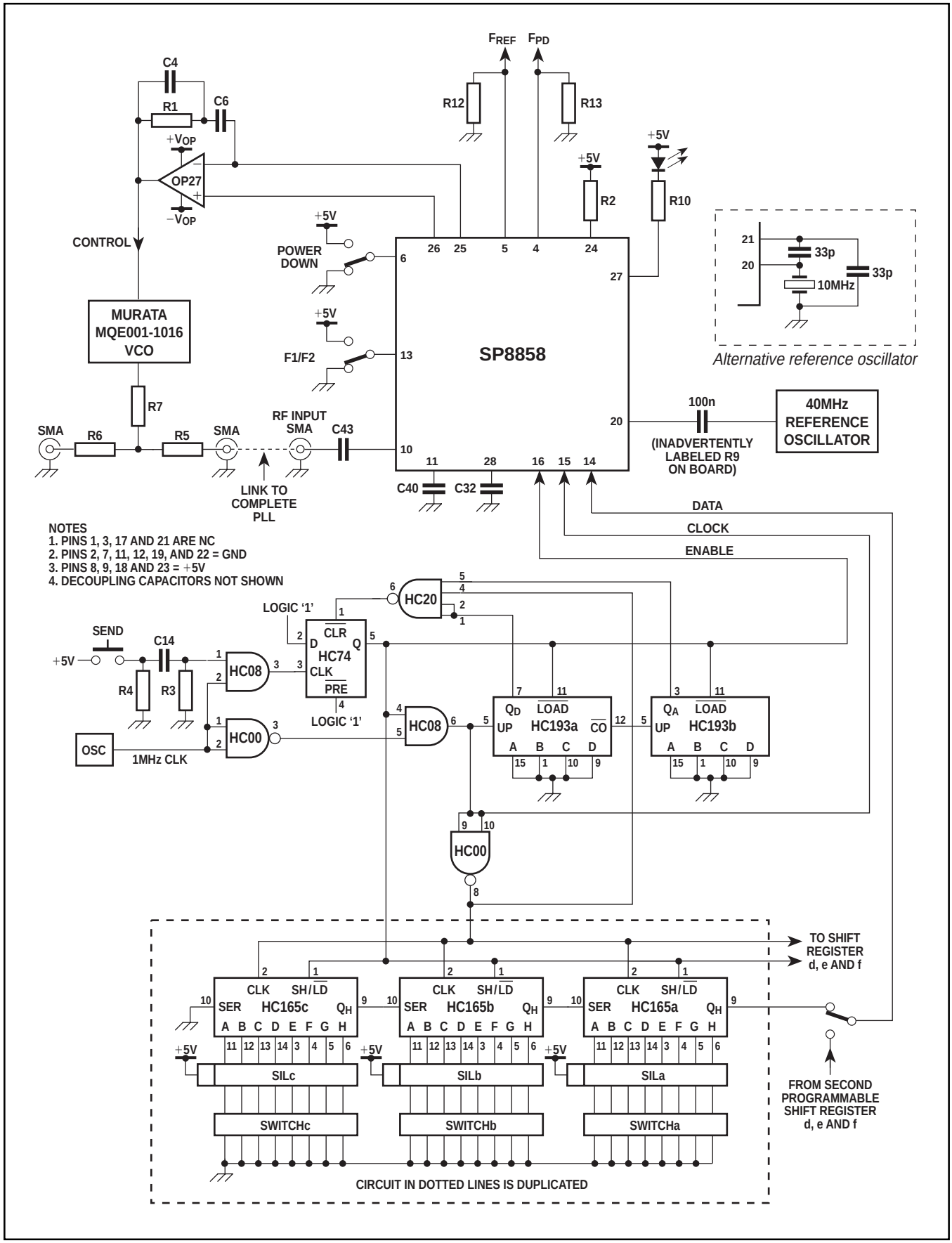


Fig. 12 SP8858 demonstration board

Integrated circuits
SP8858 1·5GHz synthesiser OP27 Operational amplifier HC00 HC08 HC20 HC74 HC165 (6 off) HC193 (2 off)
Leaded resistors and capacitors
R1, C4 and C6: Application specific to define the loop filter characteristic (no components fitted) R2: 6·8kΩ C1, C2, C7 and C10: 10μF Tantalum C3, C5, C8 and C9: 0·1μF Ceramic
Chip resistors (0805)
R3, R12, and R13: 3·3kΩ R4:10kΩ R5, R6 and R7: 15Ω R8: 100Ω R10: 2·2kΩ R11: No component

Chip capacitors (0805)
C11 through C26, C28, C29, C33, C34, C36 through C39, C41 and C42: 0·1μF C14: 1nF C32: 220pF C40 and C43: 100pF C27, C30, C31 and C35: No components
Miscellaneous
Murata MQE001-106 VCO 40MHz crystal oscillator 1MHz clock oscillator for programmer logic PCB keyboard switch (SEND) Slide switches (3 off) (SELECT, F1/F2, POWER DOWN) 16-pin DIL switch (6 off) (SIL a, b, c, d, e and f) SMA PCB mounting socket (3 off)

Table 5. Demonstration board parts list

APPENDIX A: SP8853 TO SP8858

The SP8858 is not a drop-in replacement for the SP8853; minor modifications will be required to a SP8853-based design if the SP8858 is to be used in its place. The changes mainly affect the charge pump output pins as shown in Table 6 below. The SP8858 has only one charge pump output.

In addition the modifications have:

- Increased the operating frequency range for both the RF and reference input
- Simplified the lock detect circuit
- Increased the maximum charge-pump current specification to 2mA. Recalculate the loop filter components using formula in Application section.

Pln No.	SP8853	SP8858
1	Internally connected	NC
3	PD1 output	NC
25	PD2 output	CP OUTPUT
26	NC	CP REF

Table 6

REFERENCES

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2. Gardener F.M., *Phaselock Technique*, Wiley 1979.
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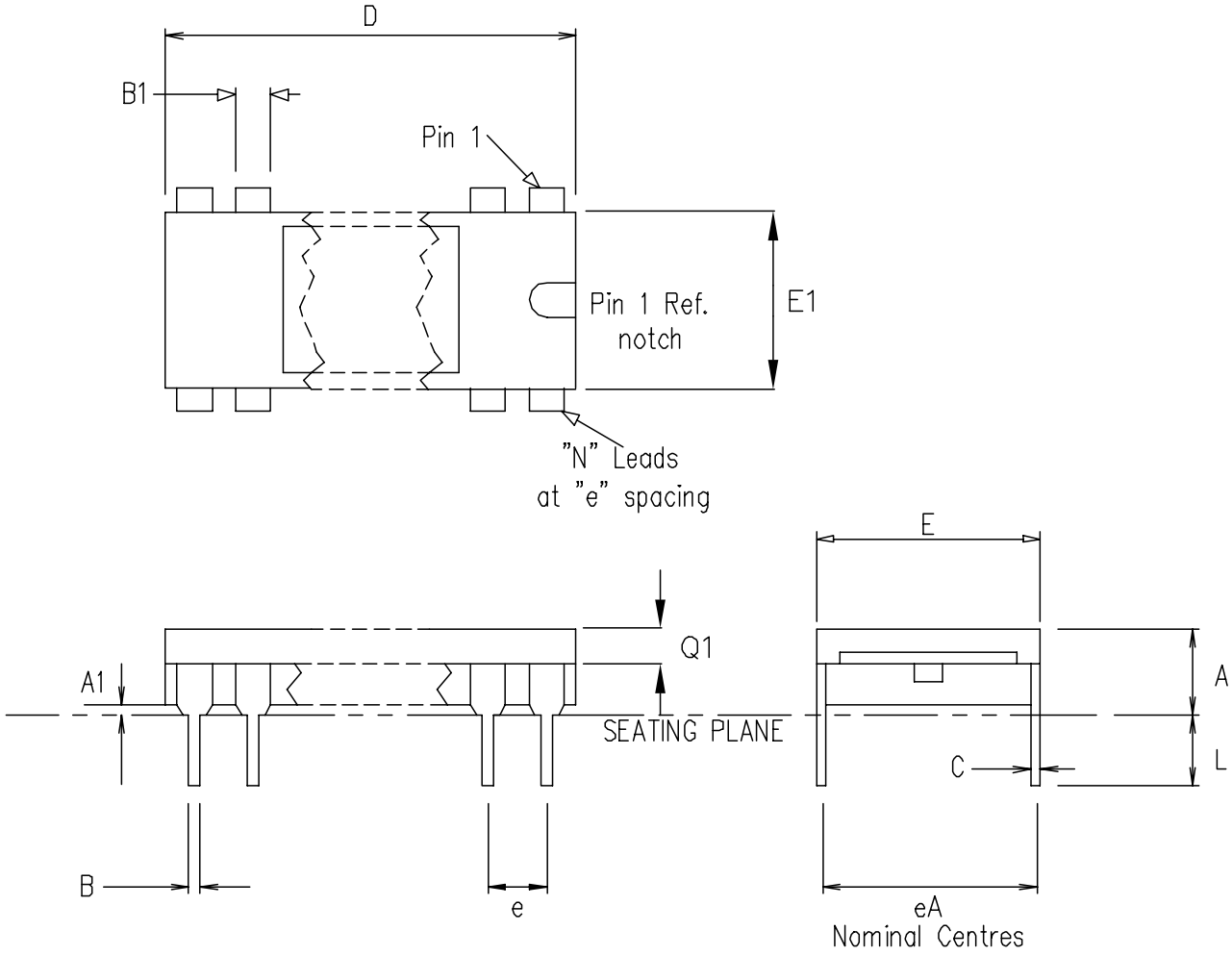


Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.16		5.08		0.085		0.200
A1	0.64		1.78		0.025		0.070
B	0.38		0.56		0.015		0.022
B1	1.14		1.65		0.045		0.065
C	0.23		0.38		0.009		0.015
D	35.05		36.07		1.380		1.420
E	15.24		15.88		0.600		0.625
E	14.73		15.49		0.580		0.610
e	2.54 BSC				0.100 BSC.		
eA		15.24				0.600	
L	3.18		5.08		0.125		0.200
Q1	0.13				0.005		
	Pin features						
N	28						

Conforms to JEDEC MS-015 CB Iss A

Notes:
1. Controlling dimension are in inches.
2. Dimensions A, A1 & L are measured with the package seated in JEDEC seating plane gauge GS-3. Dimension A includes the lid thickness, and may increase to .260 inches maximum when an eprom lid is used.
3. D & E1 dimensions do not include particles (burrs and/or projections) of package material. Such particles shall not exceed .010 inches (.25mm) per side. Includes allowance for glass overrun and meniscus, and lid to base mismatch.
4. E & eA are measured with the leads constrained to be perpendicular to plane C.
5. Maximum lead thickness includes all lead finishes.
6. Minimum base material shall be .009 inches thick.
7. Any raised irregularity on the top surface (step, mass, etc.) shall be symmetrical about the lateral and longitudinal package ceterlines.
8. Q1 is measured from the top of the ceramic body to the nearest metallization or lead.
9. Gold plating 60 micro inches minimum thickness over 100 micro inches nominal thickness of nickel unless otherwise stated on the purchase order.

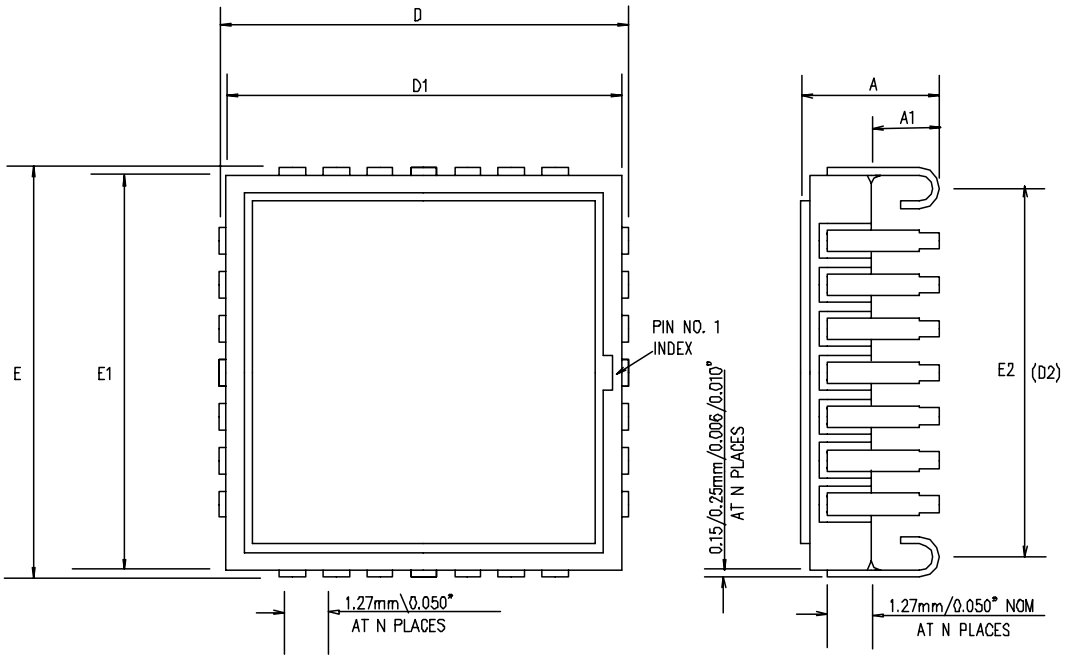
This drawing supersedes 418/ED/39500/008 issue 7 (Swindon)

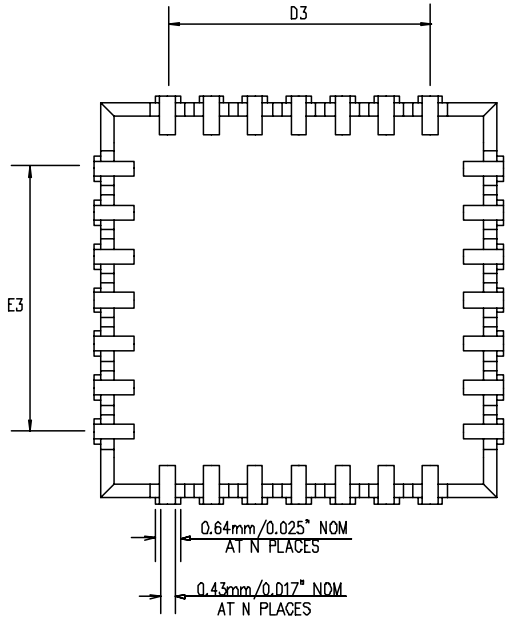
ORIGINATING SITE: SWINDON

ISSUE	1					MITEL SEMICONDUCTOR
ACN	203935					
DATE	22.JAN.98					
APPROVED						

Title: Outline drawing for 28 Lead Sidebrazed (DC)

Drawing Number
GPD00483





Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches	
	MIN	MAX		MIN	MAX
A	3.94	4.11		0.155	0.162
A1	1.98			0.078	
D	11.73			0.461	
D1	11.18	11.68		0.440	0.460
D2	10.16	11.18		0.400	0.440
D3	7.37	7.87		0.290	0.310
E	11.73			0.461	
E1	11.18	11.68		0.400	0.460
E2	10.16	11.18		0.400	0.440
E3	7.37	7.87		0.290	0.310
	Pin features				
N	28				
ND	7				
NE	7				
NOTE	SQUARE				

Note:–
1. This drawing supersedes 418/ED/51186/001 issue 2

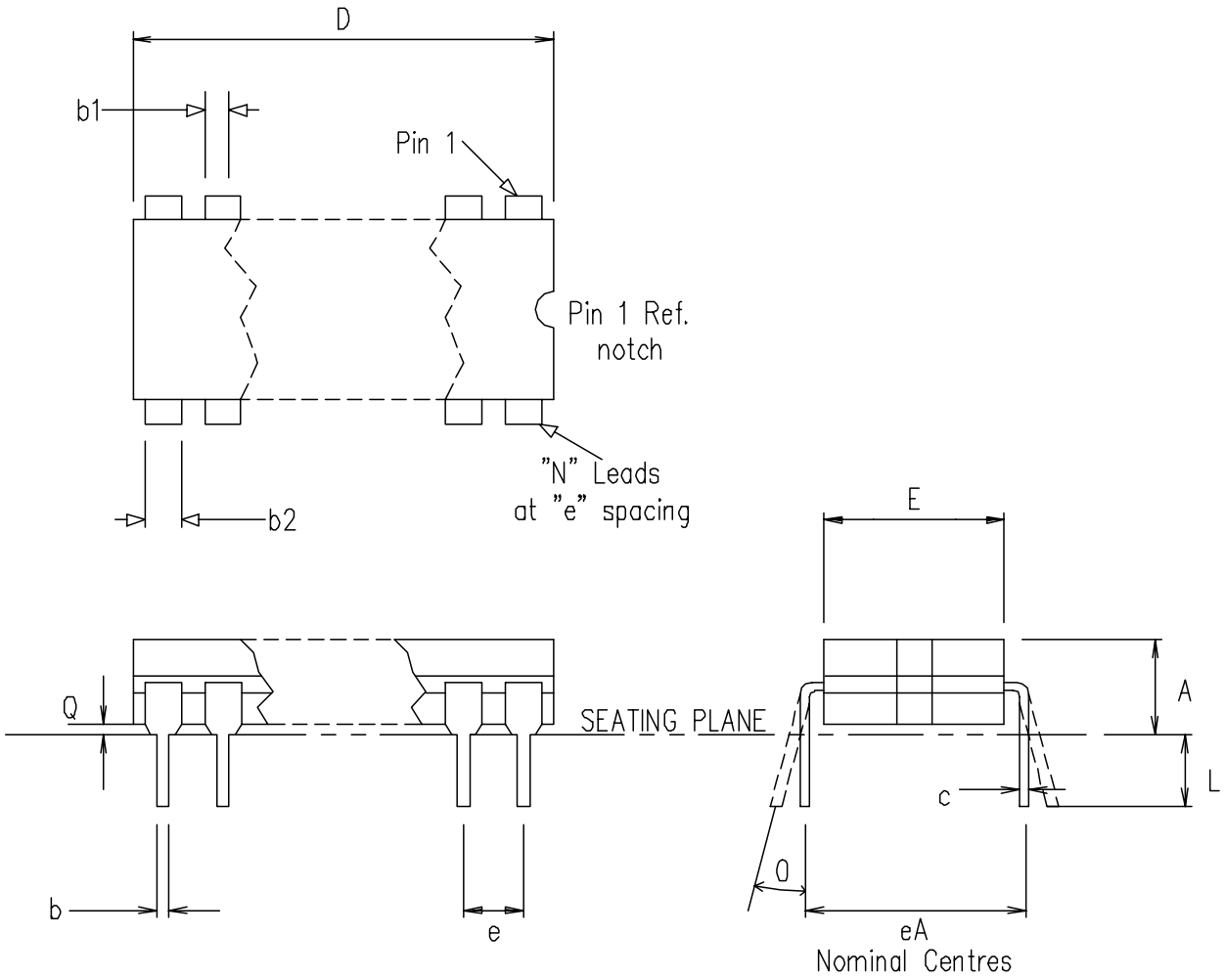
ORIGINATING SITE: Swindon

ISSUE	1				
ACN	207466				
DATE	10SEP99				
APPRD.					

MITEL SEMICONDUCTOR

Title: Outline Drawing for 28 J–LDCC (HC)

Drawing Number
GPD00602



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
L	3.18		4.06		0.125		0.160
A			5.59				0.220
Q	0.51				0.020		
E	12.70		15.49		0.500		0.610
eA		15.24				0.600	
c	0.20		0.36		0.008		0.014
D			38.10				1.500
e	2.54 BSC.				0.100 BSC.		
b1	1.14		1.65		0.045		0.065
b	0.36		0.58		0.014		0.023
b2	0.73		1.12		0.029		0.044
0			15°				15°
	Pin features						
N	28						
ND	14						
NE	0						
NOTE	RECTANGULAR						

This drawing supersedes 418/ED/39501/009 (Swindon)

ORIGINATING SITE: SWINDON

ISSUE	1					MITEL SEMICONDUCTOR
ACN	201736					
DATE	20.NOV.96					
APPROVED						

Title: Outline drawing for 28 Lead Cerdip (DG)

Drawing Number

GPD00281

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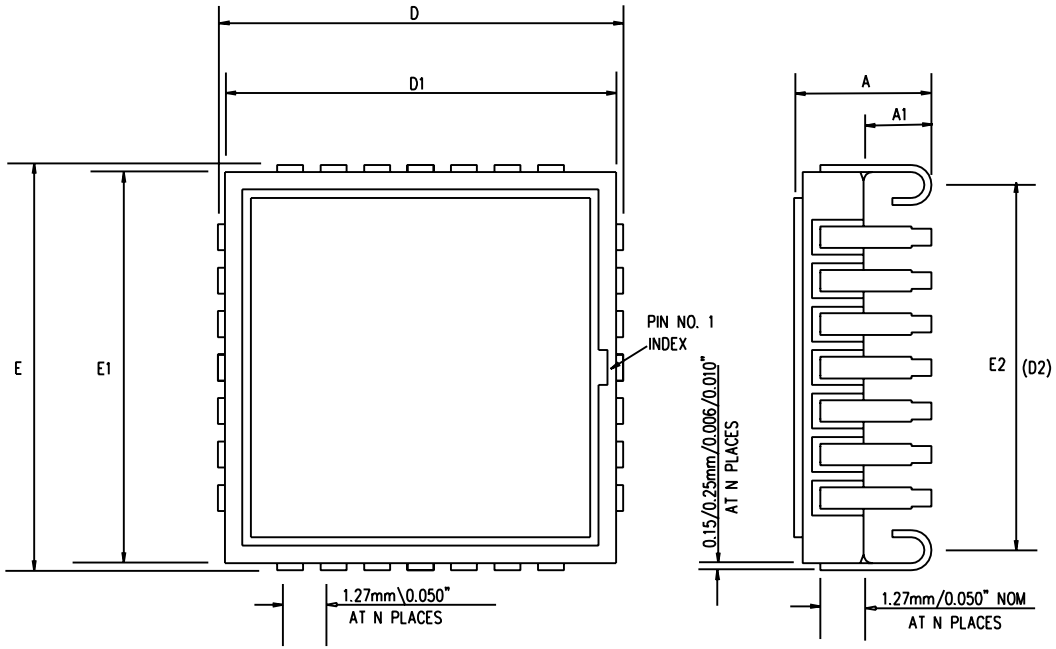
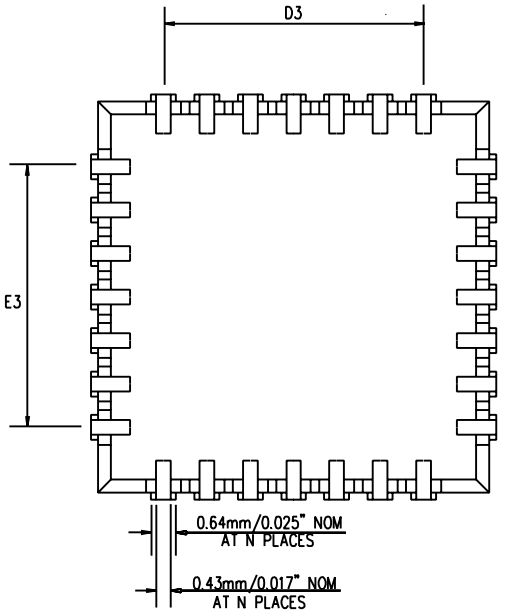




Symbol	Altern. Dimensions in millimetres			Control Dimensions in inches	
	MIN	MAX		MIN	MAX
A	3.94	4.11		0.155	0.162
A1	1.98			0.078	
D	11.73			0.461	
D1	11.18	11.68		0.440	0.460
D2	10.16	11.18		0.400	0.440
D3	7.37	7.87		0.290	0.310
E	11.73			0.461	
E1	11.18	11.68		0.400	0.460
E2	10.16	11.18		0.400	0.440
E3	7.37	7.87		0.290	0.310
	Pin features				
N	28				
ND	7				
NE	7				
NOTE	SQUARE				

Note:-
1. This drawing supersedes 418/ED/51186/001 issue 2

ISSUE	1	2		
ACN	207466	212488		
DATE	10Sep99	8Apr02		
APPRD.				

ZARLINK SEMICONDUCTOR

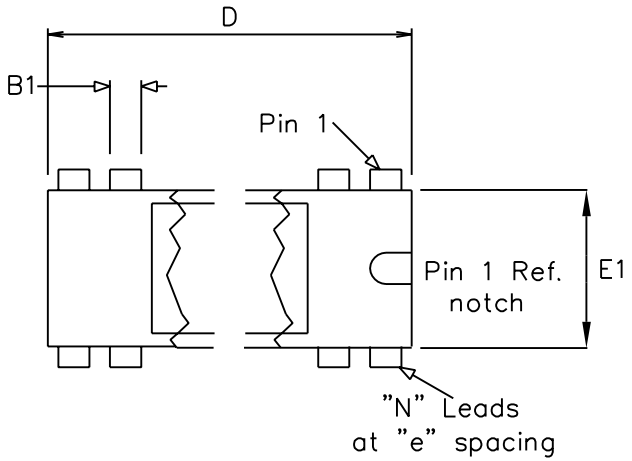
Previous package codes

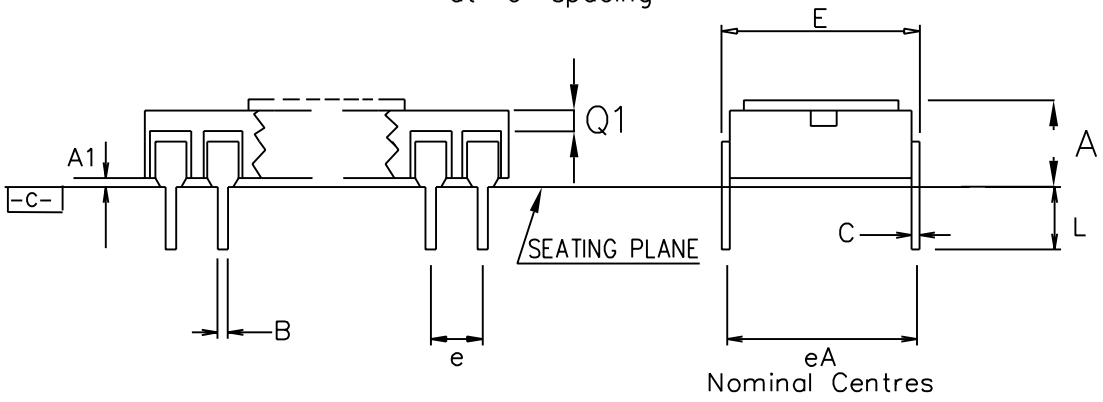
HC / J

Package Code QF

Package Outline for
28 lead J-LDCC

GPD00602





Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.16		5.08		0.085		0.200
A1	0.64		1.78		0.025		0.070
B	0.38		0.56		0.015		0.022
B1	1.14		1.65		0.045		0.065
C	0.23		0.38		0.009		0.015
D	35.05		36.07		1.380		1.420
E	15.24		15.88		0.600		0.625
E1	14.73		15.49		0.580		0.610
e	2.54 BSC				0.100 BSC.		
eA		15.24				0.600	
L	3.18		5.08		0.125		0.200
Q1	0.127				0.005		
	Pin features						
N	28						

Conforms to JEDEC MS-015 CB Iss A

Notes:

1. Controlling dimension are in inches.
2. Dimensions A, A1 & L are measured with the package seated in JEDEC seating plane gauge GS-3. Dimension A includes the lid thickness, and may increase to .260 inches maximum when an eprom lid is used.
3. D & E1 dimensions do not include particles (burrs and/or projections) of package material. Such particles shall not exceed .010 inches (.25mm) per side. Includes allowance for glass overrun and meniscus, and lid to base mismatch.
4. E & eA are measured with the leads constrained to be perpendicular to plane C.
5. Maximum lead thickness includes all lead finishes.
6. Minimum base material shall be .009 inches thick.
7. Any raised irregularity on the top surface (step, mass, etc.) shall be symmetrical about the lateral and longitudinal package ceterlines.
8. Q1 is measured from top of ceramic body to nearest metallization or lead.
9. Gold plating 60 micro inches minimum thickness over 100 micro inches nominal thickness of nickel unless otherwise stated on the purchase order.
10. Shape of lead shoulders may vary from that illustrated.

This drawing supersedes 418/ED/39500/008 issue 7 (Swindon)

ISSUE	1	2	3	
ACN	203935	208022	212485	
DATE	22Jan98	15Dec99	5Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

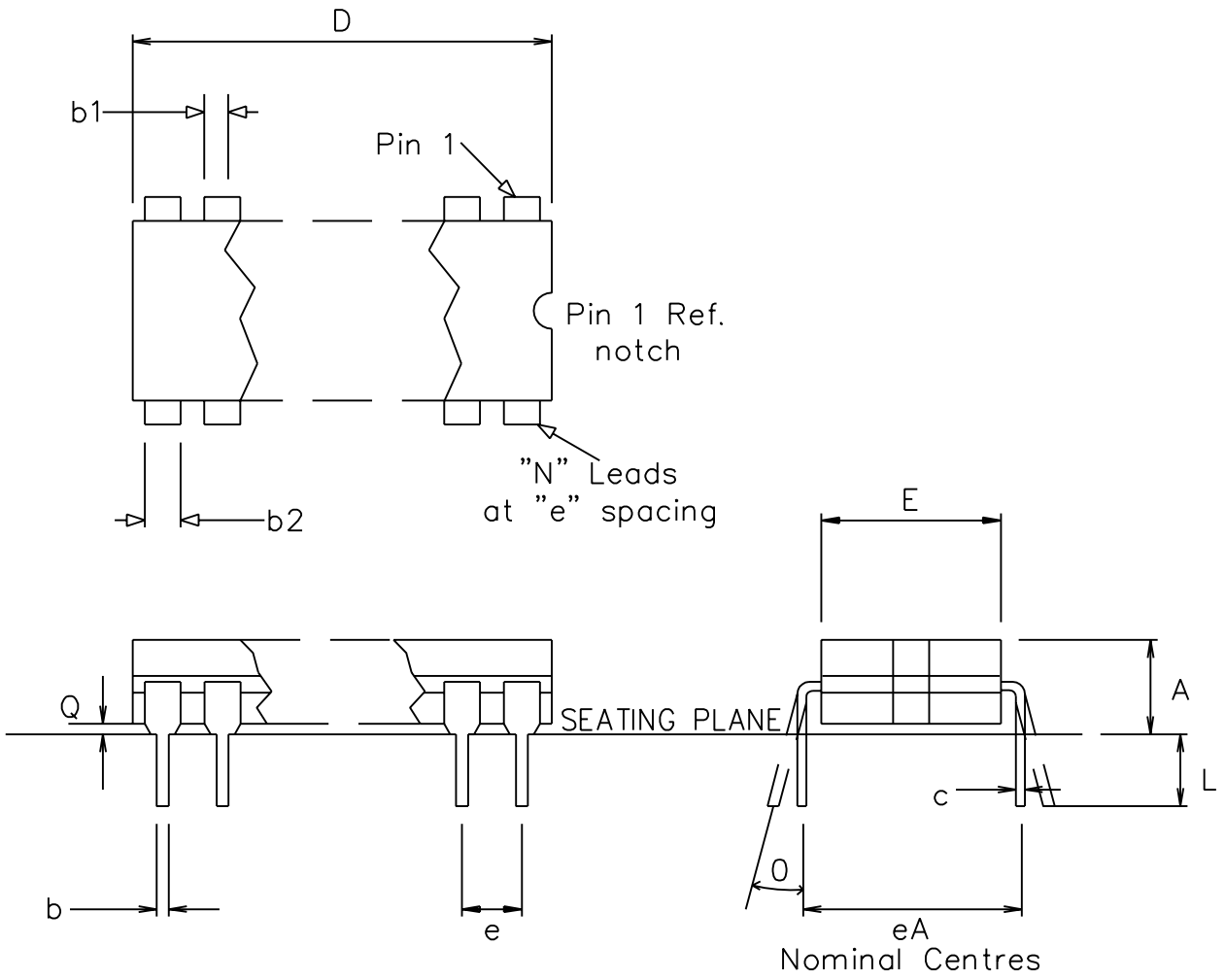
Previous package codes

DC / D

Package Code DK

Package Outline for 28 lead Sidebrazed DIL

GPD00483



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
L	3.18		4.06		0.125		0.160
A			5.59				0.220
Q	0.51				0.020		
E	12.70		15.49		0.500		0.610
eA		15.24				0.600	
c	0.20		0.36		0.008		0.014
D			38.10				1.500
e	2.54 BSC.				0.100 BSC.		
b1	1.14		1.65		0.045		0.065
b	0.36		0.58		0.014		0.023
b2	0.73		1.12		0.029		0.044
0			15°				15°
	Pin features						
N	28						
ND	14						
NE	0						
NOTE	RECTANGULAR						

This drawing supersedes 418/ED/39501/009 (Swindon)

ISSUE	1	2		
ACN	201736	212462		
DATE	20Nov96	27Mar02		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

DG / C

Package Code DH

Package Outline for 28 lead DIL (Glass Seal Ceramic)

GPD00281

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www.zarlink.com