

MB81C78A-35/-45

CMOS 64K-BIT HIGH-SPEED SRAM

8K Words x 8 Bits High-Speed CMOS Static Random Access Memory with Automatic Power Down

The Fujitsu MB81C78A is a 8,192 words x 8 bits static random access memory fabricated with a CMOS process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

A separate chip select (CS_1) pin simplifies multipackage systems design by permitting the selection of an individual package when outputs are OR-tied, and then automatically powering down the other deselected packages.

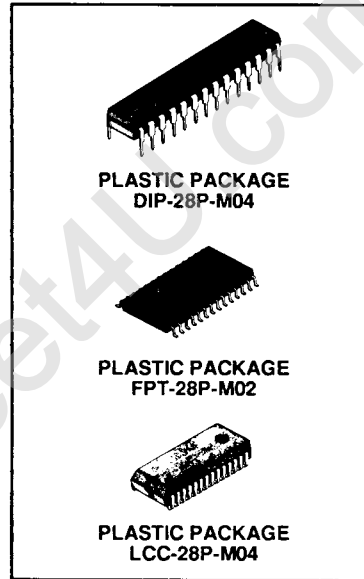
The MB81C78A offers low power dissipation, low cost, and high performance.

- Organization: 8,192 words x 8 bits
- Static operation: no clock or timing strobe required
- Access time: $t_{AA} = t_{ACS1} = 35$ ns max. (MB81C78A-35)
 $t_{AA} = t_{ACS1} = 45$ ns max. (MB81C78A-45)
- Low power consumption: 495 mW max. (Operating)
138 mW max. (Standby, TTL level)
83 mW max. (Standby, CMOS level)
- Single +5 V power supply $\pm 10\%$ tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Chip select for simplified memory expansion, automatic power down
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Package:
 - Skinnier DIP (300 mil) MB81C78A-xxPSK
 - SOP MB81C78A-xxPF
 - SOJ MB81C78A-xxPJ
- Standard 32-pad Ceramic Package:
 - LCC (metal seal) MB81C78A-CV

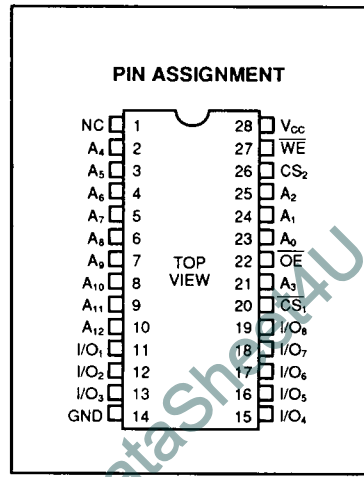
Absolute Maximum Ratings (See Note)

| Rating | Symbol | Value | Unit |
|---------------------------------------------------|------------|--------------|-------------|
| Supply Voltage | V_{CC} | -0.5 to +7.0 | V |
| Input Voltage on any pin with respect to GND | V_{IN} | -3.5 to +7.0 | V |
| Output Voltage on any I/O pin with respect to GND | V_{OUT} | -0.5 to +7.0 | V |
| Output Current | I_{OUT} | ± 20 | mA |
| Power Dissipation | P_D | 1.0 | W |
| Temperature Under Bias | T_{BIAS} | -10 to +85 | $^{\circ}C$ |
| Storage Temperature Range | Ceramic | -65 to +150 | $^{\circ}C$ |
| | Plastic | -40 to +125 | |

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



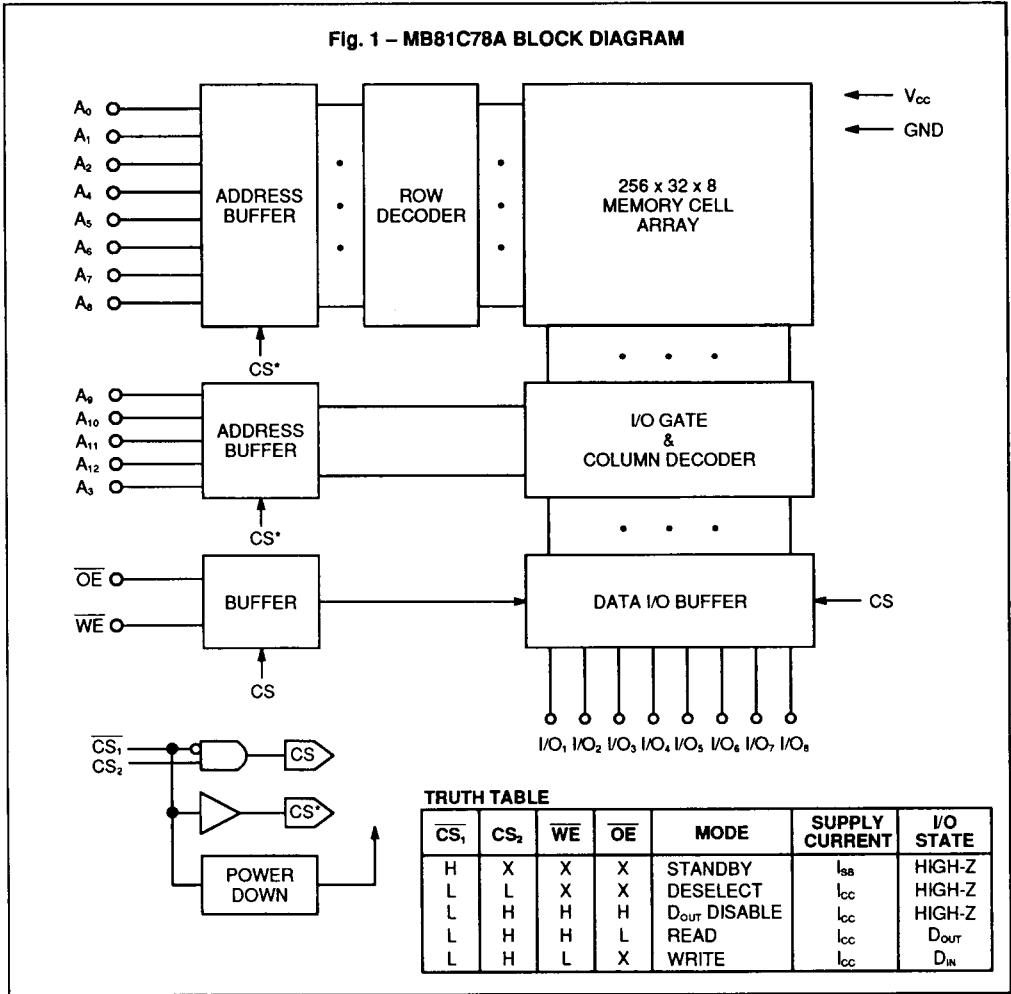
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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C78A-35
MB81C78A-45

Fig. 1 – MB81C78A BLOCK DIAGRAM



CAPACITANCE ($T_A = 25^\circ C, f = 1MHz$)

| Parameter | Symbol | Typ | Max | Unit |
|----------------------------------------------------------------------------------|----------|-----|-----|------|
| Input Capacitance ($V_{IN}=0V$) ($\overline{CS}_1, CS_2, \overline{OE}, WE$) | C_{i1} | | 7 | pF |
| Input Capacitance ($V_{IN}=0V$) (Other Inputs) | C_{i2} | | 6 | pF |
| I/O Capacitance ($V_{I/O}=0V$) | C_{iO} | | 8 | pF |

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------|----------|-----|-----|-----|------|
| Supply Voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| Ambient Temperature | T_A | 0 | | 70 | °C |

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Max | Unit | Test Condition |
|--------------------------|-----------|-------|-----|---------|--------------------------------------------------------------------------------------------------------------------------|
| Input Leakage Current | I_{LI} | -10 | 10 | μ A | $V_{IN}=0V$ to V_{CC} , $V_{CC}=\text{Max.}$ |
| Output Leakage Current | I_{LO} | -10 | 10 | μ A | $\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{OUT}=0V$ to V_{CC} |
| Operating Supply Current | I_{CC} | | 90 | mA | $\overline{CS}_1=V_{IL}$ I/O=Open, Cycle=Min |
| Standby Supply Current | I_{SB1} | | 15 | mA | $V_{CC}=\text{Min to Max.}$ $\overline{CS}_1=V_{CC}-0.2V$ $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$ |
| | I_{SB2} | | 25 | mA | $\overline{CS}_1=V_{IH}$ |
| Input Low Voltage | V_{IL} | -2.0* | 0.8 | V | |
| Input High Voltage | V_{IH} | 2.2 | 6.0 | V | |
| Output Low Voltage | V_{OL} | | 0.4 | V | $I_{OL}=8mA$ |
| Output High Voltage | V_{OH} | 2.4 | | V | $I_{OH}=-4mA$ |
| Peak Power-on Current | I_{PO} | | 50 | mA | $V_{CC}=0V$ to V_{CC} Min. $\overline{CS}_1=\text{Lower of } V_{CC} \text{ or } V_{IH} \text{ Min.}$ |

* -2.0V Min. for pulse width less than 20ns. (V_{IL} Min=-0.5V at DC level)

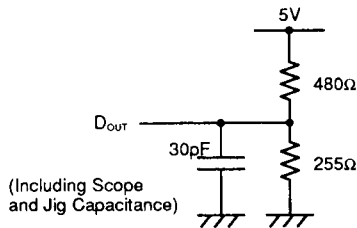
AC TEST CONDITIONS

| | |
|--------------------------------------|--------------------------------------------|
| Input Pulse Levels: | 0.6V to 2.4V |
| Input Pulse Rise And Fall Times: | 5ns (Transient time between 0.8V and 2.2V) |
| Timing Measurement Reference Levels: | Input: 1.5V Output: 1.5V |

Fig. 2

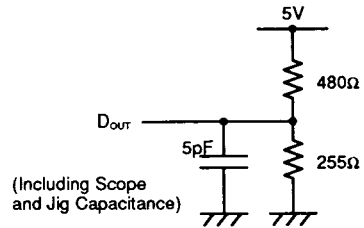
Output Load I.

For all except t_{LZ} , t_{HZ} , t_{WZ} , t_{OW} , t_{OLZ} , and t_{OHZ} .



Output Load II.

For t_{LZ} , t_{HZ} , t_{WZ} , t_{OW} , t_{OLZ} , and t_{OHZ} .



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE*1

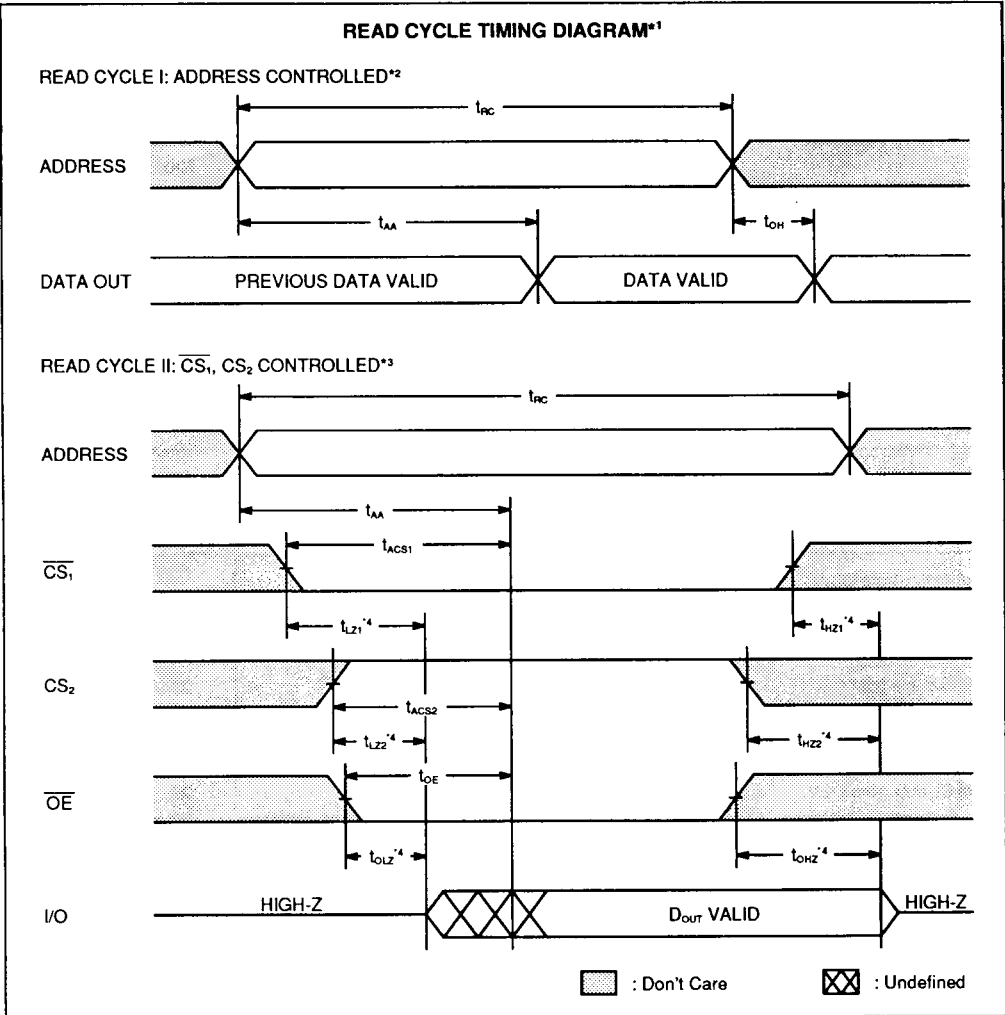
| Parameter | Symbol | MB81C78A-35 | | MB81C78A-45 | | Unit |
|------------------------------------------|------------|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle Time | t_{RC} | 35 | | 45 | | ns |
| Address Access Time*2 | t_{AA} | | 35 | | 45 | ns |
| \overline{CS}_1 Access Time*3 | t_{ACS1} | | 35 | | 45 | ns |
| CS_2 Access Time*3 | t_{ACS2} | | 15 | | 20 | ns |
| Output Hold from Address Change | t_{OH} | 3 | | 3 | | ns |
| \overline{OE} Access Time | t_{OE} | | 15 | | 20 | ns |
| Output Active from \overline{CS}_1 *4 | t_{LZ1} | 5 | | 5 | | ns |
| Output Active from CS_2 *4 | t_{LZ2} | 3 | | 3 | | ns |
| Output Active from \overline{OE} *4 | t_{OLZ} | 3 | | 3 | | ns |
| Output Disable from \overline{CS}_1 *4 | t_{HZ1} | | 20 | | 25 | ns |
| Output Disable from CS_2 *4 | t_{HZ2} | | 20 | | 25 | ns |
| Output Disable from \overline{OE} *4 | t_{OHZ} | | 20 | | 25 | ns |

Note: *1 \overline{WE} is high for Read cycle.

*2 Device is continuously selected, $\overline{CS}_1=V_{IL}$, $CS_2=V_H$, and $\overline{OE}=V_{IL}$.

*3 Address valid prior to or coincident with \overline{CS}_1 transition low, CS_2 transition high.

*4 Transition is specified at the point of $\pm 500mV$ from steady state voltage with specified Load II in Fig. 2.



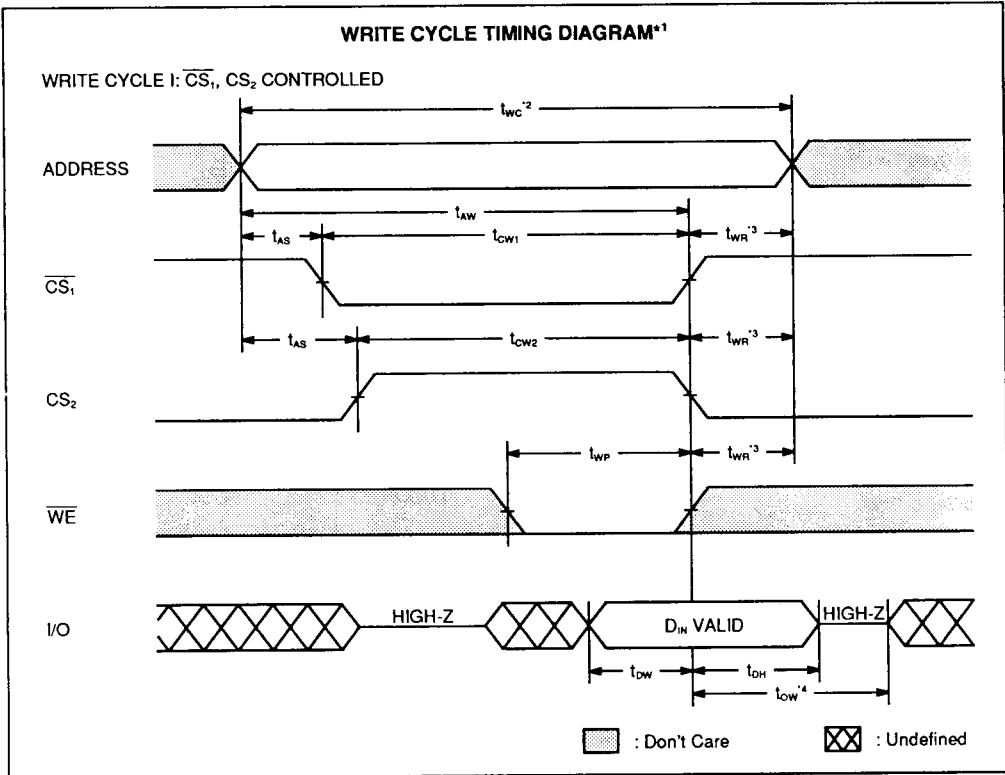
- Note:**
- *1 \overline{WE} is high for Read cycle.
 - *2 Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ and $\overline{OE} = V_{IL}$.
 - *3 Address valid prior to or coincident with \overline{CS}_1 transition low, CS_2 transition high.
 - *4 Transition is specified at the point of $\pm 500mV$ from steady state voltage with specified Load II in Fig. 2.

WRITE CYCLE**

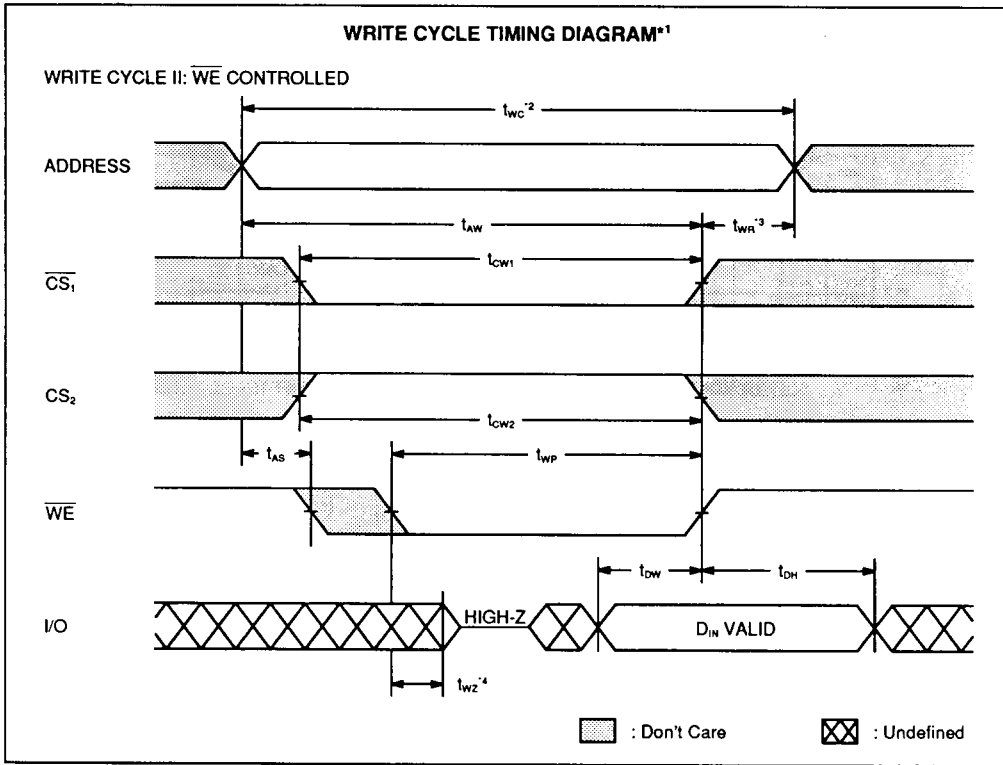
| Parameter | Symbol | MB81C78A-35 | | MB81C78A-45 | | Unit |
|----------------------------------------|-----------|-------------|-----|-------------|-----|------|
| | | Min | Max | Min | Max | |
| Write Cycle Time**2 | t_{wc} | 35 | | 45 | | ns |
| \overline{CS}_1 to End of Write | t_{cw1} | 30 | | 40 | | ns |
| CS_2 to End of Write | t_{cw2} | 20 | | 25 | | ns |
| Address Valid to End of Write | t_{aw} | 30 | | 40 | | ns |
| Address Setup Time | t_{as} | 0 | | 0 | | ns |
| Write Pulse Width | t_{wp} | 20 | | 25 | | ns |
| Data Setup Time | t_{dw} | 17 | | 20 | | ns |
| Write Recovery Time**3 | t_{wr} | 3 | | 3 | | ns |
| Data Hold Time | t_{dh} | 0 | | 0 | | ns |
| Output High-Z from \overline{WE} **4 | t_{wz} | | 15 | | 20 | ns |
| Output Low-Z from \overline{WE} **4 | t_{ow} | 0 | | 0 | | ns |

- Note:**
- *1 If \overline{CS}_1 goes high simultaneously with \overline{WE} high, the output remains in high impedance state.
 - *2 All write cycles are determined from the last address transition to the first address transition of next address.
 - *3 t_{wr} is defined from the end point of Write Mode.
 - *4 Transition is specified at the point of $\pm 500mV$ from steady state voltage with specified Load II in Fig. 2.

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- Note:**
- *1 If \overline{OE} , \overline{CS}_1 , and CS_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - *2 All write cycle are determined from the last address transition to the first address transition of next address.
 - *3 t_{WR} is defined from the end point of WRITE Mode.
 - *4 Transition is specified at the point of $\pm 500mV$ from steady state voltage with specified Load II in Fig. 2.



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- Note:**
- *1 If \overline{OE} , \overline{CS}_1 , and \overline{CS}_2 are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 - *2 All write cycles are determined from the last address transition to the first address transition of next address.
 - *3 t_{WR} is defined from the end point of WRITE Mode.
 - *4 Transition is specified at the point of $\pm 500\text{mV}$ from steady state voltage with specified Load II in Fig. 2.

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Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

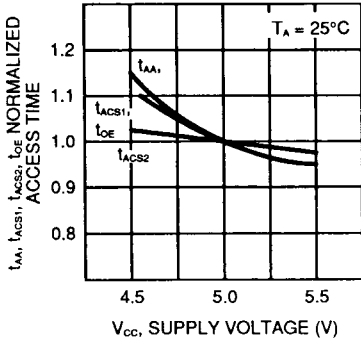


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

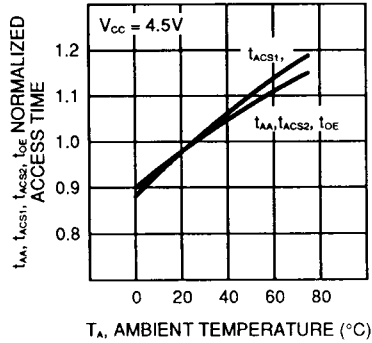


Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

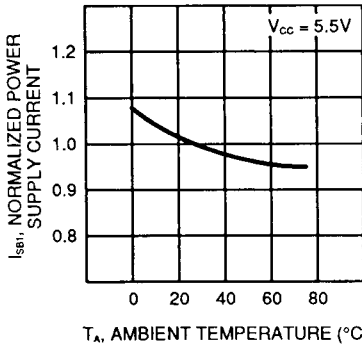


Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

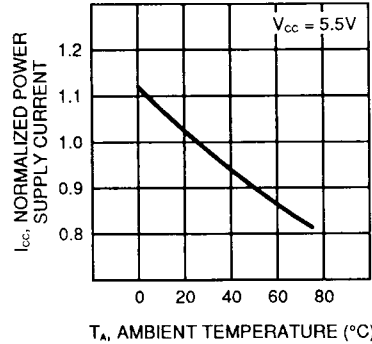


Fig. 7 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

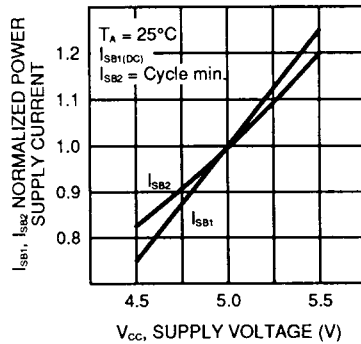


Fig. 8 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

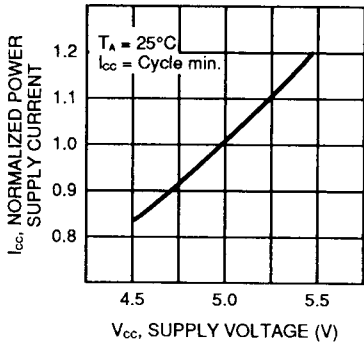


Fig. 9 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

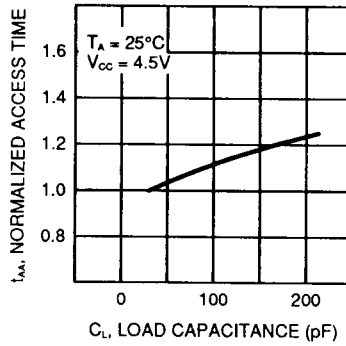


Fig. 10 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

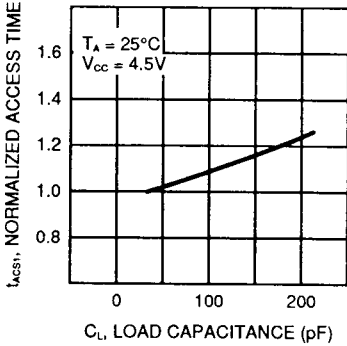


Fig. 11 – NORMALIZED ACCESS TIME vs. LOAD CAPACITANCE

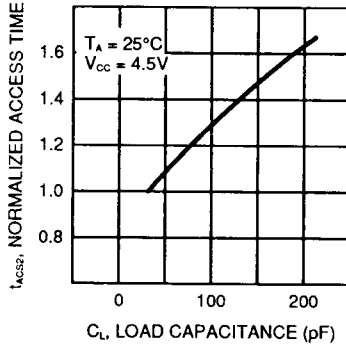
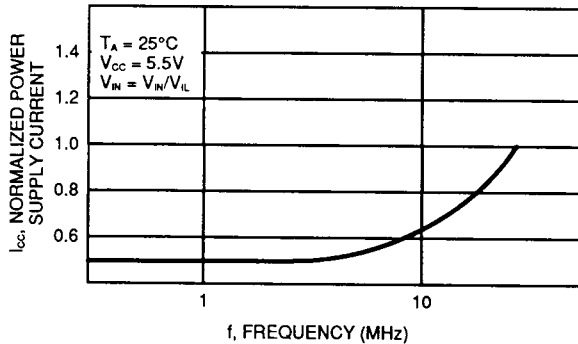


Fig. 12 – NORMALIZED POWER SUPPLY CURRENT vs. FREQUENCY



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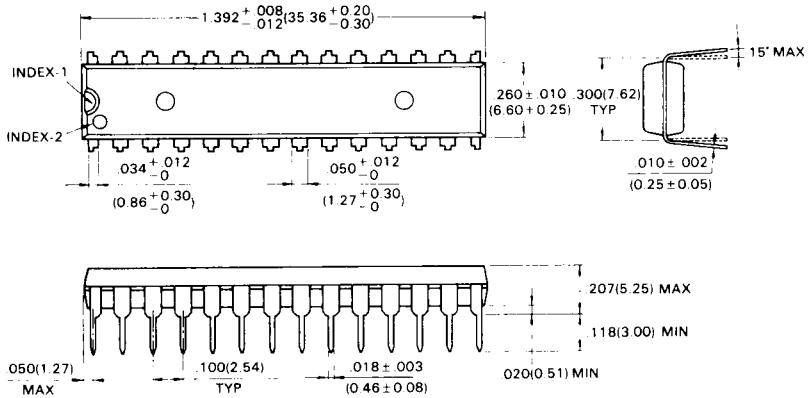
MB81C78A-35
MB81C78A-45

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)



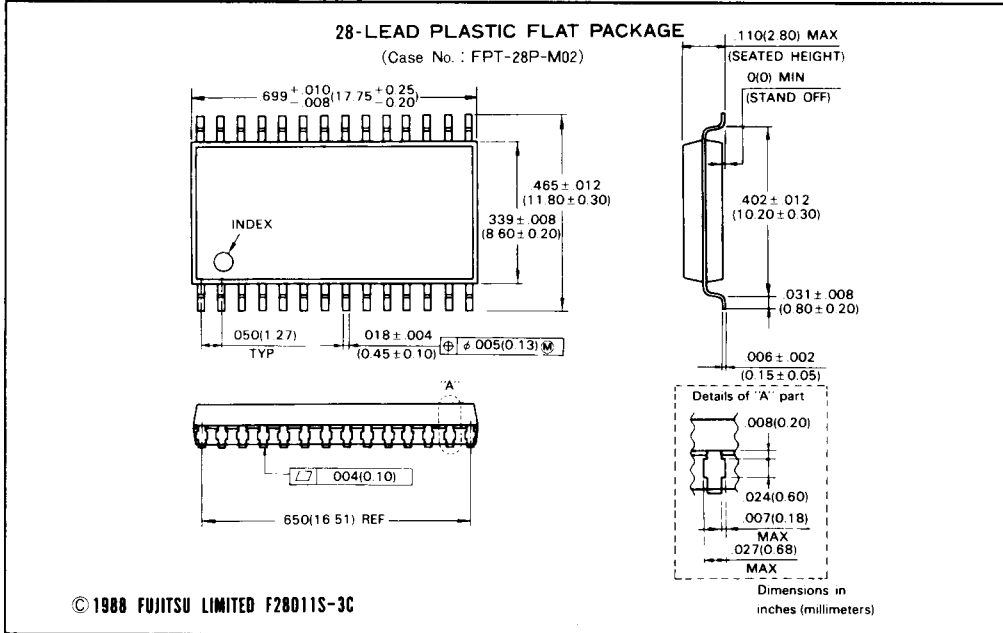
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Dimensions in
inches (millimeters)

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PACKAGE DIMENSIONS

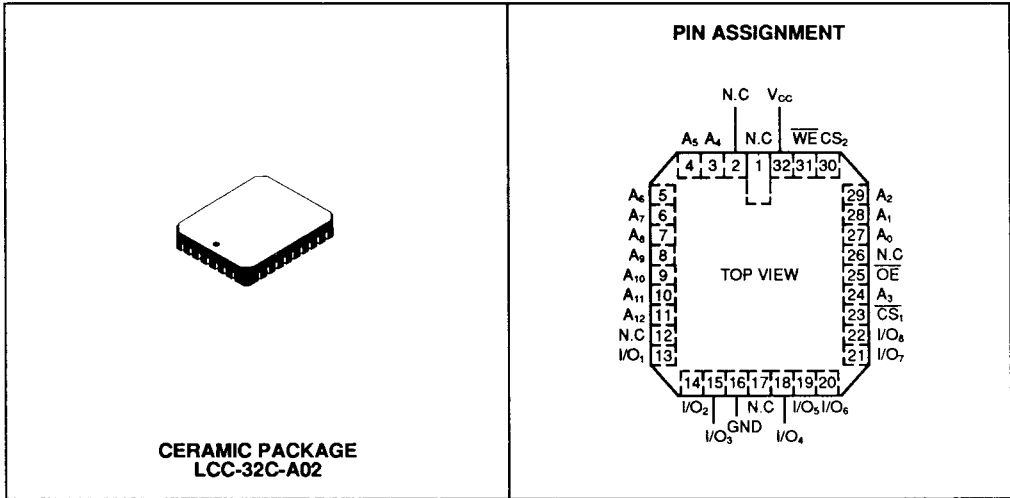
PLASTIC FPT (Suffix: PF)



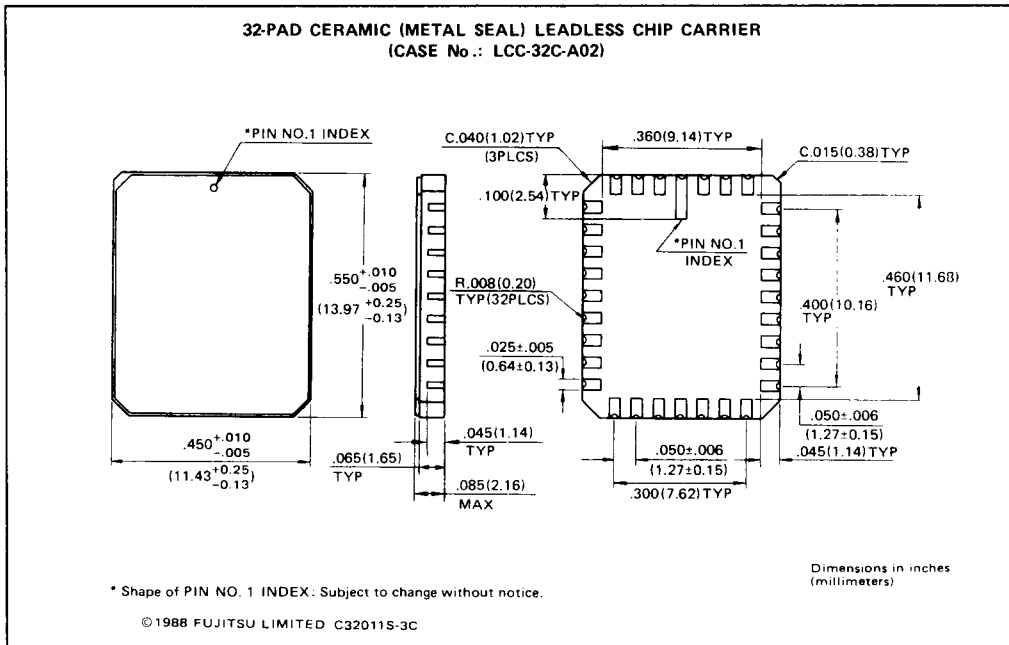
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PACKAGE DIMENSIONS (Cont'd)

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CERAMIC LCC (Suffix: CV)



PACKAGE DIMENSIONS

Plastic (Suffix: PJ)

