SIEMENS

8-Bit Single Chip Microcontroller

SAB 80513/80513-16
SAB 8352-5/8352-5-16

Preliminary Data

SAB 80513/80513-16 Microcontroller with 16 Kbyte ROM (12 MHz/16 MHz)
SAB 8352-5/8352-5-16 Microcontroller with 32 Kbyte ROM (12 MHz/16 MHz)

- 16 K x 8 ROM (SAB 80513)
- 32 K x 8 ROM (SAB 8352-5)
- 256 X 8 RAM
- Four 8-bit I/O ports
- Three 16-bit timer/event counters
- High performance full-duplex serial channel with flexible transmit/receive baud rate capability
- Six interrupt vectors, two priority levels are programmable
- Boolean processor
- Most instructions execute in 1 µs (750 ns)
- 4 µs (3 µs) multiply and divide
- External memory expandable up to 128 Kbytes
- Fully backward compatible to SAB 8051A and SAB 8052A/B
- Package: P-DIP-40 and PL-CC-44
- Two temperature ranges available
  - 0 to 70 °C
  - T3: – 40 to 85 °C

The SAB 80513 and SAB 8352-5 are new members of the Siemens SAB 8051 family of 8-bit microcontrollers. They are fabricated in N-channel, silicon-gate Siemens MYMOS technology.

The SAB 80513 and the SAB 8352-5 are stand-alone, high-performance, single chip microcontrollers based on the SAB 8051 architecture. Both devices maintain all features of the SAB 8051A and SAB 8052A/B (including Timer 2 of the SAB 8052A/B) and thus are fully compatible to both the SAB 8051A and SAB 8052A/B.

In addition, the SAB 80513 contains 16 Kbytes of on-chip ROM; the SAB 8352-5 contains 32 Kbyte of on-chip ROM. This feature makes very cost-effective microcontrollers for applications requiring more ROM space.

Furthermore, both parts contain 256-byte on-chip RAM, four 8-bit ports, a powerful interrupt structure with six vectors and two programmable priority levels, a serial interface as well as on-chip oscillator and clock circuitry.

Both parts are available in a 12 MHz version and in a 16 MHz version which offers an additional performance increase of 33 %.

The SAB 80513 and the SAB 8352-5 are supplied in a 40-pin plastic dual-in-line (P-DIP-40) package or a 44-pin plastic leaded chip carrier (PL-CC-44) package.

The parts are available for standard temperature range (0 to 70 °C) and extended temperature range (T3: – 40 to 85 °C).

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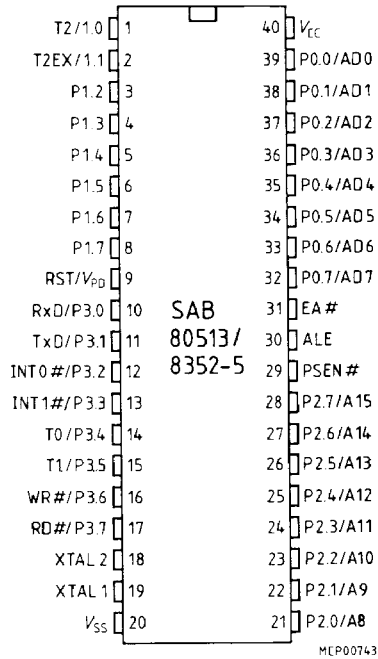
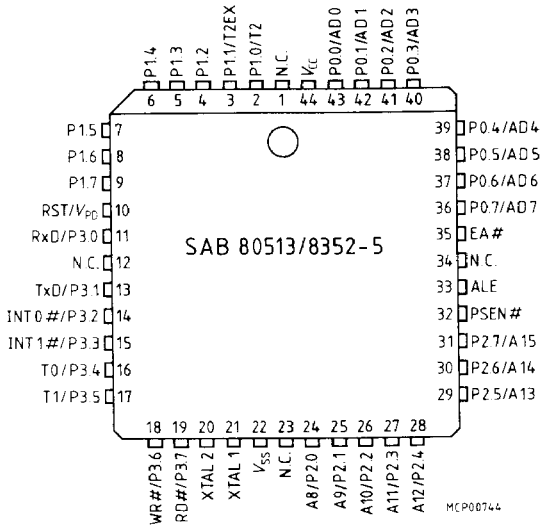
Ordering Information

Type	Ordering code	Package	Function (8-bit single-chip microcontroller)
SAB 80513-P	Q67120-C383	P-DIP-40	with 16-KByte mask-programmable ROM
SAB 80513-N	Q67120-C384	PL-CC-44	with 16-KByte mask-programmable ROM
SAB 80513-16-P	Q67120-C441	P-DIP-40	with 16-KByte mask-programmable ROM, 16 MHz
SAB 80513-16-N	Q67120-C443	PL-CC-44	with 16-KByte mask-programmable ROM, 16 MHz
SAB 80513-16-P-T3	Q67120-C506	P-DIP-40	with 16-KByte mask-programmable ROM, 16 MHz, ext. Temp.
SAB 8352-5-P	Q67120-C526	P-DIP-40	with 32-KByte mask-programmable ROM
SAB 8352-5-N	Q67120-C524	PL-CC-44	with 32-KByte mask-programmable ROM
SAB 8352-5-16-P	Q67120-C529	P-DIP-40	with 32-KByte mask-programmable ROM, 16 MHz
SAB 8352-5-16-N	Q67120-C533	PL-CC-44	with 32-KByte mask-programmable ROM, 16 MHz
SAB 8352-5-16-P-T3	Q67120-C531	P-DIP-40	with 32-KByte mask-programmable ROM, 16 MHz, ext. Temp.

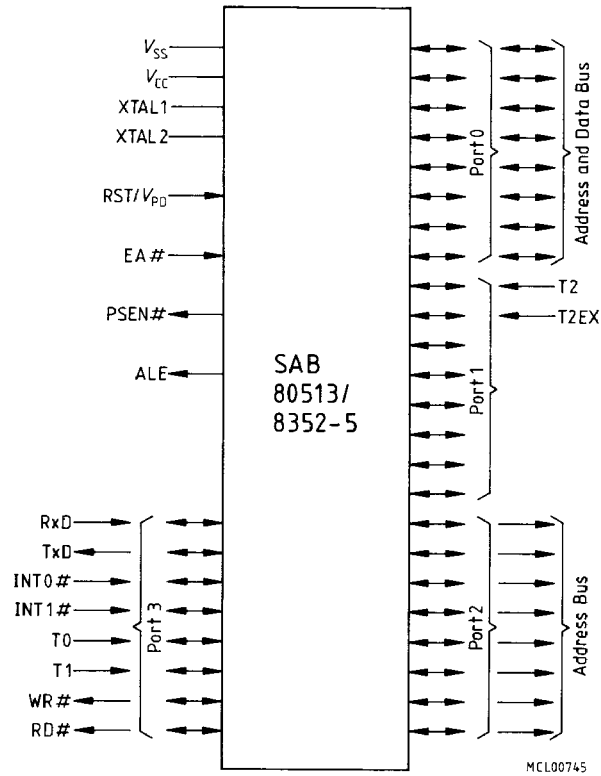
Pin Configuration
P-DIP-40



PL-CC-44



Logic Symbol



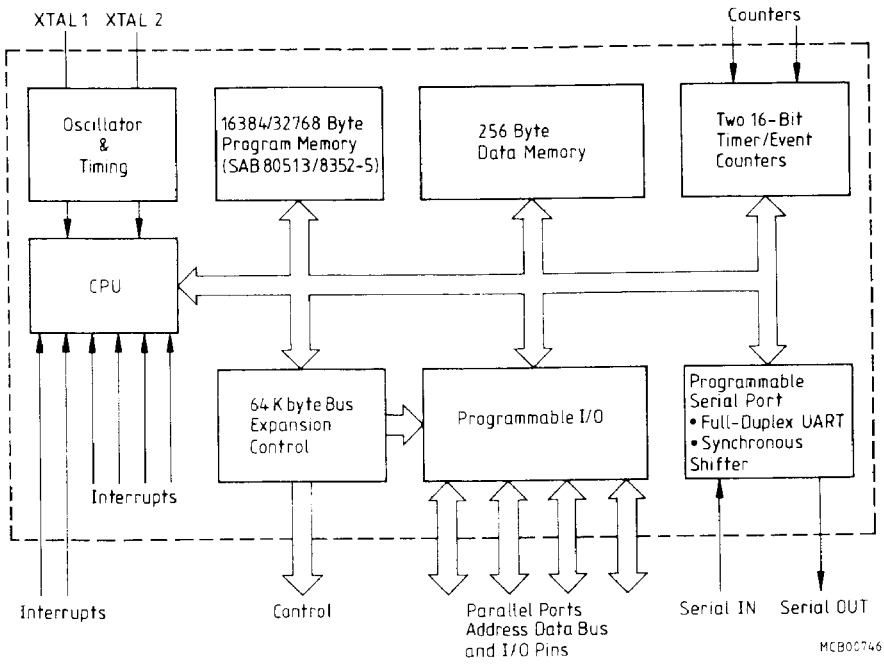
Pin Definitions and Functions

Symbol	Pin Number		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1–8	2–9	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to timer 2, and T2EX, timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/V_{PD}	9	10	I	**RESET** input. A high level on this pin resets the SAB 80513/8352-5. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10–17	11, 13–19	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD# and WR# pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – INT0# (P3.2). Interrupt 0 input or gate control input for counter 0. – INT1# (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – WR# (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – RD# (P3.7). The read control signal enables external data memory to port 0.

Pin Definitions and Functions (cont'd)

Symbol	Pin Number		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
XTAL1 XTAL2	19 18	21 20	–	**XTAL1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL2. **XTAL2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/ source four LS TTL loads.
PSEN#	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
EA#	31	35	I	**External Access** enable. When this pin is held on high level, the SAB 80513 executes instructions from the internal ROM when the PC is less than 4000H. When this pin is held on high level, the SAB 8352-5 executes instructions from the internal ROM when the PC is less than 8000H. When EA# is held on low level, the SAB 80513/8352-5 fetches all instructions from external program memory.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	**Power Supply** during operation and program verification.
V_{SS}	20	22	–	**Ground** (0 V)
NC	–	1,12,23,34	–	**No Connection**

Block Diagram



Instruction Set Summary

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A,Rn	Add register to accumulator	1	1
ADD	A,direct	Add direct byte to accumulator	2	1
ADD	A,@Ri	Add indirect RAM to accumulator	1	1
ADD	A,#data	Add immediate data to accumulator	2	1
ADDC	A,Rn	Add register to accumulator with carry flag	1	1
ADDC	A,direct	Add direct byte to A with carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC	A,#data	Add immediate data to A with carry flag	2	1
SUBB	A,Rn	Subtract register from A with borrow	1	1
SUBB	A,direct	Subtract direct byte from A with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A and B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal adjust accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Logical operations				
ANL	A,Rn	AND register to accumulator	1	1
ANL	A,direct	AND direct byte to accumulator	2	1
ANL	A,@Ri	AND indirect RAM to accumulator	1	1
ANL	A,#data	AND immediate data to accumulator	2	1
ANL	direct,A	AND accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to accumulator	1	1
ORL	A,direct	OR direct byte to accumulator	2	1
ORL	A,@Ri	OR indirect RAM to accumulator	1	1
ORL	A,#data	OR immediate data to accumulator	2	1
ORL	direct,A	OR accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive OR register to accumulator	1	1
XRL	A,direct	Exclusive OR direct byte to accumulator	2	1
XRL	A,@Ri	Exclusive OR indirect RAM to accumulator	1	1
XRL	A,#data	Exclusive OR immediate data to accumulator	2	1
XRL	direct,A	Exclusive OR accumulator to direct byte	2	1
XRL	direct,#data	Exclusive OR immediate data to direct byte	3	2
CLR	A	Clear accumulator	1	1
CPL	A	Complement accumulator	1	1
RL	A	Rotate accumulator left	1	1
RLC	A	Rotate A left through carry flag	1	1
RR	A	Rotate accumulator right	1	1
RRC	A	Rotate A right through carry flag	1	1
SWAP	A	Swap nibbles within the accumulator	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Data transfer				
MOV	A,Rn	Move register to accumulator	1	1
MOV	A,direct*)	Move direct byte to accumulator	2	1
MOV	A,@Ri	Move indirect RAM to accumulator	1	1
MOV	A,#data	Move immediate data to accumulator	2	1
MOV	Rn,A	Move accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct, A	Move accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct byte	3	2
MOV	direct,@R	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move code byte relative to DPTR to accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr.) to accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr.) to accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr.)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr.)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with accumulator	1	1
XCH	A,direct	Exchange direct byte with accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A	1	1

*) MOV A, ACC is not a valid instruction

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr.)	2	2
JMP	@A + DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if accumulator is zero	2	2
JNZ	rel	Jump if accumulator is not zero	2	2
JC	rel	Jump if carry flag is set	2	2
JNC	rel	Jump if carry flag is not set	2	2
JB	bit,rel	Jump if direct bit is set	3	2
JNB	bit,rel	Jump if direct bit is not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct byte to A and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to A and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp. immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Instruction Set Summary (cont'd)

Mnemonic		Description	Byte	Cycle
Boolean variable manipulation				
CLR	C	Clear carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to carry flag	2	2
ANL	C,/bit	AND complement of direct bit to carry	2	2
ORL	C,bit	OR direct bit to carry flag	2	2
ORL	C,/bit	OR complement of direct bit to carry	2	2
MOV	C,bit	Move direct bit to carry flag	2	1
MOV	bit,C	Move carry flag to direct bit	2	2

Notes on data addressing modes:

Rn – Working register R0 – R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal or external RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 and 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes

addr 16 – Destination address for LCALL and LJMP may be anywhere within the 64 Kbyte program memory address space.
addr 11 – Destination address for ACALL and AJMP will be within the same 2 Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is + 127/– 128 bytes relative to first byte of the following instruction.

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Instruction Op Codes in Hexadecimal Order

Hex-code	Number of bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr, code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr, code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A, *#data*
25	2	ADD	A, *data addr*
26	1	ADD	A, @R0
27	1	ADD	A, @R1
28	1	ADD	A, R0
29	1	ADD	A, R1
2A	1	ADD	A, R2
2B	1	ADD	A, R3
2C	1	ADD	A, R4
2D	1	ADD	A, R5
2E	1	ADD	A, R6
2F	1	ADD	A, R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A, *#data*
35	2	ADDC	A, *data addr*
36	1	ADDC	A, @R0
37	1	ADDC	A, @R1
38	1	ADDC	A, R0
39	1	ADDC	A, R1
3A	1	ADDC	A, R2
3B	1	ADDC	A, R3
3C	1	ADDC	A, R4
3D	1	ADDC	A, R5
3E	1	ADDC	A, R6
3F	1	ADDC	A, R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr, A*
43	3	ORL	*data addr, #data*
44	2	ORL	A, *#data*
45	2	ORL	A, *data addr*
46	1	ORL	A, @R0
47	1	ORL	A, @R1
48	1	ORL	A, R0
49	1	ORL	A, R1

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
4A	1	ORL	A, R2
4B	1	ORL	A, R3
4C	1	ORL	A, R4
4D	1	ORL	A, R5
4E	1	ORL	A, R6
4F	1	ORL	A, R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr, A*
53	3	ANL	*data addr, #data*
54	2	ANL	A, *#data*
55	2	ANL	A, *data addr*
56	1	ANL	A, @R0
57	1	ANL	A, @R1
58	1	ANL	A, R0
59	1	ANL	A, R1
5A	1	ANL	A, R2
5B	1	ANL	A, R3
5C	1	ANL	A, R4
5D	1	ANL	A, R5
5E	1	ANL	A, R6
5F	1	ANL	A, R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr, A*
63	3	XRL	*data addr, #data*
64	2	XRL	A, *#data*
65	2	XRL	A, *data addr*
66	1	XRL	A, @R0
67	1	XRL	A, @R1
68	1	XRL	A, R0
69	1	XRL	A, R1
6A	1	XRL	A, R2
6B	1	XRL	A, R3
6C	1	XRL	A, R4
6D	1	XRL	A, R5
6E	1	XRL	A, R6
6F	1	XRL	A, R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C, *bit addr*
73	1	JMP	@A + DPTR
74	2	MOV	A, *#data*
75	3	MOV	*data addr, #data*
76	2	MOV	@R0, *#data*
77	2	MOV	@R1, *#data*
78	2	MOV	R0, *#data*
79	2	MOV	R1, *#data*
7A	2	MOV	R2, *#data*
7B	2	MOV	R3, *#data*
7C	2	MOV	R4, *#data*
7D	2	MOV	R5, *#data*
7E	2	MOV	R6, *#data*
7F	2	MOV	R7, *#data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C, *bit addr*
83	1	MOVC	A, @A + PC
84	1	DIV	AB
85	3	MOV	*data addr, data addr*
86	2	MOV	*data addr*, @R0
87	2	MOV	*data addr*, @R1
88	2	MOV	*data addr*, R0
89	2	MOV	*data addr*, R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*, R4
8D	2	MOV	*data addr*, R5
8E	2	MOV	*data addr*, R6
8F	2	MOV	*data addr*, R7
90	3	MOV	DPTR, *#data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*, C
93	1	MOVC	A, @A + DPTR

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
94	2	SUBB	A, *#data*
95	2	SUBB	A, *data addr*
96	1	SUBB	A, @R0
97	1	SUBB	A, @R1
98	1	SUBB	A, R0
99	1	SUBB	A, R1
9A	1	SUBB	A, R2
9B	1	SUBB	A, R3
9C	1	SUBB	A, R4
9D	1	SUBB	A, R5
9E	1	SUBB	A, R6
9F	1	SUBB	A, R7
A0	2	ORL	C, */bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C, *bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0, *data addr*
A7	2	MOV	@R1, *data addr*
A8	2	MOV	R0, *data addr*
A9	2	MOV	R1, *data addr*
AA	2	MOV	R2, *data addr*
AB	2	MOV	R3, *data addr*
AC	2	MOV	R4, *data addr*
AD	2	MOV	R5, *data addr*
AE	2	MOV	R6, *data addr*
AF	2	MOV	R7, *data addr*
B0	2	ANL	C, */bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,*#data, code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0, *#data, code addr*
B7	3	CJNE	@R1, *#data, code addr*
B8	3	CJNE	R0, *#data, code addr*
B9	3	CJNE	R1, *#data, code addr*
BA	3	CJNE	R2, *#data, code addr*
BB	3	CJNE	R3, *#data, code addr*
BC	3	CJNE	R4, *#data, code addr*
BD	3	CJNE	R5, *#data, code addr*
BE	3	CJNE	R6, *#data, code addr*
BF	3	CJNE	R7, *#data, code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A, *data addr*
C6	1	XCH	A, @R0
C7	1	XCH	A, @R1
C8	1	XCH	A, R0
C9	1	XCH	A, R1
CA	1	XCH	A, R2
CB	1	XCH	A, R3
CC	1	XCH	A, R4
CD	1	XCH	A, R5
CE	1	XCH	A, R6
CF	1	XCH	A, R7
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr, code addr*
D6	1	XCHD	A, @R0
D7	1	XCHD	A, @R1
D8	2	DJNZ	R0, *code addr*
D9	2	DJNZ	R1, *code addr*
DA	2	DJNZ	R2, *code addr*
DB	2	DJNZ	R3, *code addr*
DC	2	DJNZ	R4, *code addr*
DD	2	DJNZ	R5, *code addr*

Instruction Op Codes in Hexadecimal Order (cont'd)

Hex-code	Number of bytes	Mnemonic	Operands
DE	2	DJNZ	R6, *code addr*
DF	2	DJNZ	R7, *code addr*
E0	1	MOVX	A, @DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A, @R0
E3	1	MOVX	A, @R1
E4	1	CLR	A
E5	2	MOV	A, *data addr* *)
E6	1	MOV	A, @R0
E7	1	MOV	A, @R1
E8	1	MOV	A, R0
E9	1	MOV	A, R1
EA	1	MOV	A, R2
EB	1	MOV	A, R3
EC	1	MOV	A, R4
ED	1	MOV	A, R5
EE	1	MOV	A, R6
EF	1	MOV	A, R7
F0	1	MOVX	@DPTR, A
F1	2	ACALL	code addr
F2	1	MOVX	@R0, A
F3	1	MOVX	@R1, A
F4	1	CPL	A
F5	2	MOV	*data addr*, A
F6	1	MOV	@R0, A
F7	1	MOV	@R1, A
F8	1	MOV	R0, A
F9	1	MOV	R1, A
FA	1	MOV	R2, A
FB	1	MOV	R3, A
FC	1	MOV	R4, A
FD	1	MOV	R5, A
FE	1	MOV	R6, A
FF	1	MOV	R7, A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings

Ambient temperature under bias	0 to + 70 °C
	– 40 to + 85 °C (for - T3)
Storage temperature	– 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS})	– 0.5 to + 7 V
Power dissipation	2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, PSEN#	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, PSEN#	2.4	–	V	I_{OH} = – 400 µA
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL2	–	– 3.2	mA	XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} – 1.5V
I_{LI}	Input leakage current to port 0, EA#	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current			mA	all outputs disconnected
	SAB 80513	–	175		
	SAB 80513-16	–	175		
	SAB 80513-16-T3	–	200		
	SAB 8352-5	–	200		
	SAB 8352-5-16	–	TBD		
	SAB 8352-5-16-T3	–	TBD		
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

AC Characteristics for SAB 80513/8352-5

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 to 12 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	127	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	53	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	48	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to PSEN#	58	–	t_{CLCL} – 25	–	ns
t_{PLPH}	PSEN# pulse width	215	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	150	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ} 1)	Input instruction float after PSEN#	–	63	–	t_{CLCL} – 20	ns
t_{PXAV} 1)	Address after PSEN#	75	–	t_{CLCL} – 8	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	5 t_{CLCL} – 115	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

External Data Memory Characteristics

t_{RLRH}	RD# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	WR# pulse width	400	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	132	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	RD# to valid data in	–	252	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	550	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	598	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to WR# or RD#	200	300	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to WR# or RD#	203	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	WR# or RD# high to ALE high	43	123	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to WR# transition	33	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before WR#	433	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after WR#	33	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

1) Interfacing the SAB 80513/8352-5 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 to 12 MHz		
		min.	max.	

External Clock Drive XTAL2

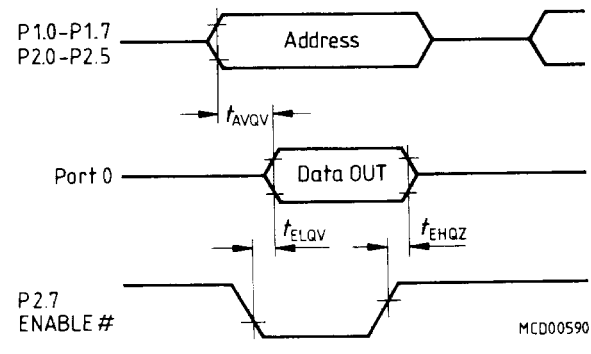
t_{CLCL}	Oscillator period	83.3	833.3	ns
t_{CHCX}	High time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	20	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCH}	Rise time	–	20	ns
t_{CHCL}	Fall time	–	20	ns

ROM Verification Characteristics for SAB 80513/80513-16

$T_A = 25\ °C \pm 5\ °C$; $V_{CC} = 5\ V \pm 10\ \%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48t_{CLCL}$	ns
t_{ELQV}	ENABLE# to valid data	–	$48t_{CLCL}$	ns
t_{EHQZ}	Data float after ENABLE#	0	$48t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

ROM Verification



Address:	P1.0 – P1.7	= A0 – A7	Inputs:	P2.6, PSEN#	= V_{SS}
	P2.0 – P2.5	= A8 – A13		ALE, EA#	= V_{IH}
Data:	Port 0	= D0 – D7		RST/V_{PD}	= V_{IH1}

AC Characteristics for SAB 80513-16/8352-5-16

T_A = 0 to 70 °C; T_A = – 40 to + 85 °C for T3; V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN# outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 to 16 MHz		
		min.	max.	min.	max.	

Program Memory Characteristics

t_{LHLL}	ALE pulse width	85	–	2 t_{CLCL} – 40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL} – 30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL} – 35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	4 t_{CLCL} – 100	ns
t_{LLPL}	ALE to PSEN#	38	–	t_{CLCL} – 25	–	ns
t_{PLPH}	PSEN# pulse width	153	–	3 t_{CLCL} – 35	–	ns
t_{PLIV}	PSEN# to valid instruction in	–	88	–	3 t_{CLCL} – 100	ns
t_{PXIX}	Input instruction hold after PSEN#	0	–	0	–	ns
t_{PXIZ} 1)	Input instruction float after PSEN#	–	48	–	t_{CLCL} – 15	ns
t_{PXAV} 1)	Address after PSEN#	60	–	t_{CLCL} – 3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	5 t_{CLCL} – 90	ns
t_{AZPL}	Address float to PSEN#	0	–	0	–	ns

External Data Memory Characteristics

t_{RLRH}	RD# pulse width	275	–	6 t_{CLCL} – 100	–	ns
t_{WLWH}	WR# pulse width	275	–	6 t_{CLCL} – 100	–	ns
t_{LLAX2}	Address hold after ALE	90	–	2 t_{CLCL} – 35	–	ns
t_{RLDV}	RD# to valid data in	–	148	–	5 t_{CLCL} – 165	ns
t_{RHDX}	Data hold after RD#	0	–	0	–	ns
t_{RHDZ}	Data float after RD#	–	55	–	2 t_{CLCL} – 70	ns
t_{LLDV}	ALE to valid data in	–	350	–	8 t_{CLCL} – 150	ns
t_{AVDV}	Address to valid data in	–	398	–	9 t_{CLCL} – 165	ns
t_{LLWL}	ALE to WR# or RD#	138	238	3 t_{CLCL} – 50	3 t_{CLCL} + 50	ns
t_{AVWL}	Address to WR# or RD#	120	–	4 t_{CLCL} – 130	–	ns
t_{WHLH}	WR# or RD# high to ALE high	23	103	t_{CLCL} – 40	t_{CLCL} + 40	ns
t_{QVWX}	Data valid to WR# transition	13	–	t_{CLCL} – 50	–	ns
t_{QVWH}	Data setup before WR#	288	–	7 t_{CLCL} – 150	–	ns
t_{WHQX}	Data hold after WR#	13	–	t_{CLCL} – 50	–	ns
t_{RLAZ}	Address float after RD#	–	0	–	0	ns

1) Interfacing the SAB 80513-16/8352-5-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit
		Variable clock Freq. = 1.2 to 16 MHz		
		min.	max.	

External Clock Drive XTAL2

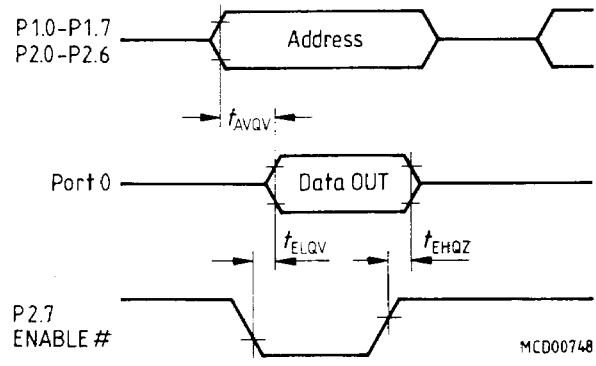
t_{CLCL}	Oscillator period	62.5	833.3	ns
t_{CHCX}	High time	15	$t_{CLCL} - t_{CLCX}$	ns
t_{CLCX}	Low time	15	$t_{CLCL} - t_{CHCX}$	ns
t_{CLCH}	Rise time	–	15	ns
t_{CHCL}	Fall time	–	15	ns

ROM Verification Characteristics for SAB 80513/80513-16

$T_A = 25\ °C \pm 5\ °C$; $V_{CC} = 5\ V \pm 10\ \%$; $V_{SS} = 0\ V$

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	$48t_{CLCL}$	ns
t_{ELQV}	ENABLE# to valid data	–	$48t_{CLCL}$	ns
t_{EHQZ}	Data float after ENABLE#	0	$48t_{CLCL}$	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

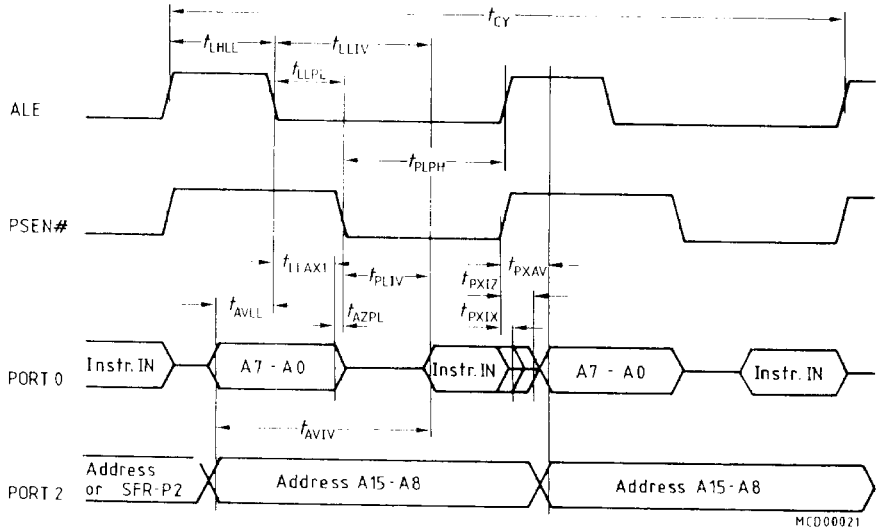
ROM Verification



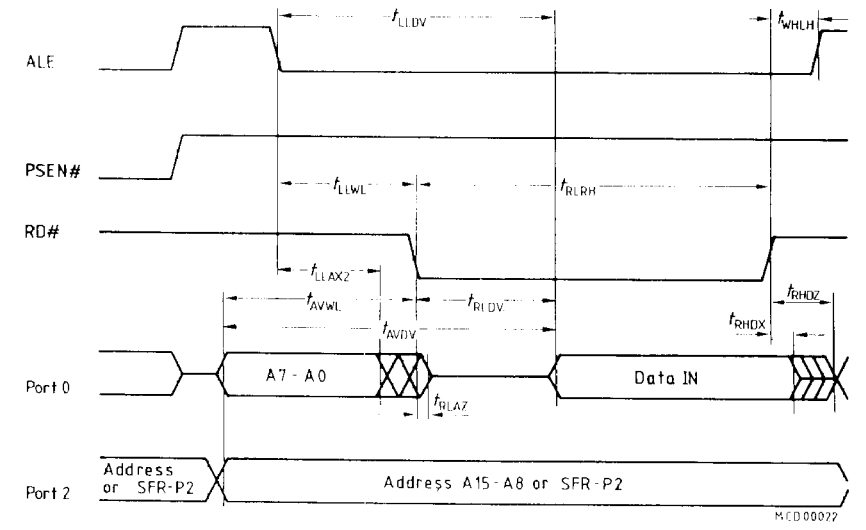
Address:	P1.0 – P1.7	= A0 – A7	Inputs:	P2.6, PSEN#	= V_{SS}
	P2.0 – P2.6	= A8 – A14		ALE, EA#	= V_{IH}
Data:	Port 0	= D0 – D7		RST/V_{PD}	= V_{IH1}

Waveforms

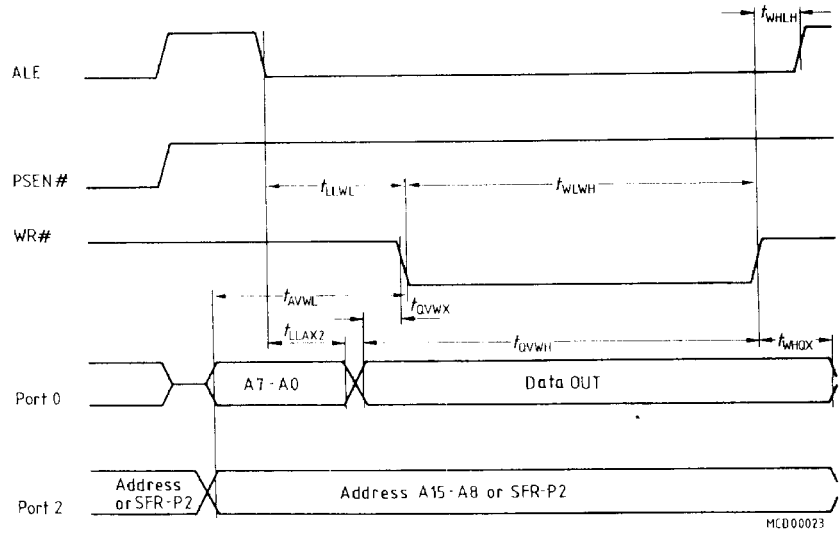
Program Memory Read Cycle



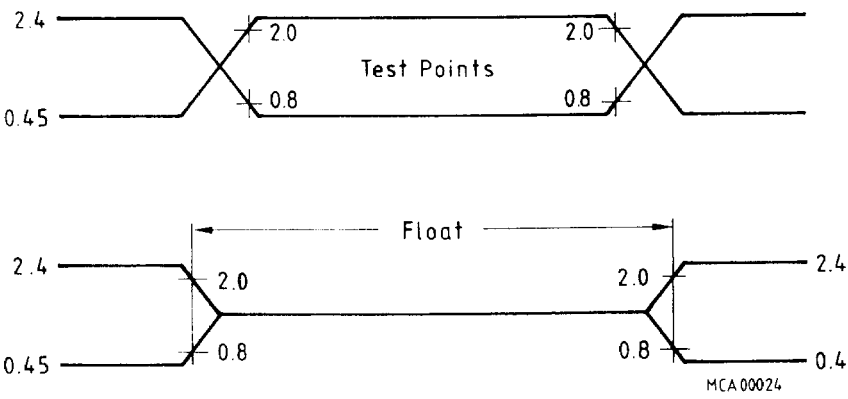
Data Memory Read Cycle



Data Memory Write Cycle

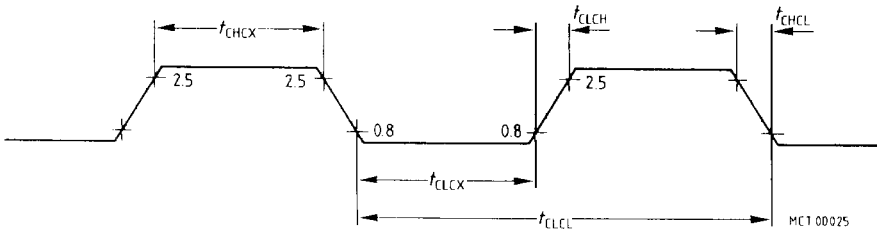


AC Testing Input, Output, Float Waveforms

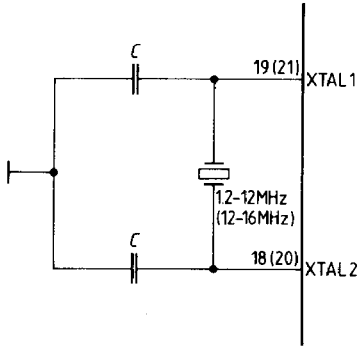


AC testing inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at voltage test levels.

External Clock Cycle



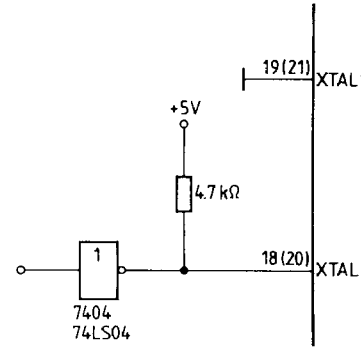
Recommended Oscillator Circuits



$C = 30\,pF \pm 10\,pF$

Crystal Oscillator Mode

Pin numbers in (...) are for PL-CC-44 package



Driving from External Source MCS00747