NEC Electronics Inc.

μPD75P54/P64
4-Bit, Single-Chip, One-Time Programmable (OTP) CMOS Microcomputers With Serial I/O

T-49-19-59

Description

The μPD75P54 and μPD75P64 are 1024 x 8-bit on-chip, one-time programmable (OTP) ROM versions of the mask ROMs, μPD7554 and μPD7564. They have the same functions as, and are pin-compatible with, their mask ROMs. Because of their programming capabilities, the μPD75P54/P64 are suitable for evaluation and small lot production for system development. Their unique features will be described in this data sheet. For information about the base part μPD7554/64, please refer to its data sheet.

Features

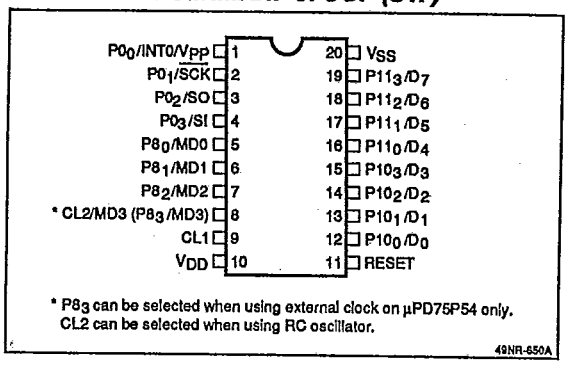
- 47 instructions (subset of μPD7500 set B)
- Instruction cycle:
  - — External clock (μPD75P54): 2.86 μs/700 kHz, 5 V
  - — RC oscillator (μPD75P54): 4 μs/500 kHz, 5 V
  - — Ceramic oscillator (μPD75P64): 2.86 μs/700 kHz, 5 V
- Program memory (ROM) of 1024 x 8 bits
- Data memory (RAM) of 64 x 4 bits
- 8-bit timer/event counter
- 8-bit serial interface
- I/O lines: 16-μPD75P54; 15-μPD75P64
- Data memory retention at low supply voltage
- CMOS technology
- Low-power consumption
- Single power supply:
  - — 4.5 to 6.0 V normal operation
  - — 6.0 V OTP
- STOP, HALT standby functions
- 20-pin plastic shrink DIP or SOP (OTP)

Ordering Information

Part Number	Package Type
μPD75P54CS	20-pin plastic shrink DIP (OTP)
μPD75P64CS	
μPD75P54G	20-pin plastic SOP (OTP)
μPD75P64G	

Pin Configuration

20-Pin Plastic Shrink DIP or SOP (OTP)



* P83 can be selected when using external clock on μPD75P54 only. CL2 can be selected when using RC oscillator.

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Pin Identification

Symbol	Function
$P0_0$/INT0/V_{PP}	4-bit input port 0/count clock input/serial interface. Programming voltage supply pin for program memory write/verify.
$P0_1$/$\overline{SCK}$	
$P0_2$/SO	
$P0_3$/SI	
$P8_0$-$P8_2$/MD0-MD2 CL2/MD3 ($P8_3$/MD3)	4-bit output port 8/OTP operation mode. Connection for ceramic resonator or RC (No $P8_3$ on μPD75P64) (Note 1)
CL1	Connection for ceramic resonator or RC
V_{DD}	4.5 to 6.0 V power supply, normal operation. 6.0 V for OTP.
RESET	Reset input pin
$P10_1$-$P10_3$/D_0-D_3	4-bit I/O port 10 and D_0-D_3 during programming write/verify.
$P11_0$-$P11_3$/D_4-D_7	4-bit I/O port 11 and D_4-D_7 during programming write/verify.
V_{SS}	Ground

Note:

(1) MD0-MD3 are used as mode select pins during programming.

PIN FUNCTIONS

$P0_0$/INT0/V_{PP}, $P0_1$/$\overline{SCK}$ $P0_2$/SO, $P0_3$/SI (Port 0/Count Clock Input/Programming/ Serial Interface)

4-bit input port 0/count clock input/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface, under control of the serial mode select register. The serial input SI (active high), serial output SO (active low), as the serial clock $\overline{SCK}$ (active low—synchronizes data transfer) comprise the 8-bit serial I/O interface. If $P0_0$/INT0 is unused, connect it to ground. If any of $P0_1$-$P0_3$ are unused, connect them to ground. The port is in the input state at reset.

$P8_0$-$P8_2$/MD0-MD2, $P8_3$/MD3 (CL2/MD3) (Port 8/Clock Input/Mode Selection for OTP)

4-bit output port 8. This port can sink 15 mA and interface 12 V. $P8_3$ is a output port on the μPD75P64. On the μPD75P54, CL2 is one of the pins to which a resistor for RC oscillation is connected. On the μPD75P64, CL2 is one of the pins to which a ceramic resonator is connected. If any of $P8_0$-$P8_2$ pins are unused, leave them open. The port is in the high impedance state at reset. MD0-MD3 are used for OTP program memory write and read mode selection. There is no $P8_3$ on the μPD75P64.

CL1 (Clock Input 1)

On the μPD75P54, CL1 is one of the two pins to which a resistor for RC oscillation is connected. On the μPD75P64, CL1 is one of the two pins to which a ceramic resonator is connected.

V_{DD} (Power Supply)

Positive power supply. 4.5 to 6.0 V for normal operation. 6.0 V for program memory write/verify.

RESET (Reset)

System reset input pin (active high). This pin is not internally connected to a pull-down resistor.

$P10_0$-$P10_3$/D_0-D_3 (Port 10/Data I/O)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset. D_0-D_3 are 4-bit I/O pins for program memory write/verify.

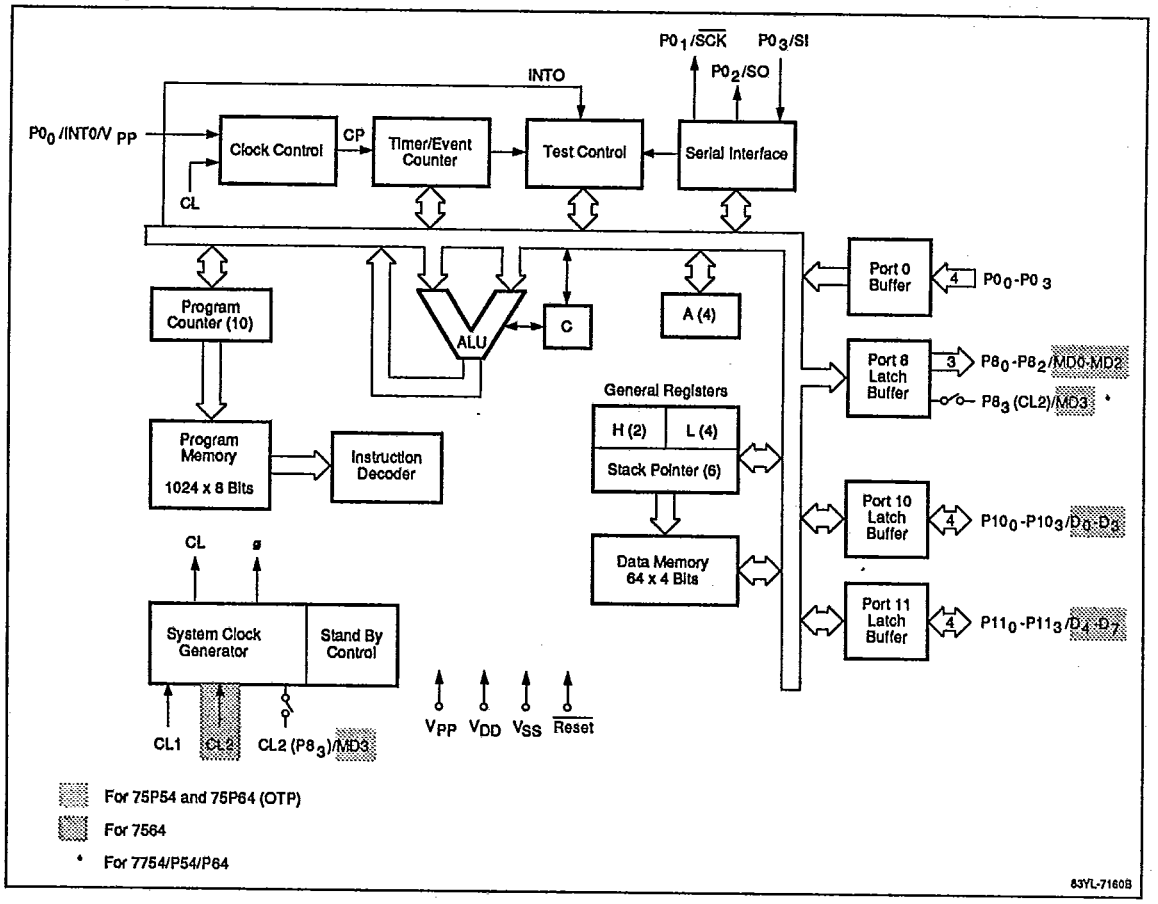
$P11_0$-$P11_3$/D_4-D_7 (Port 11/Data I/O)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset. D_4-D_7 are 4-bit I/O pins for program memory write/verify.

V_{SS} (Ground)

Ground.

Block Diagram



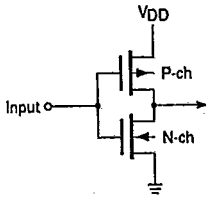
FUNCTIONAL DESCRIPTION

I/O Ports

Figure 1 shows the internal circuits at I/O ports 0, 8, 10, and 11.

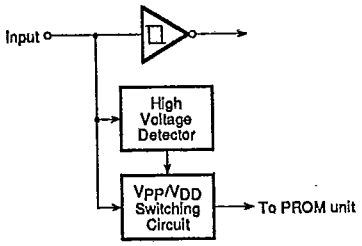
Figure 1. Interface at I/O Ports

Type A
(for Type W)



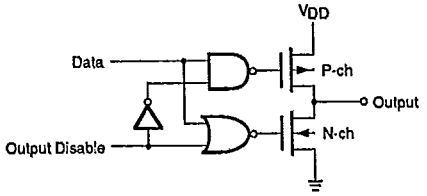
CMOS standard input buffer

Type B-B



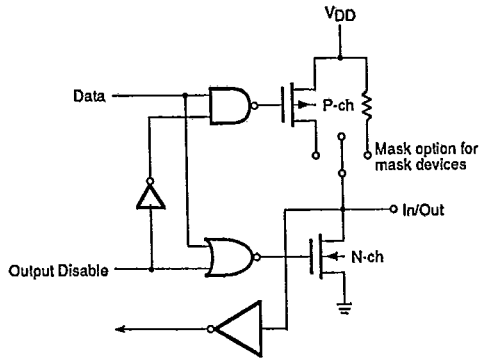
When a voltage of 21 V is applied to this pin, V_{PP} is supplied to the PROM unit. When input of V_{SS} to V_{DD} is applied, V_{DD} is supplied to this pin.

Type D
(for Types W and X)

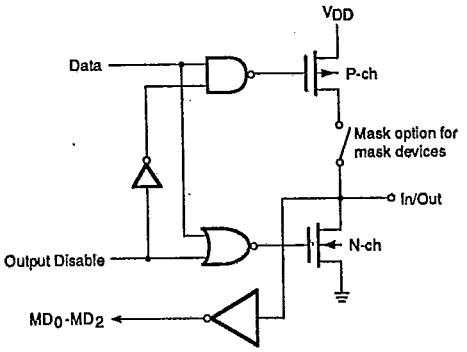


Push-pull output where output can be placed in high impedance when a RESET input is applied. P and N channels are turned off.

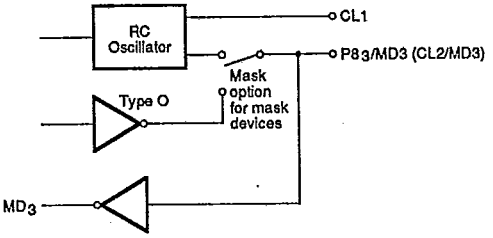
Type P



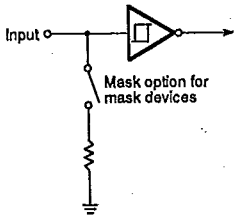
Type P-A



Type Q-A



Type R



Type S

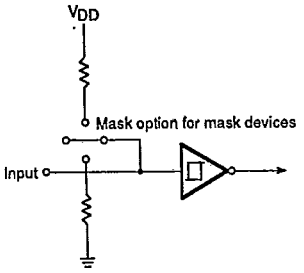


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Figure 1. Interface at I/O Ports (cont)

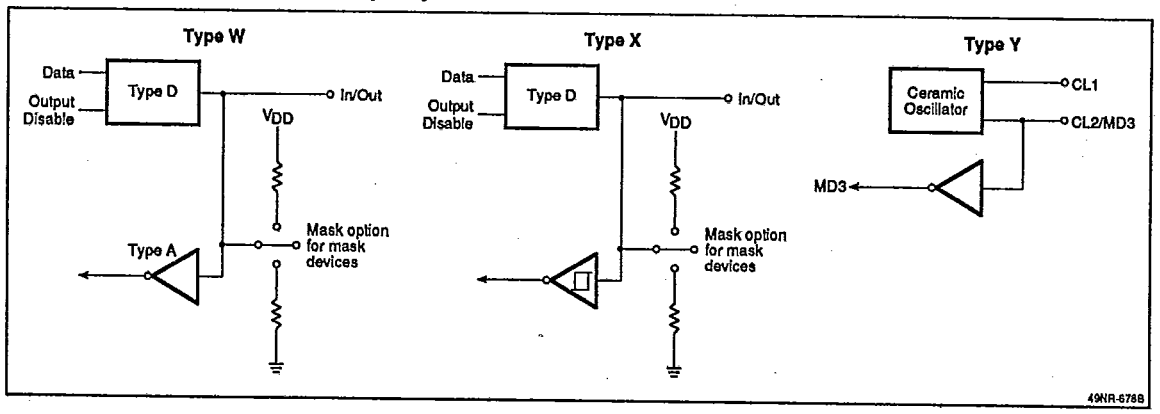


Table 1 compares the features of the μPD7554/64 and their OTP versions, μPD75P54/P64.

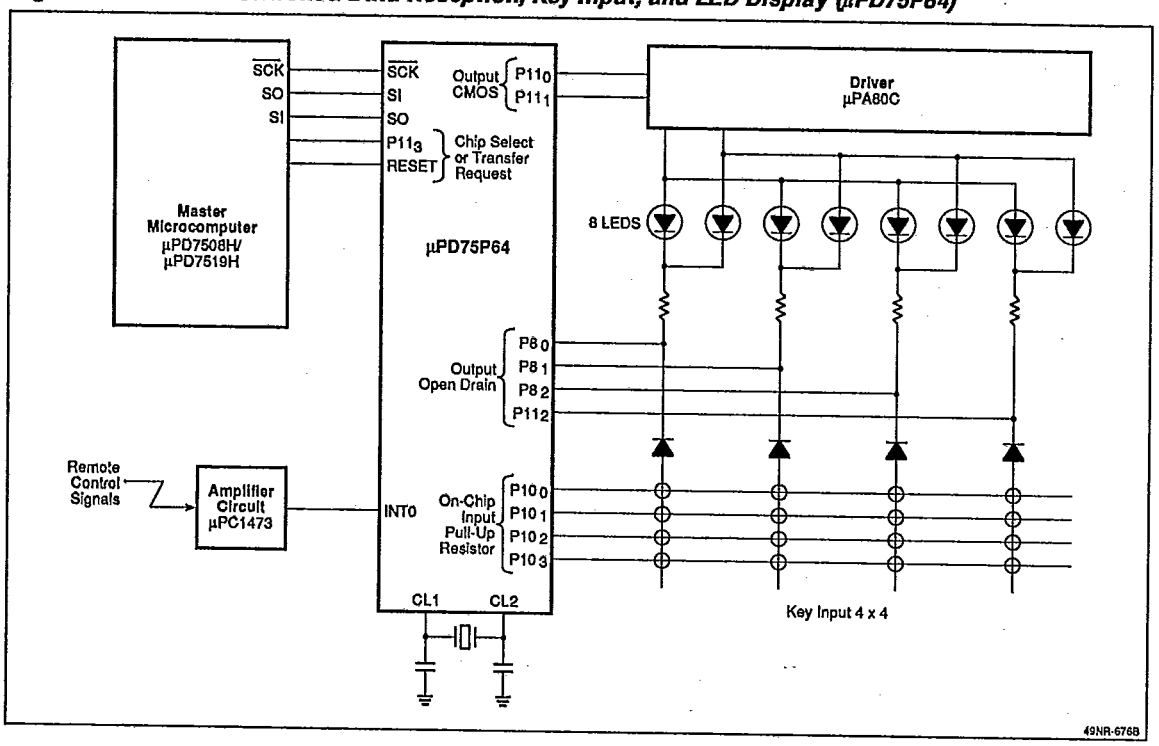
Table 1. Product Differences and Comparisons, μPD7554/64 and μPD75P54/P64

Item		μPD7554	μPD7564	μPD75P54 (OTP)	μPD75P64 (OTP)
Instruction cycle/system clock (5 V)	RC	4 μs/ 500 kHz	4 μs/ 500 kHz	4 μs/ 500 kHz	
	External	2.86 μs/ 700 kHz		2.86 μs/ 700 kHz	
	Ceramic		3 μs/ 660 kHz		2.86 μs/ 700 kHz
Instruction set		47 (set B)	47 (set B)	47 (set B)	47 (set B)
ROM or PROM		1024 x 8 mask ROM	1024 x 8 mask ROM	1024 x 8 one-time PROM	1024 x 8 one-time PROM
RAM		64 x 4	64 x 4	64 x 4	64 x 4
I/O port total		16 (max)	15	16 (max)	15
Port 0		$P0_0$-$P0_3$	$P0_0$-$P0_3$	$P0_0$-$P0_3$/MD0-MD3	$P0_0$-$P0_3$/MD0-MD3
$P0_0$ pin mask option		Available	Available	None	None
Port 8		$P8_0$-$P8_2$ $P8_3$/CL2	$P8_0$-$P8_2$	$P8_0$-$P8_2$/MD0-MD2 $P8_3$/MD3	$P8_0$-$P8_2$/MD0-MD2 CL2/MD3
Port 10		$P10_0$-$P10_3$	$P10_0$-$P10_3$	$P10_0$-$P10_3$/D_0-D_3	$P10_0$-$P10_3$/D_0-D_3
Port 11		$P11_0$-$P11_3$	$P11_0$-$P11_3$	$P11_0$-$P11_3$/D_4-D_7	$P11_0$-$P11_3$/D_4-D_7
Timer/event counter		8-bit	8-bit	8-bit	8-bit
Serial interface		8-bit	8-bit	8-bit	8-bit
Sense input		INT0, INTS, INTT	INT0, INTS, INTT	INT0, INTS, INTT	INT0, INTS, INTT
Supply voltage		2.5 to 6.0 V	2.7 to 6.0 V	4.5 to 6.0 V	4.5 to 6.0 V
Process		CMOS	CMOS	CMOS	CMOS
Package		20-pin plastic SOP	20-pin plastic SOP	20-pin plastic SOP	20-pin plastic SOP
		20-pin shrink DIP	20-pin shrink DIP	20-pin shrink DIP	20-pin shrink DIP
Output and I/O pins		N-channel open drain	N-channel open drain	N-channel open drain	N-channel open drain
Input pins		Mask options available	Mask options available	No on-chip resistor	No on-chip resistor
RESET		Mask options available	Mask options available	No pull-down resistor	No pull-down resistor

μPD75P64 Application

Figure 2 shows an example of an application circuit for remote-controlled data reception, key input, and LED display for the μPD75P64.

Figure 2. Remote-Controlled Data Reception, Key Input, and LED Display (μPD75P64)



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OTP PROM (Program Memory Write and Verify)

The μPD75P54/P64 is a, one-time programmable (OTP) PROM version of the μPD7554/64. The OTP is programmed by the pins and their functions listed in table 2. During OTP programming, addresses are updated by inputting clocks, instead of addresses, from the CL1 pin.

Table 2. OTP Access

Pin	Function
V_{PP}	OTP programming voltage pin (normally V_{DD})
CL1	Address update clock input during programming
MD0-MD3	Mode selection during OTP programming
D_0-D_7	8-bit data I/O pins during OTP programming
V_{DD}	Supply voltage pin: 4.5 to 6.0 V during normal operation; 6 V during OTP programming

Notes:

The μPD75P54/P64 has no erasure window. The program memory data cannot be erased with ultraviolet light.

OTP Operation Mode

The μPD75P54/P64 operates in the program memory write/verify mode when +6 V is applied to V_{DD} and 21 V to V_{PP}. Mode pins MD0-MD3 select the operation modes shown in Table 3.

Table 3. OTP Operation Mode Selection

V_{PP} = +21 V; V_{DD} = +6 V

MD0	MD1	MD2	MD3	Operating Mode
H	L	H	L	Program memory address clear (Note 2)
L	H	H	H	Program memory write (Note 3)
L	L	H	H	Program memory verify (Note 4)
H	X	H	H	Program inhibit (Note 5)

Notes:

(1) X = L or H.

(2) While HLHL is being applied, the program counter continues to be cleared.

(3) While LHHH is being applied, data applied to D0-D7 continue to be written to the OTP.

(4) While LLHH is being applied, the OTP contents at the address that the program counter indicates continue to be output to P0-D7.

(5) While HXHH is being applied, the OTP continues to be nonaccessible, and D0-D7 remain at a high impedance level.

Program Memory Write Procedure. The program memory write procedure follows (high speed write is enabled):

(1) Connect unused pins to V_{SS} through a pull-down resistor. RESET is pulled up to V_{DD} through a resistor. Hold CL1 low.

(2) Supply 5 V to V_{DD} and V_{PP}.

(3) Select the program memory address clear mode.

(4) Change the voltage on V_{DD} to 6 V, and on V_{PP} to 21 V.

(5) Select the program inhibit mode.

(6) Write data in the 1 ms write mode.

(7) Select the program inhibit mode.

(8) Select the verify mode. If data is written correctly, proceed to step 9; if data is not written correctly, repeat steps 6-8.

(9) Perform an additional write of X (number of times a write was performed in steps 6-8) x 1 ms.

(10) Select the program inhibit mode.

(11) Increment the program memory address by one, by inputting four pulses to CL1.

(12) Repeat steps 6-11 until the end address occurs.

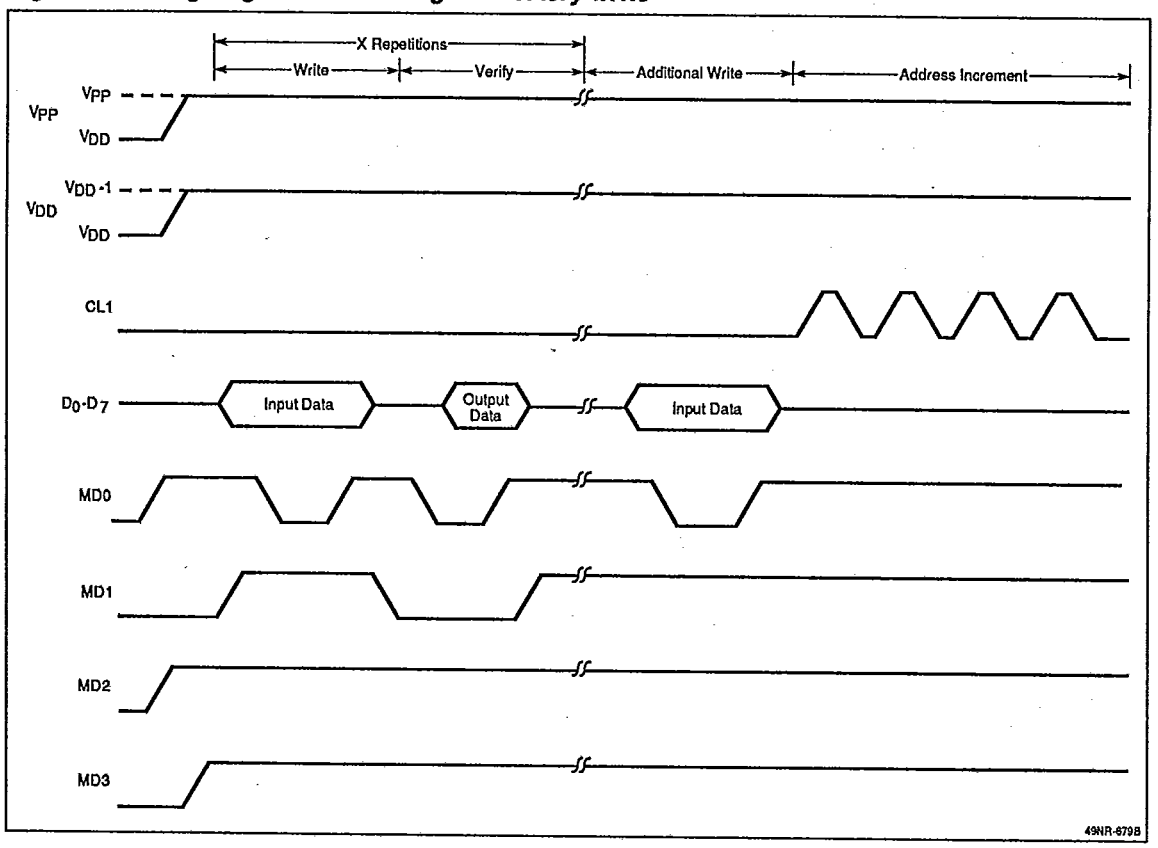
(13) Select the program memory address clear mode.

(14) Change the voltage on V_{DD} and V_{PP} to 5 V.

(15) Turn off power.

The timing for steps 2-11 is shown in figure 3.

Figure 3. Timing Diagram for OTP Program Memory Write



Program Memory Read Procedure. The program memory read procedure follows:

(1) Connect unused pins to V_{SS} through a pull-down resistor. RESET is pulled up to V_{DD} through a resistor. Hold CL1 low.

(2) Supply 5 V to V_{DD} and V_{PP}.

(3) Select the program memory address clear mode.

(4) Change the voltage on V_{DD} to 6 V, and on V_{PP} to 21 V.

(5) Select the program inhibit mode.

(6) Select the verify mode. Data is read from "000H." Upon entry of a clock pulse to CL1, data is sequentially output by one address in a cycle of four pulses.

(7) Pulse input to the CL1. Program memory address is updated at the rising edge of the third pulse. Address after updated one (+1) is updated every four pulses. Repeat update to last address.

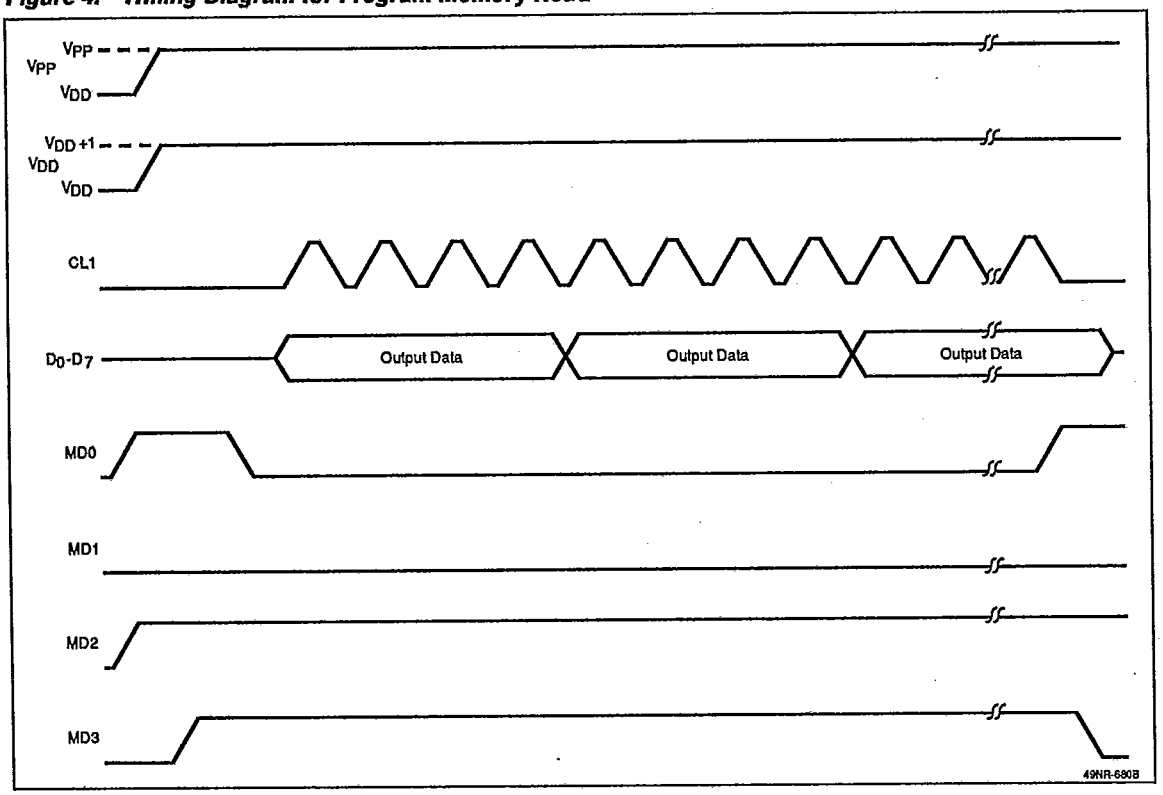
(8) Select the program memory address clear mode.

(9) Change the voltage on V_{DD} and V_{PP} to 5 V.

(10) Turn off power.

The timing for steps 2-9 is shown in figure 4.

Figure 4. Timing Diagram for Program Memory Read



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	
Except ports 10, 11	−0.3 to V_{DD} +0.3 V
Ports 10, 11 (Note 1)	−0.3 to V_{DD} +0.3 V
Ports 10, 11 (Note 2)	−0.3 to +13 V
Output voltage, V_O	
Except ports 10, 11	−0.3 to V_{DD} +0.3 V
Ports 10, 11 (Note 1)	−0.3 to V_{DD} +0.3 V
Ports 10, 11 (Note 2)	−0.3 to +13 V
Output current, high I_{OH}	
One pin	−5 mA
All output pins, total	−15 mA
Output current, low I_{OL}	
$P0_1$, $P0_2$	5 mA
Ports 10, 11	15 mA
Port 8	30 mA
All ports, total	100 mA
Power dissipation, P_D (T_A = +70°C)	
Shrink DIP	480 mW
SOP	250 mW

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) CMOS I/O or N-channel open drain + internal pull up resistor.

(2) N-channel open drain I/O.

Capacitance

T_A = 25°C, V_{DD} = V_{SS} = 0 V; f = 1 MHz. Unmeasured pins returned to V_{SS}.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			50	pF	$P0_0$
				15	pF	$P0_3$
Output capacitance	C_O			35	pF	Port 8
I/O capacitance	$C_{I/O}$			35	pF	Ports 10, 11 and $P0_1$, $P0_2$

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DC Characteristics, Normal Operation; V_{DD} = 4.5 to 6.0 V; V_{SS} = 0 V

T_A = −10 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high voltage except CL1	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
Input high voltage CL1	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	
Input high voltage ports 10, 11 (Note 1)	V_{IH3}	0.7 V_{DD}		12	V	
Input high voltage RESET	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	Data retention mode
Input low voltage except CL1	V_{IL1}	0		0.3 V_{DD}	V	
Input low voltage CL1	V_{IL2}	0		0.5	V	
Input leakage current except CL1	I_{LI1}	−3		3	μA	0 V ≤ V_I ≤ V_{DD}
Input leakage current CL1	I_{LI2}	−10		10	μA	0 V ≤ V_I ≤ V_{DD}
Input leakage current ports 10, 11	I_{LI3}			10 (Note 1)	μA	V_I = 12 V
Output voltage high PO_1, PO_2, ports 8-11	V_{OH}	V_{DD} − 2.0			V	I_{OH} = −1 mA
Output voltage low PO_1, PO_2, ports 10, 11	V_{OL}			0.4	V	PO_1, PO_2: I_{OL} = 1.6 mA; Ports 10, 11: I_{OL} = 1.6 mA
Output voltage low ports 8, 10, 11	V_{OL}			2.0	V	Port 8: I_{OL} = 15 mA Ports 10, 11: I_{OL} = 10 mA
Output leakage current	I_{LO1}	−3		3	μA	0 V ≤ V_O ≤ V_{DD}
Output leakage current ports 8-11	I_{LO2}			10 (Note 1)	μA	V_O = 12 V
Supply voltage, data retention mode	V_{DDDR}	2.0		6.0	V	
Supply current, normal operation	I_{DD1}		400	1400	μA	μPD75P54: V_{DD} = 5 V ±10%; R = 56 kΩ ±2%
			700	2300	μA	μPD76P64: V_{DD} = 5 V ±10%; f_{CC} = 700 kHz
Supply current, HALT mode	I_{DD2}		120	400	μA	μPD75P54: V_{DD} = 5 V ±10%; R = 56 kΩ ±2%
			450	1500	μA	μPD 75P64: V_{DD} = 5 V ±10%; f_{CC} = 700 kHz
Supply current, STOP mode	I_{DD3}		0.1	10	μA	V_{DD} = 5.0 V ±10%
Supply current, data retention mode	I_{DDDR}		0.1	5	μA	V_{DDDR} = 2.0 V

Notes:

(1) N-channel, open drain I/O ports.

DC Characteristics, Programming Mode; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 21 ± 0.5 V, V_{SS} = 0 V (Notes 1 and 2)

T_A = 25°C

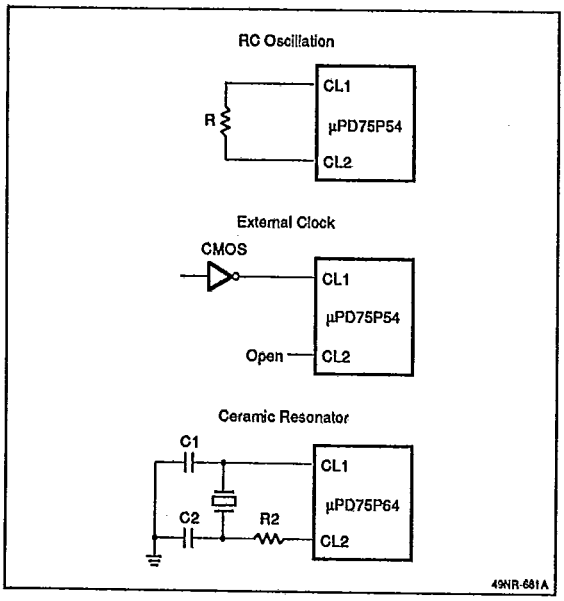
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input high voltage except CL1	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
Input high voltage CL1	V_{IH2}	V_{DD} – 0.5		V_{DD}	V	
Input low voltage except CL1	V_{IL1}	0		0.3 V_{DD}	V	
Input low voltage CL1	V_{IL2}	0		0.5	V	
Input leakage current	I_{LI}			10	μA	V_I = V_{IL} or V_{IH}
Output voltage high	I_{OH}	V_{DD} – 2.0			V	I_{OH} = –1 mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply voltage	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Notes:

(1) V_{PP}, including an overshoot, should not exceed +22 V.

(2) Apply V_{DD} before V_{PP}, and cut off after V_{PP}.

Figure 5. Recommended Circuits



AC Characteristics, Normal Operation; V_{DD} = 4.5 to 6.0 V; V_{SS} = 0 V

T_A = −10 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
System clock oscillation frequency	f_{CC}	400	500	600	kHz	μPD75P54: R = 56 kΩ ±2%
		290		710	kHz	μPD75P64: R = 100 kΩ ±2%
External clock frequency, CL1	f_C	10		710	kHz	μPD75P54: 50% duty
Oscillation stabilization time	t_{OS}	20			ms	μPD75P64 (Note 1)
System clock rise time, CL1	t_{CR}			0.2	μs	
System clock fall time, CL1	t_{CF}			0.2	μs	
System clock pulse width	t_{CH}	0.7		50	μs	
System clock pulse width, CL1	t_{CL}	0.7		50	μs	
Event input frequency ($P0_0$)	f_{P0}	0		710	kHz	50% duty
$P0_0$ rise time	t_{POR}			200	ns	
$P0_0$ fall time	t_{POF}			200	ns	
$P0_0$ pulse width, high	t_{P0H}	0.7			μs	V_{DD} = 4.5 to 6.0 V
$P0_0$ pulse width, low	t_{P0L}	0.7			μs	V_{DD} = 2.7 V
INT0 high time	t_{IOH}	10			μs	
INT0 low time	t_{IOL}	10			μs	
RESET high time	t_{RSH}	10			μs	
RESET low time	t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	
$\overline{SCK}$ cycle time	t_{KCY}	2.0			μs	Input
		2.5			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.0			μs	Input
$\overline{SCK}$ pulse width, low	t_{KL}	1.25			μs	Output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	0.1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	0.1			μs	
SO output delay time after $\overline{SCK}$ ↑	t_{KSO}			0.85	μs	CL = 100 pF

Notes:

(1) Hold the RESET signal at a high level until oscillation becomes stable.

AC Characteristics, Programming Mode; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 21 ±0.5 V, V_{SS} = 0 V

T_A = 25°C

Parameter	Symbol	Note 1	Min	Typ	Max	Unit	Conditions
Address setup time for MD0 ↓ (Note 2)	t_{AS}	t_{AS}	2			μs	
MD1 setup time for MD0 ↓	t_{MIS}	t_{OES}	2			μs	
Data setup for MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address hold time for MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2			μs	
Data hold time for MD0↑	t_{DH}	t_{DH}	2			μs	
MD0 ↑ to data output float delay time	t_{DF}	t_{DF}	0		200	ns	
V_{PP} setup time for MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time for MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 setup time for MD1 ↑	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ to data output delay time	t_{DV}	t_{DV}			1 (Note 3)	μs	MD0 = MD1 = V_{IL}
MD1 hold time for MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{MIR} \geq 50$ μs
MD1 recovery time for MD0 ↓	t_{M1R}	t_{OR}	2			μs	
Program counter reset time	t_{PCR}		10			μs	
CL1 input high- and low-level widths	t_{XH}, t_{XL}		0.7			μs	
CL1 input frequency	f_X				710	kHz	
Initial mode set time	t_I		2			μs	
MD3 setup time for MD1 ↑	t_{M3S}		2			μs	
MD3 hold time for MD1 ↓	t_{M3H}		2			μs	
MD3 setup time for MD0 ↓	t_{M3SR}		2			μs	During program memory read
Address to data output delay time (Note 2)	t_{DAD}	t_{ACC}	2			μs	
Address to data output hold time (Note 2)	t_{HAD}	t_{OH}	0		300	ns	
MD3 hold time for MD0 ↑	t_{M3HR}		2			μs	
MD3 ↓ to data output float delay time	t_{DFR}		2			μs	

Notes:

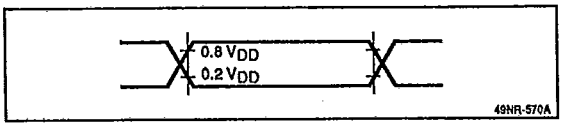
(1) Symbol of the corresponding μPD27C256.

(2) "1" is added to the internal address signal at the rising edge of the third CL1 input. The signal is not input to the pin.

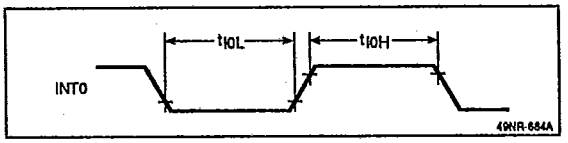
(3) During CMOS output.

Timing Waveforms

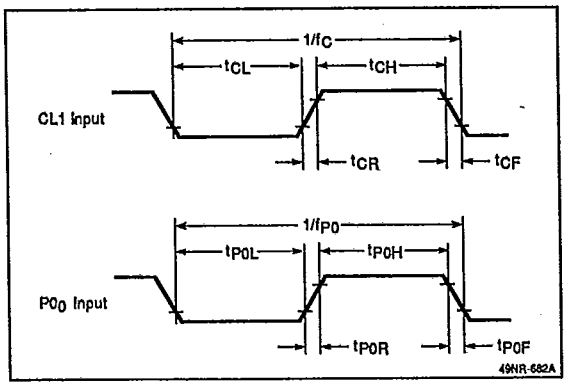
AC Test Points



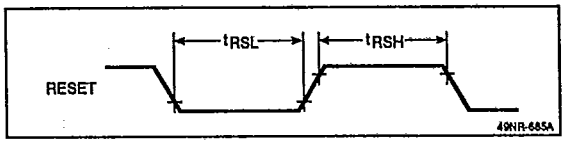
Test



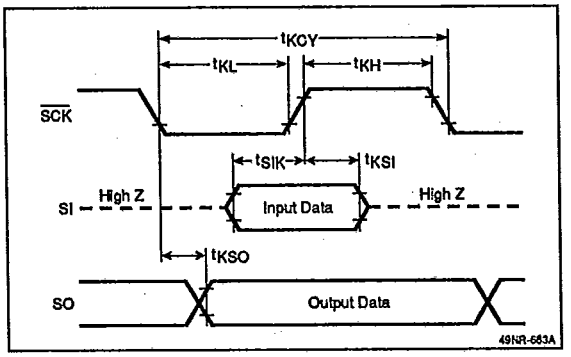
Clock



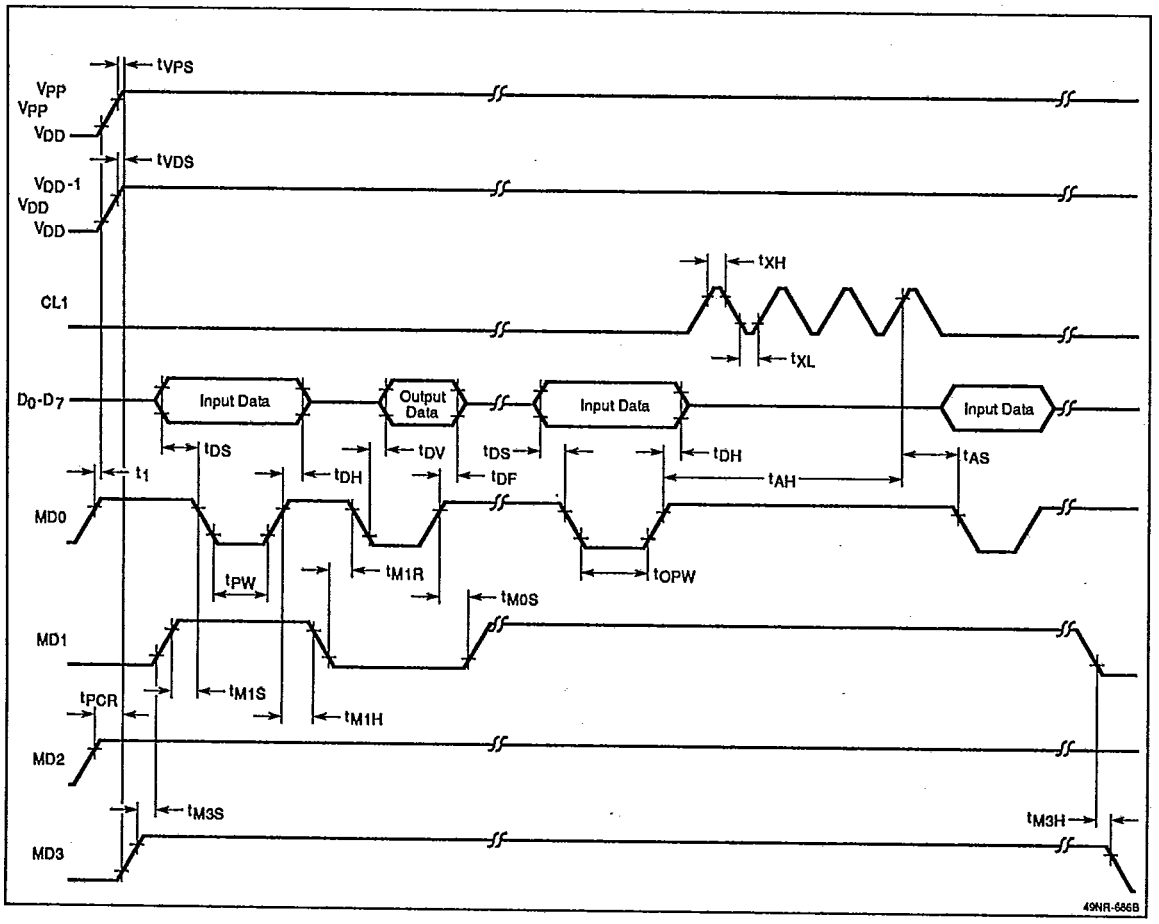
RESET



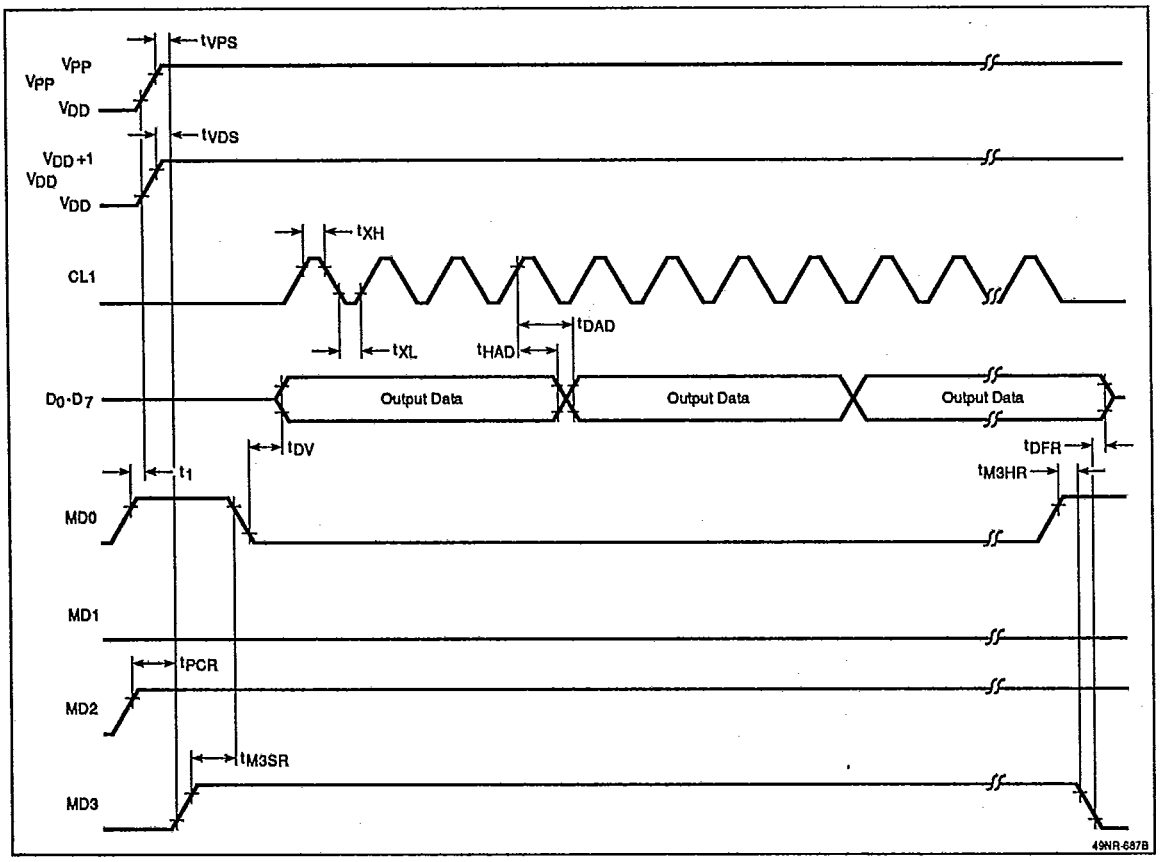
Serial Transfer



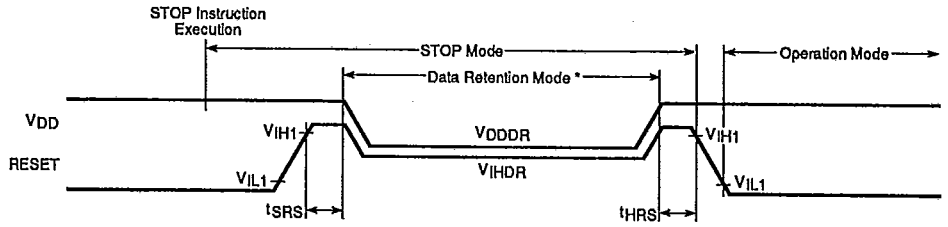
Program Memory Write



Program Memory Read



Data Retention Timing, μPD75P54



* In the data retention mode, set all inputs to a value smaller than V_{DDDR}.

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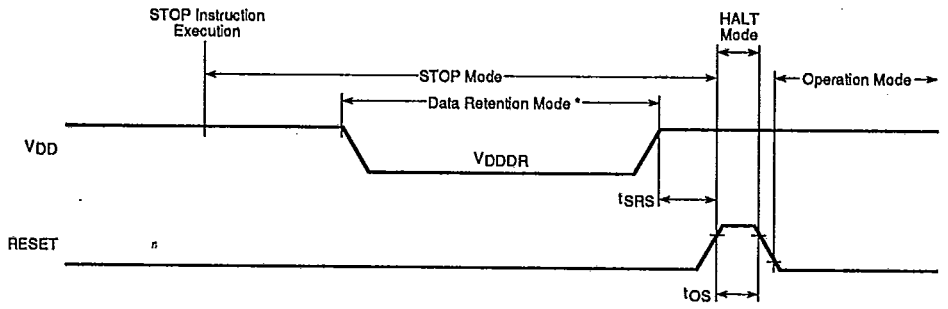
Data Retention Timing, μPD75P64



* In the data retention mode, set all inputs to a value smaller than V_{DDDR}.

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