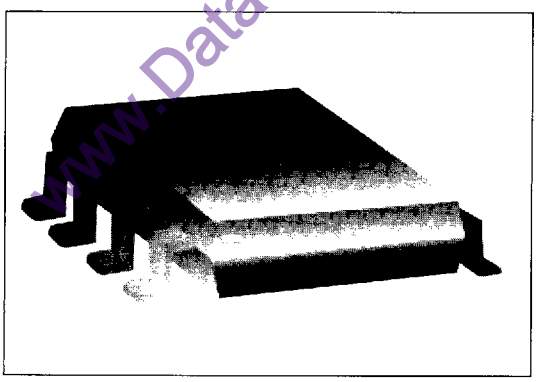
IRM7000
DATA TRANSCEIVER
Preliminary



FEATURES
- **Simplifies Connection to 16550 UART**
- **Compatible with IrDA Physical Layer Specification**
- **Compatible with Siemens IRM3105 and IRM3001 Transceivers**
- **Based on 1 Micron CMOS Gate Array Design**
- **Performs Pulse Shaping Function Between Siemens Transceivers, IRM3001/IRM3105, and other applications:**
  - **Hand Held Data Collection Devices**
  - **Automotive Diagnostics**
  - **Telecommunication Systems**
  - **Laptop Computers**
  - **Palmtop Computers**
  - **Computer Peripherals**
  - **Consumer Electronics**

DESCRIPTION
The IRM7000 is a modulator/demodulator interface which encodes in the transmit block and decodes in the receive block. In many applications, a standard 16550 UART is used which has a BAUDOUT signal as an external signal. The IRM7000 can be used in conjunction with the UART to shape electrical pulses.

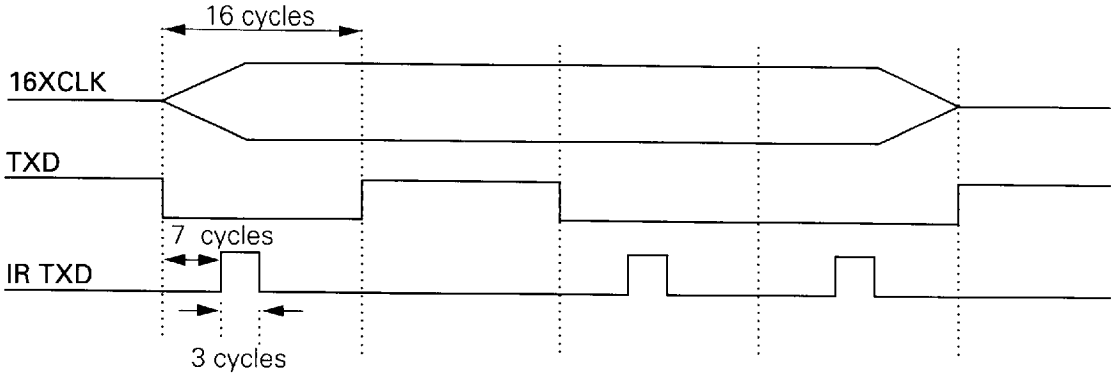
The Encode and Decode function both rely on a 16XCLK which is set to 16 times the data transmission. The Encode scheme is a modulated TXD signal which drives the transceiver and sends a pulse for every (0) that is sent, and a no pulse for every (1) transmitted. The Decode scheme receives a $^3/_{16}$th signal from the transceiver and is demodulated (stretched) to accommodate 1-bit time. The IRM7000 is based on 1-micron technology using CMOS gate array design.

Pin Functions

Pin no.	Name	Function
1	16XCLK	Positive edge triggered input clock signal that is set to 16 times the data transmission baudrate. The encoding and decoding schemes require the presence of this signal. Typically, the signal is tied to the UART's BAUDOUT signal.
2	TXD	Negative edge triggered input signals that is normally tied to the SOUT signal of a UART (serial dat to be transmitted). Data is modulated and output is IR_TXD.
3	RCV	Output signal normally tied to UART SIN signal (received serial data). Demodulated output.
4	GND	Chip package ground
5	NRST	Active low signal used to reset the Decode state machine. Normally tied to POR (power on reset line of the circuit or V_{CC}. Also can be used to disable data reception.
6	IR_RCV	Input from transceiver at $^3/_{16}$th pulse time pulse centered around the bit of information (0) that is being transmitted. For consecutive spaces, pulses with a 1 bit time delay are generated in series. If a logic 1 (mark) is sent, then the encoder does not generate a pulse.
7	IR_TXD	Modulated TXD signal from transceiver
8	V_{CC}	Power

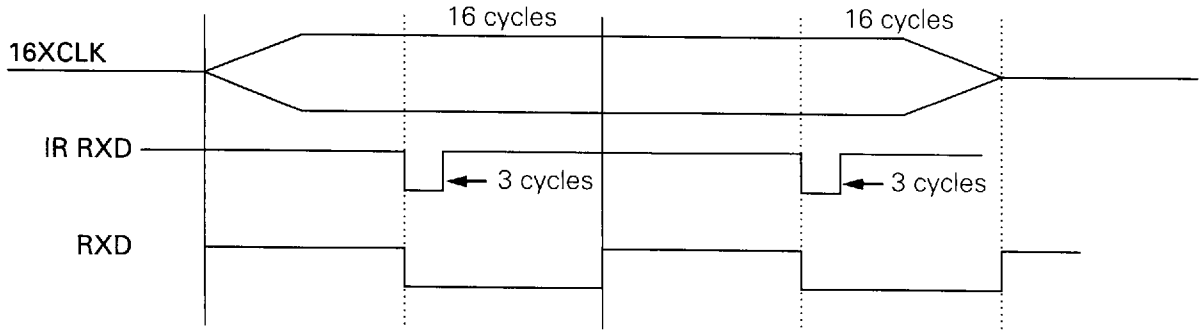
Encoding Scheme

The encoding scheme relies on a resident clock which is set to 16X the data transmission baud rate.



The encoder sends a pulse for every space (0) that is sent. On a high to low transition of the TXD line, the pulse generation is delayed for 7 clock cycles of the 16XCLK clock before the pulse is set high for 3 clock cycles ($3/16$ of bit time) and subsequently pulled low. In essence, this generates a $3/16$th bit time pulse centered around the bit of information (0) that is being transmitted. For consecutive spaces, pulses with a 1-bit time delay are generated in series. If a logic 1 (mark) is sent, then the encoder does not generate a pulse.

Decoding Scheme



The decoding modulation method can described as a pulse stretching scheme. Every high to low transition of the IR_RXD line signifies the arrival of a $3/16$th pulse. This pulse needs to be stretched to accommodate 1-bit time or 16 clock cycles. Every pulse that is received is translated into a "0"or space on the RXD line. If a series of pulses separated by 1-bit time are received, then the net result is a 1-bit time low pulse for every $3/16$th pulse received. To be correctly received and interpreted by a UART, the stretched pulse must at least last $3/4$ of a bit time.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	−0.5	+6.5	V
Input/Output Voltage	V_I/V_O	−0.5	V_{CC} +0.5	V
Power Dissipation	P_{MAX}		0.22	W
Output Current	I_O		10	mA
Operating Temperature	T_A	−10	+85	°C
Storage Temperature	T_S	−65	+150	°C

Switching Characteristics V_{CC}=5 V ±10% T_A=–40 to +85°C

Parameter	Symbol	Typ.	Unit
Toggle Frequency	f_{tog}	120	MHz
Propagation Delay Time	t_{pd}	0.5 1.0 2.0	ns ns ns
Output Rise Time	t_r	1.54	ns
Output Fall Time	t_r	1.42	ns

Capacitance V_{CC}=0 V, T_A=–40 to +85°C

Parameter	Symbol	Condition	Typ.	Max.	Unit
Input Capacitance	C_{IN}	f=1 MHz, unmeasured pins returned to 0 V	10	20	pF
Output Capacitance	C_{OUT}		10	20	pF
Output Fall Time			10	20	pF

Recommended Operating Conditions T_A=–40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	CMOS Level	4.0	5.0	5.5	mA
Input Voltage	V_I	CMOS Level	0		V_{CC}	V
Ambient Temperature	T_A	CMOS Level	–40		+85	°C
High Level Input Voltage	VIH	CMOS Level	0.7 V_{CC}		V_{CC}	V
Low Level Input Voltage	VIL	CMOS Level	0		0.3 V_{CC}	V
Positive Trigger Voltage	V_P	CMOS Level	1.61		4.00	V
Negative Trigger Voltage	V_N	CMOS Level	0.55		3.10	V
Hysteresis Voltage	V_H	CMOS Level	0.50		2.00	V
Power Dissipation	P_{DISS}	f_{16XCLK}=2 MHz		4.9	220	mW
Input Rise /Fall Time	t_r, t_f	f_{16XCLK}=2 MHz			200	ns
Maximum Clk Frequency (16XCLK)*	f_{16XCLK}				2	MHz
Minimum Pulse Width (IR_TXD)†	t_{mpx}	f_{16XCLK}=2 MHz	250			ns

* The Max Clk Frequency (f_{16XCLK}) represents the maximum clock frequency that the IRM7000's internal state machine can be driven. Under normal conditions, this clock input should not exceed the maximum transmission rate recommended in the IrDA 1.0 specification—16*115.s Kb/s or 1.84 MHz.

† The Minimum Pulse Width (t_{mpx}) represents the minimum pulse width of the encoded IR_TXD pulse (as well as the minimum pulse width for the IR_RCD) pulse. IrDA 1.0 specifies the minimum pulse width of the IR_TXD and IR_RCV to be 3*(1/1.84 MHz) or 1.63 µs. The minimum pulse width that can be handled by the IRM7000 is 250 ns. Under normal conditions and using a 16XCLK that does not exceed 1.84 MHz, the minimum pulse width of IR_TXD should not be more than 1.63 µs.