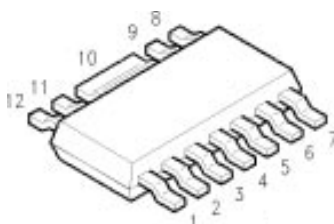


Datasheet

<p>*Power amplifier for GSM or AMPS application *Fully integrated 2 stage amplifier *Operating voltage range: 2.7 to 6 V *Overall power added efficiency 45 % *Input matched to 50 ohms, simple output match</p> <p>ESD: ElectroStatic discharge sensitive device, observe handling precautions!</p>	
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Type	Marking	Ordering code (taped)	Package ¹⁾
CGY 92	CGY 92	Q68000-A8884	MW 12

Maximum ratings

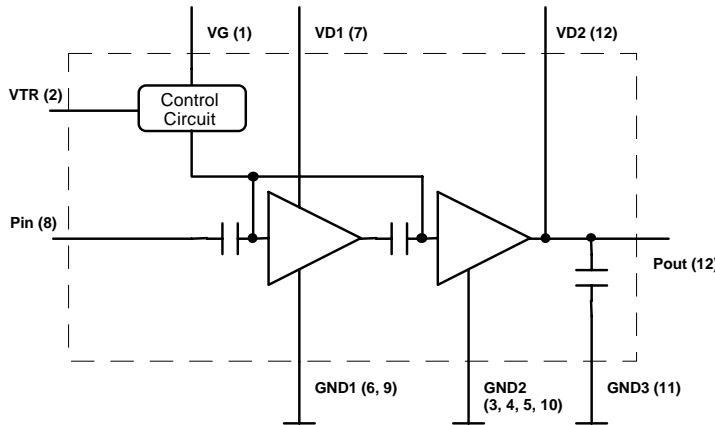
Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	9	V
Negative supply voltage	V_G	-6	V
Supply current	I_D	2	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
RF input power	P_{in}	25	dBm
Pulse peak power dissipation <i>duty cycle 12.5%, $t_{on}=0.577ms$</i>	P_{Pulse}	9	W
Total power dissipation (CW, $T_s \leq 81^\circ C$) <i>T_s: Temperature at soldering point</i>	P_{tot}	5	W

Thermal Resistance

Channel-soldering point	R_{thChS}	≤ 14	K/W
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1) Plastic body identical to SOT 223, dimensions see page 14

Functional block diagramm:



Control circuit:

The drain current I_D of the CGY 92 is adjusted by the internal control circuit. Therefore a negativ voltage (-4V...-6V) has to be supplied at VG. For transmit operation VTR must be set to 0V. During receive operation VTR should be disconnected (shut off mode).

Pin #		Configuration
1	VG	Negative voltage at control circuit (-4V...-6V)
2	VTR	Control voltage for transmit mode (0V) or receive mode (open)
3,4,5,10	GND 2	RF and DC ground of the 2nd stage
6,9	GND 1	RF and DC ground of the 1st stage
7	VD1	Positive drain voltage of the 1st stage
8	RFin	RF input power
11	GND 3	Ground for internal output matching
12	VD2, RFout	Positive drain voltage of the 2nd stage, RF output power

DC characteristics

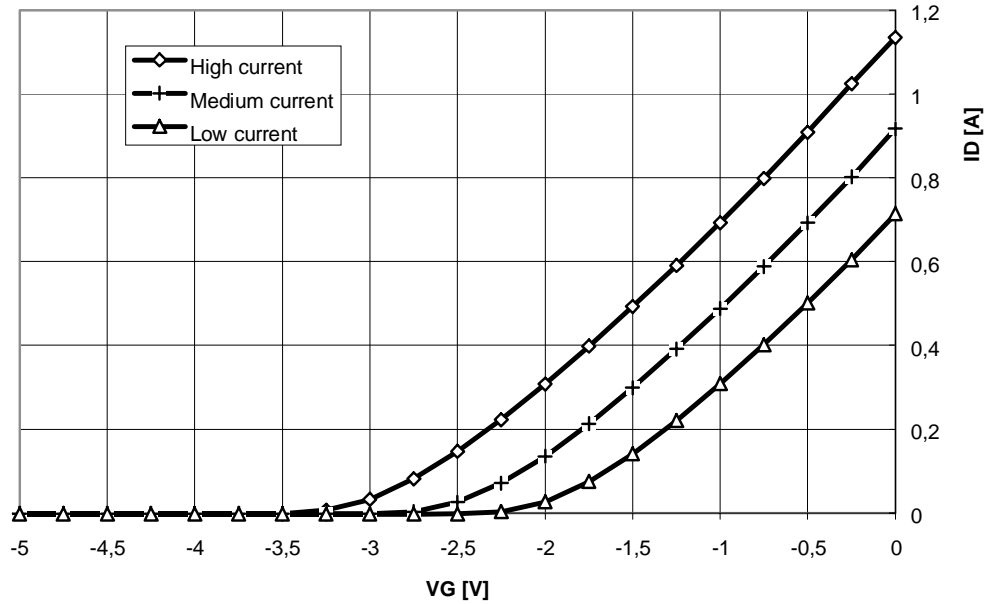
Characteristics	Symbol	Conditions	min	typ	max	Unit
Drain current stage 1	$IDSS1$	VD=3V, VG=0V, VTR n.c.	0.6	0.9	1.2	A
	stage 2		$IDSS2$	2.4	3.5	4.8
Drain current with active current control	ID	VD=3V, VG=-4V, VTR=0V	-	1.0	-	A
Transconductance (stage 1 and 2)	$gfs1$	VD=3V, ID=350mA	0.28	0.32	-	S
	$gfs2$	VD=3V, ID=700mA	1.1	1.3	-	S
Pinch off voltage	Vp	VD=3V, ID<500μA (all stages)	-3.8	-2.8	-1.8	V

Electrical characteristics

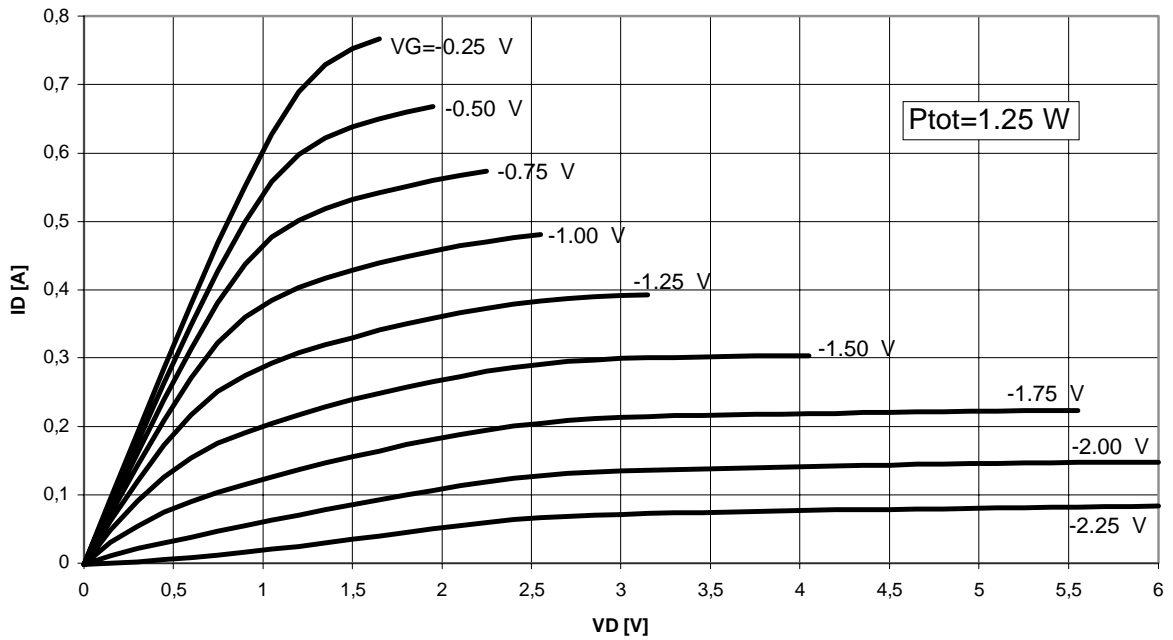
($T_A = 25^\circ\text{C}$, $f=0.9\text{ GHz}$, $Z_S=Z_L=50\text{ Ohm}$, $V_D=3.0\text{V}$, $V_G=-4\text{V}$, VTR pin connected to ground, unless otherwise specified, pulsed with a duty cycle of 10%, $t_{on}=0.33\text{ms}$)

Characteristics	Symbol	min	typ	max	Unit
Supply current <i>P_{in}=10dBm</i>	I_{DD}	-	1.05	-	A
Negative supply current <i>(normal operation)</i>	I_G	-	2	-	mA
Shut-off current <i>VTR n.c.</i>	I_D	-	400	-	μA
Negative supply current <i>(shut off mode, VTR pin n.c.)</i>	I_G	-	10	-	μA
Small signal gain <i>P_{in} = -5dBm</i>	G	27.0	29.0	-	dB
Power gain <i>V_D=3V; P_{in}=10dBm</i>	G	21.0	21.8	-	dB
Output Power <i>V_D=3V; P_{in}=10dBm</i>	P_O	31.0	31.8	-	dBm
Output Power <i>V_D=3.6V; P_{in}=10dBm</i>	P_O	32.3	33.1	-	dBm
Output Power <i>V_D=5V; P_{in}=10dBm</i>	P_O	34.0	35.0	-	dBm
Overall Power added Efficiency <i>V_D=3V; P_{in}=10dBm</i>	η	43	48	-	%
Overall Power added Efficiency <i>V_D=3.6V; P_{in}=10dBm</i>	η	41	46	-	%
Overall Power added Efficiency <i>V_D=5V; P_{in}=10dBm</i>	η	40	45	-	%
Harmonics (<i>P_{in}=10dBm</i>) <i>V_D=3V; (P_{out}=32dBm)</i>	$2f_0$	-	-	-46	dBc
	$3f_0$	-	-	-37	dBc
Harmonics (<i>P_{in}=10dBm</i>) <i>V_D=5V; (P_{out}=35dBm)</i>	$2f_0$	-	-	-48	dBc
	$3f_0$	-	-	-38	dBc
Input VSWR <i>V_D=3.0V;</i>	-	-	1.7 : 1	2.0 : 1	-
Third order intercept point <i>V_D=3V; pulsed with a duty cycle of 10%;</i> <i>f₁=900.00MHz; f₂=900.20MHz;</i>	IP_3	-	40	-	dBm
Third order intercept point <i>V_D=4.8V; pulsed with a duty cycle of 10%;</i> <i>f₁=900.00MHz; f₂=900.20MHz;</i>	IP_3	-	45	-	dBm

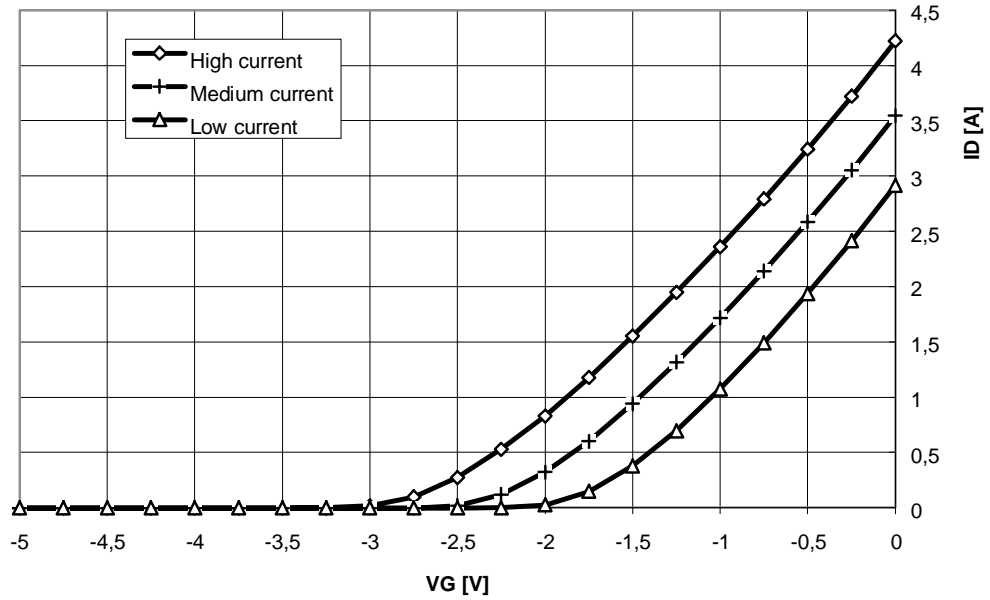
DC-ID(VG) characteristics - typical values of stage 1, VD=3V



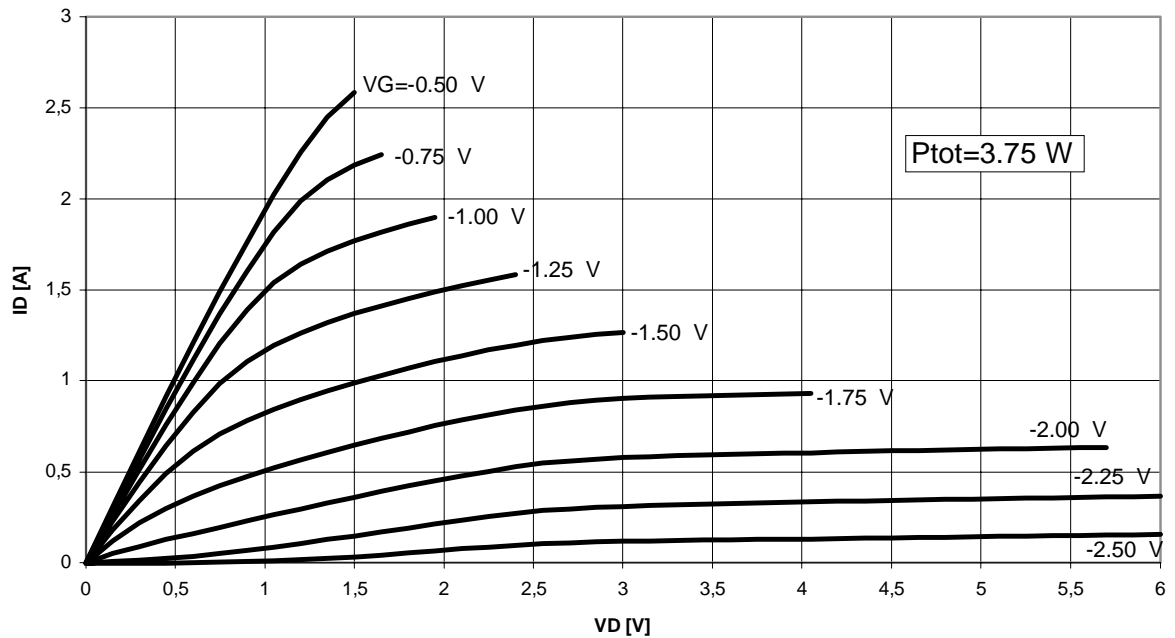
DC-Output characteristics - typical values of stage 1



DC-ID(VG) characteristics - typical values of stage 2, VD=3V

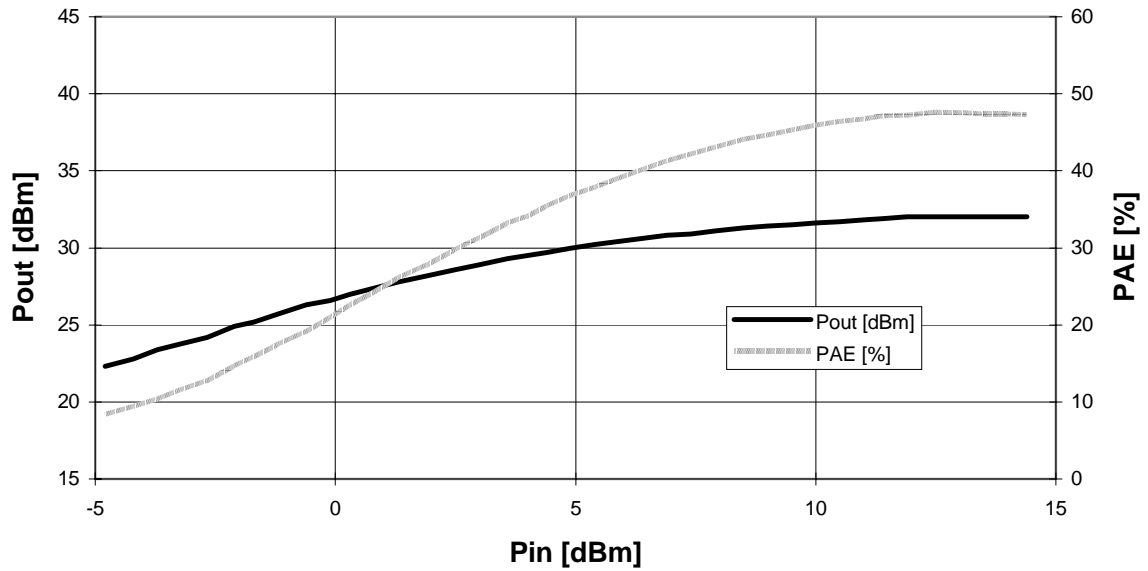


DC-Output characteristics - typical values of stage 2



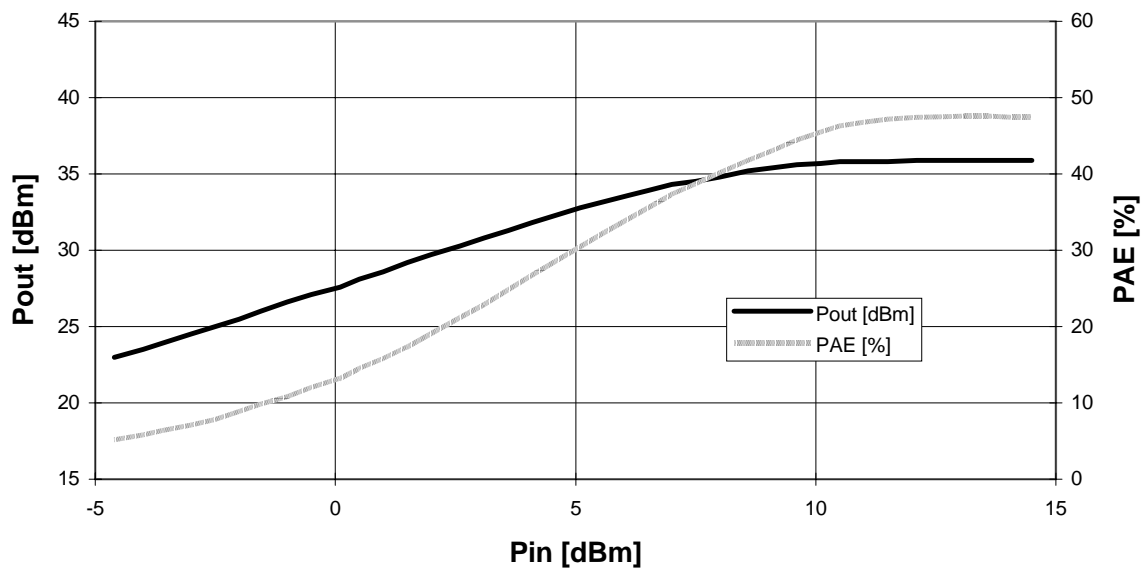
Pout and PAE vs. Pin

(VD=3V, VG=-4V, VTR=0V, f=900MHz, pulsed with a duty cycle of 10%, ton=0.33ms)



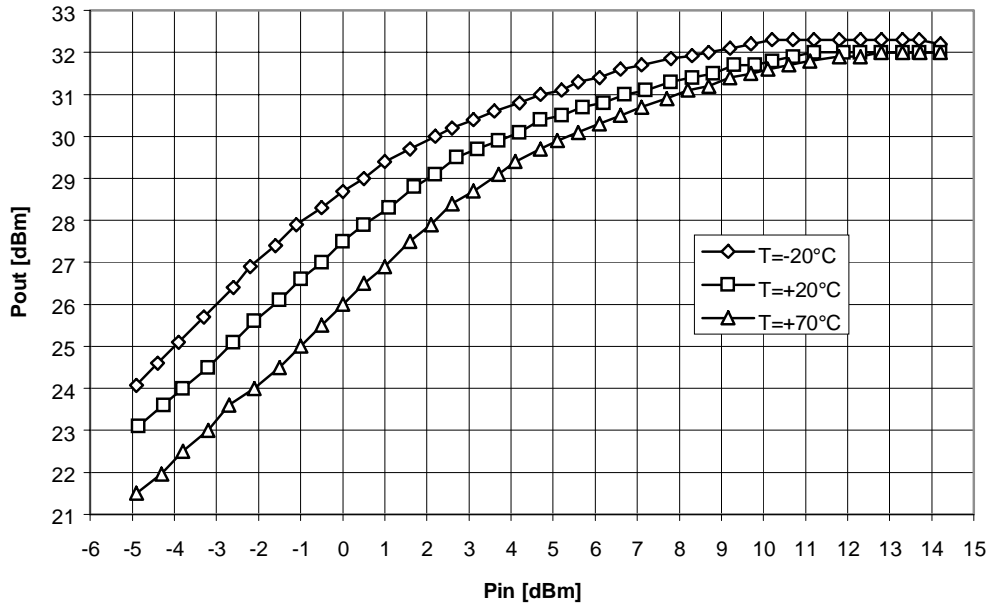
Pout and PAE vs. Pin

(VD=5V, VG=-4V, VTR=0V, f=900MHz, pulsed with a duty cycle of 10%, ton=0.33ms)



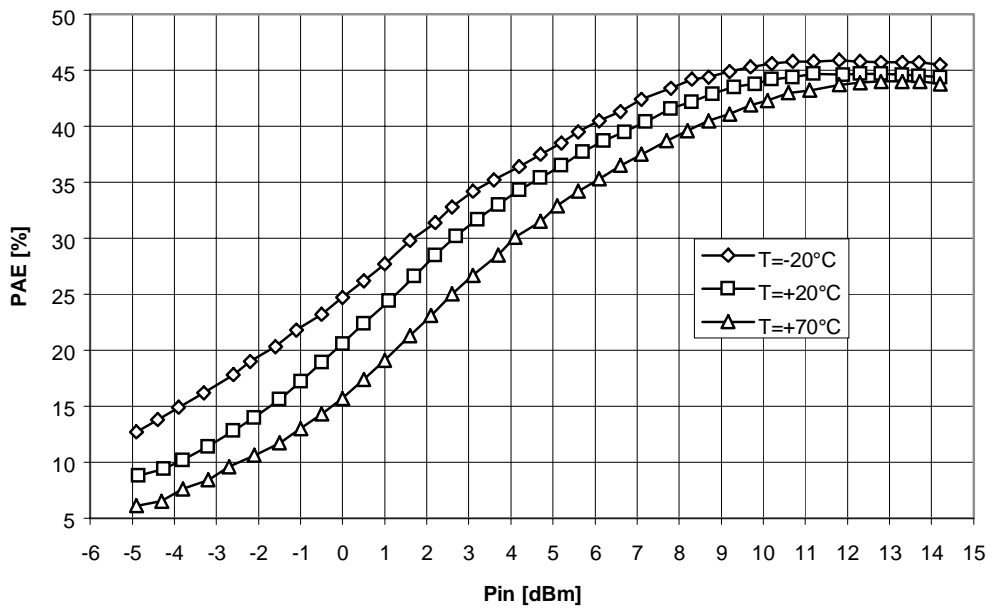
Output power at different temperatures

(VD=3V, VG=-4V, VTR=0V, f=900MHz, pulsed with a duty cycle of 10%, ton=0.33ms)



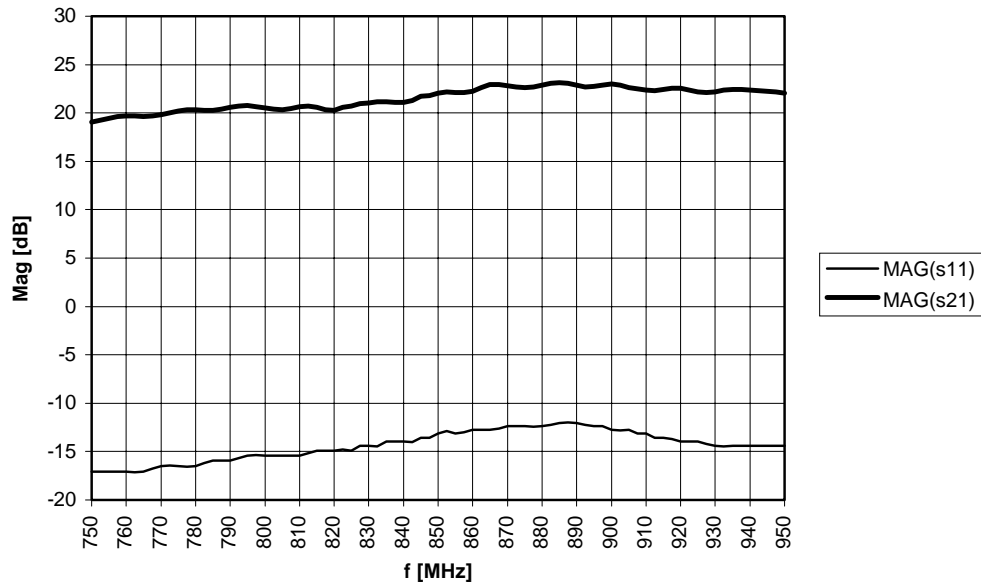
Power added efficiency at different temperatures

(VD=3V, VG=-4V, VTR=0V, f=900MHz, pulsed with a duty cycle of 10%, ton=0.33ms)



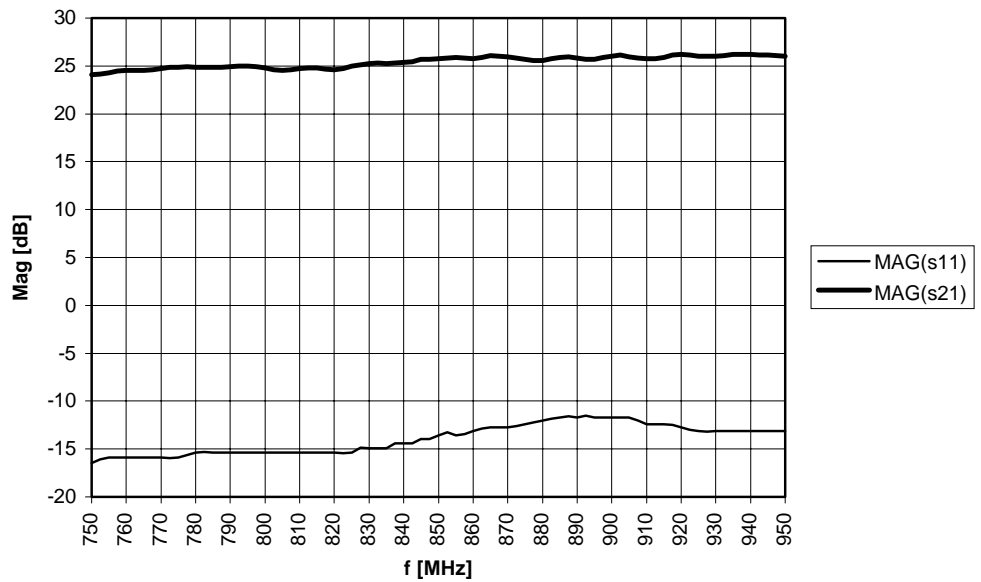
Measured S-parameter at VD=3V and Pin=9dBm

(VG=-4V, VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



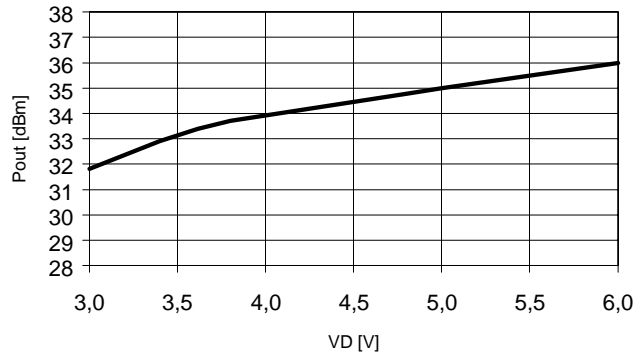
Measured S-parameter at VD=5V and Pin=9dBm

(VG=-4V, VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



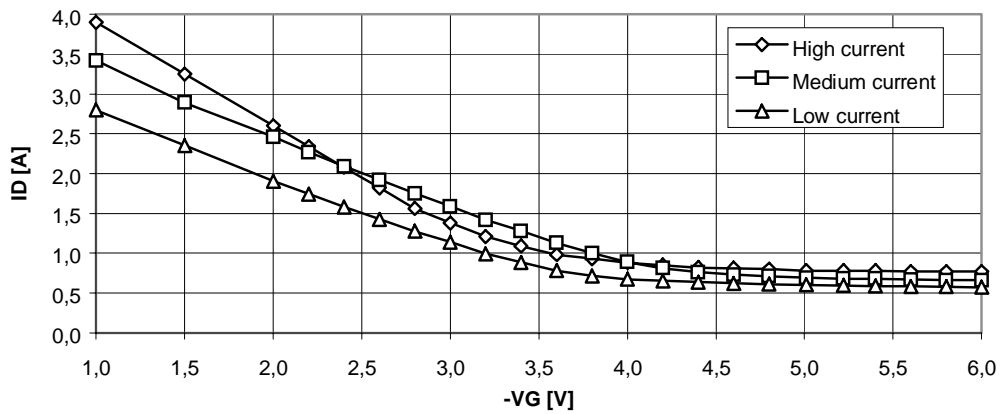
Output power vs. drain voltage

(Pin=10dBm, VG=-4V, VTR=0V, f=900MHz, pulsed with a duty cycle of 10%, ton=0.33ms)



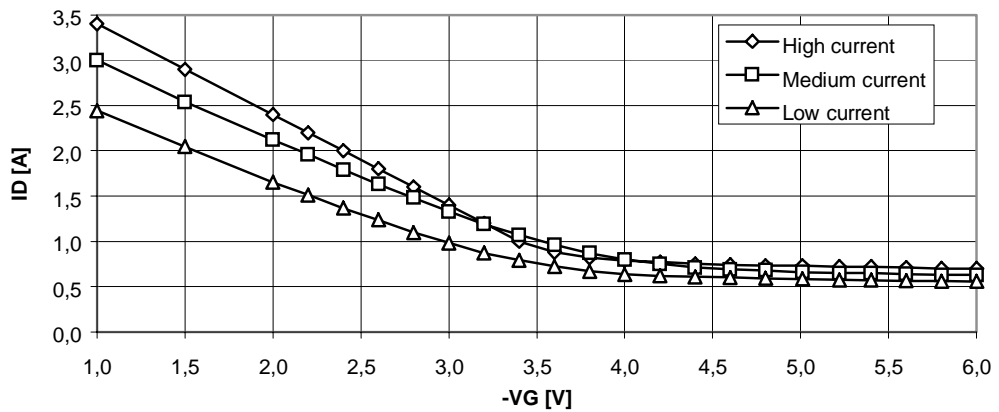
Performance of internal bias control circuit @VD=3V

(VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)

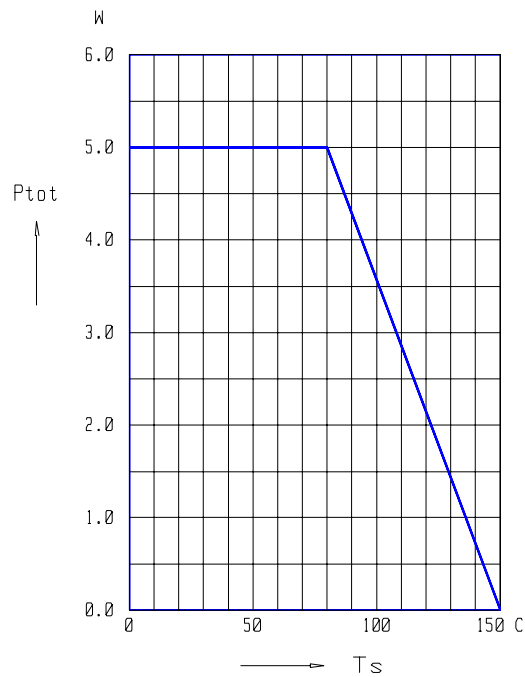


Performance of internal bias control circuit @VD=5V

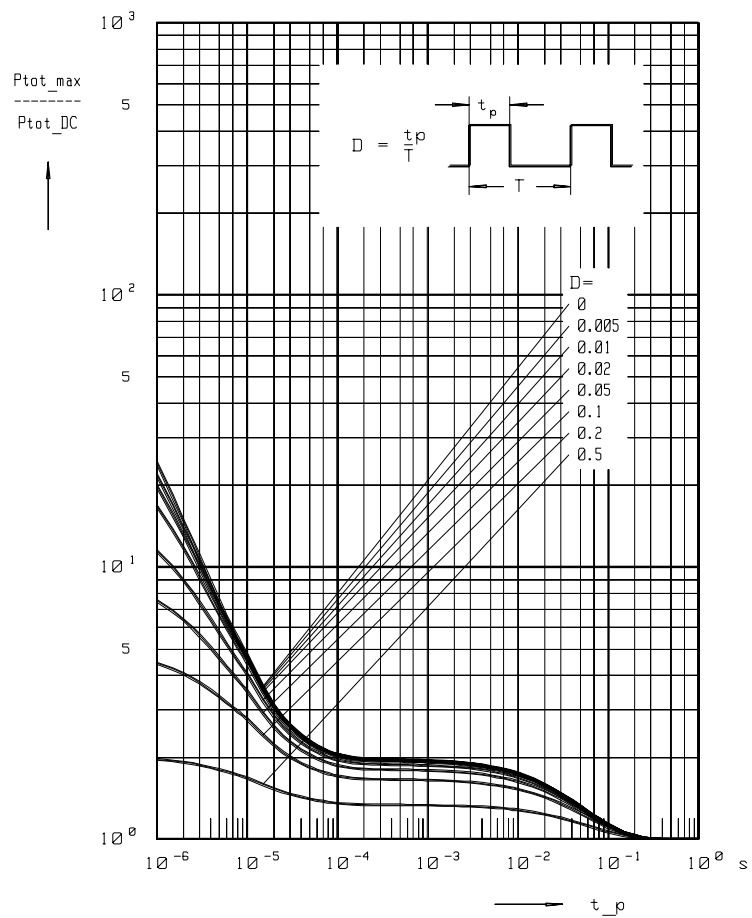
(VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



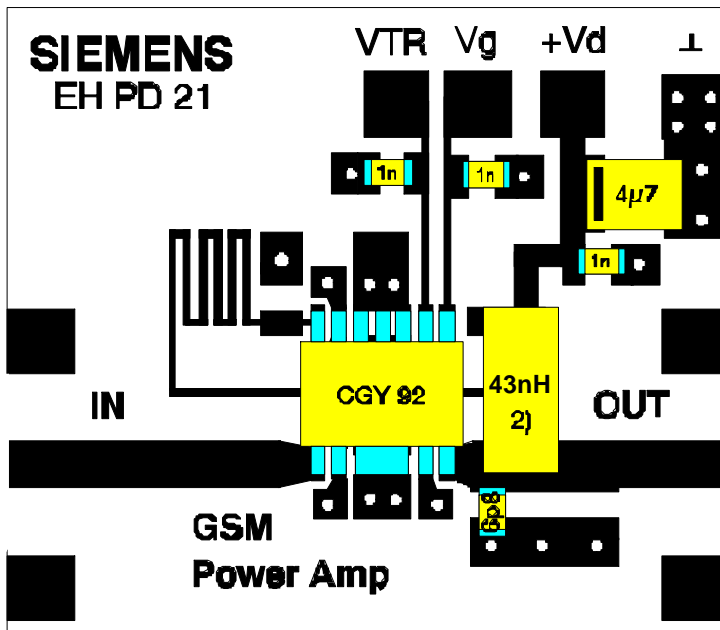
Total Power Dissipation $P_{tot}=f(T_s)$



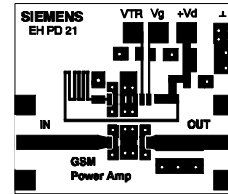
Permissible pulse load $P_{tot_max}/P_{tot_DC} = f(t_p)$



Test circuit board:



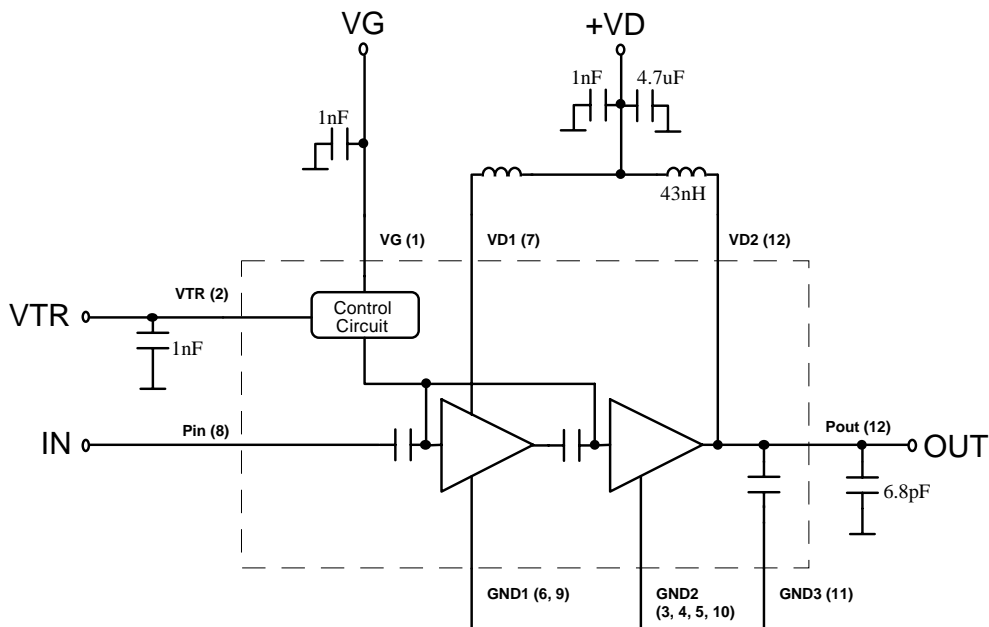
size: 30 x 26 mm



Note:

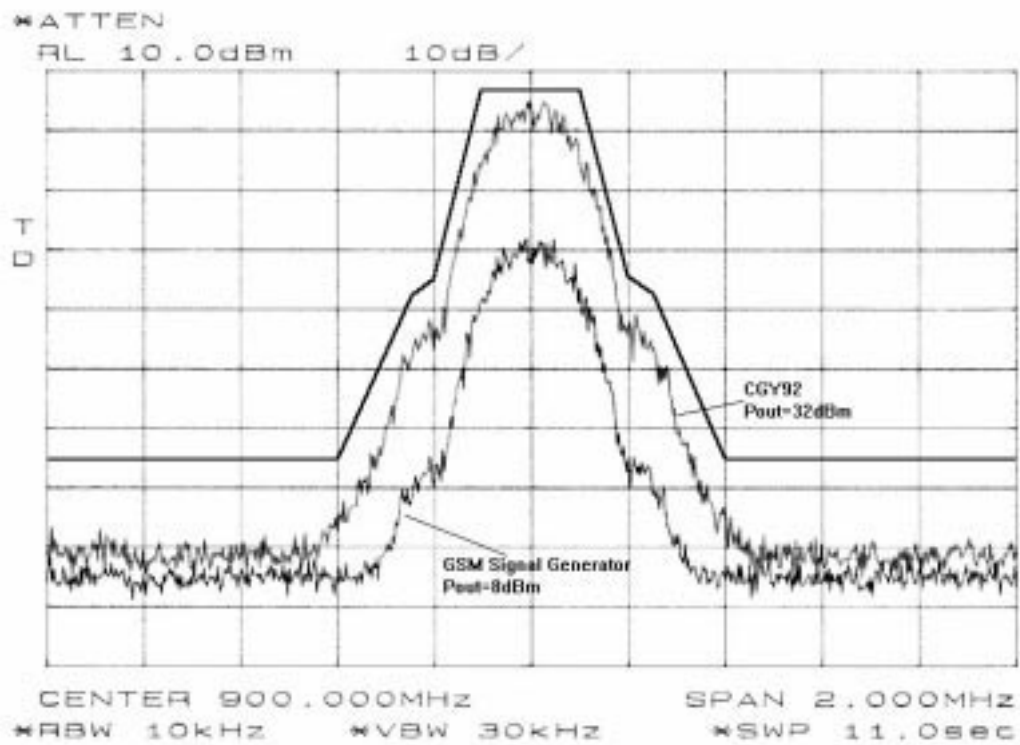
By changing the position of the 6.8 pF capacitor at pin # 12 it is possible to tune the board for max. Pout or max. PAE. To achieve the maximum output power place the capacitor close to the CGY92. For a better PAE increase the distance between the capacitor and the CGY92 device (2-5mm).

Principal circuit:

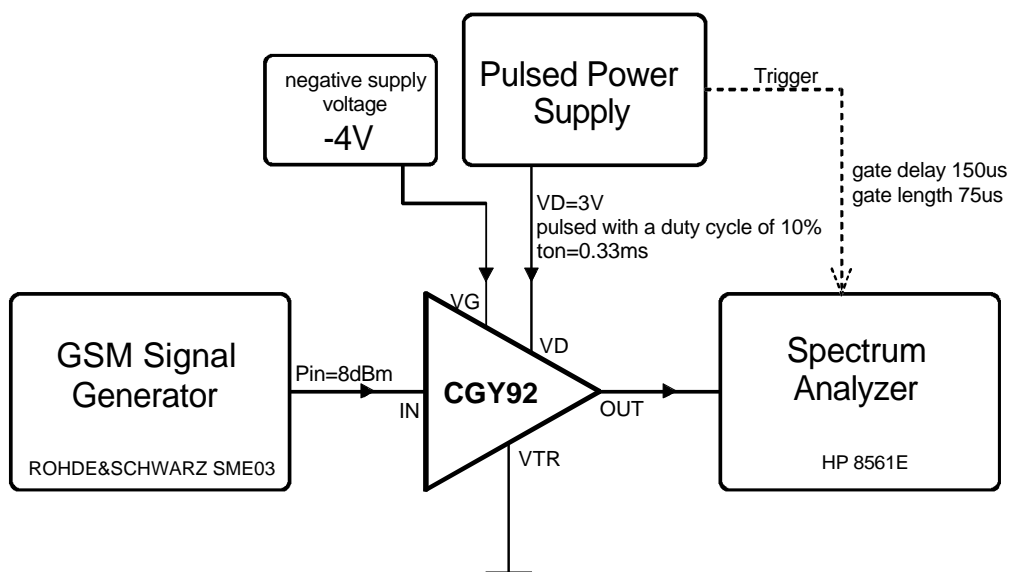


2) Coilcraft SMD Spring Inductor
distribution by Ginsbury Electronic GmbH, Am Moosfeld 85 D-81829 München, Tel. 089/45170-223

Emissions due to GMSK modulation:



Measurement was done with the following equipment:



APPLICATION - HINTS

1. CW - capability of the CGY92

Proving the possibility of CW - operation there must be known the total power dissipation of the device. This value can be found as a function of the temperature in the datasheet (page 10). The CGY92 has a maximum total power dissipation of $P_{tot} = 5 \text{ W}$.

As an example we take the operating point with a drain voltage $V_D = 3 \text{ V}$ and a typical drain current of $I_D = 1.0 \text{ A}$. So the maximum DC - power can be calculated to:

$$P_{DC} = V_D \cdot I_D = 3 \text{ W}$$

This value is smaller than 5 W and CW - operation is possible.

By decoupling RF power out of the CGY92 the power dissipation of the device can be further reduced. Assuming a power added efficiency (PAE) of 40 % the total power dissipation P_{tot} can be calculated using the following formula:

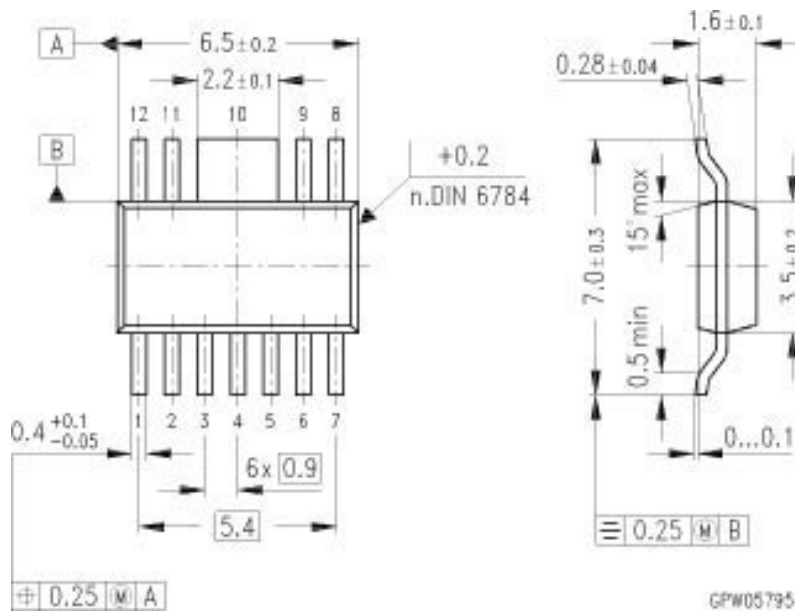
$$P_{tot} = P_{DC} (1 - PAE) = 3 \text{ W} (1 - 0.40) = 1.8 \text{ W}$$

2. Operation without using the internal current control

If you don't want to use the internal current control, it is recommended to connect the negative supply voltage at pin 1 (V_{TR}) instead of pin 2 (V_G). In that case V_G is not connected.

3. Biasing and use considerations

Biasing should be timed such that gate voltage (V_G) is always applied before the drain voltage (V_D), and when returning to the standby mode, gate voltage should only be removed once the drain voltage have been removed.



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