

SWITCHING
 P-CHANNEL POWER MOS FET

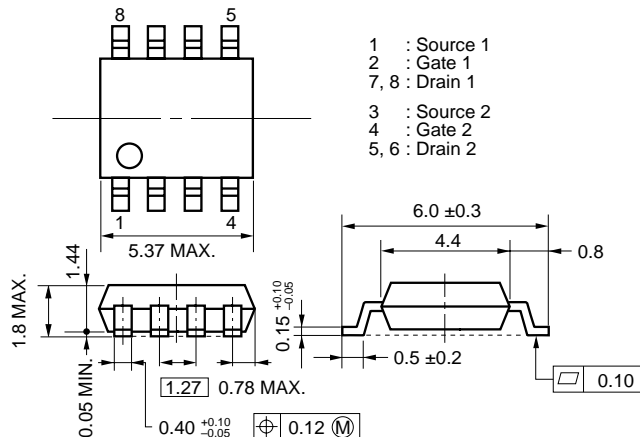
DESCRIPTION

The μ PA1772 is Dual P-Channel MOS Field Effect Transistor designed for power management applications of portable machines.

FEATURES

- Dual chip type
- Low on-state resistance
 $R_{DS(on)1} = 20.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -4 \text{ A)}$
 $R_{DS(on)2} = 29.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -4 \text{ A)}$
 $R_{DS(on)3} = 34.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -4 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1500 \text{ pF TYP. (} V_{DS} = -10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



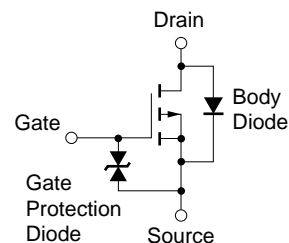
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1772G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC)	$I_{D(DC)}$	∓ 8	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 32	A
Total Power Dissipation (2 unit) ^{Note2}	P_T	2.0	W
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

EQUIVALENT CIRCUIT
 (1/2 circuit)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

2. $T_A = 25^\circ\text{C}$, Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 2.2 \text{ mm}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device..

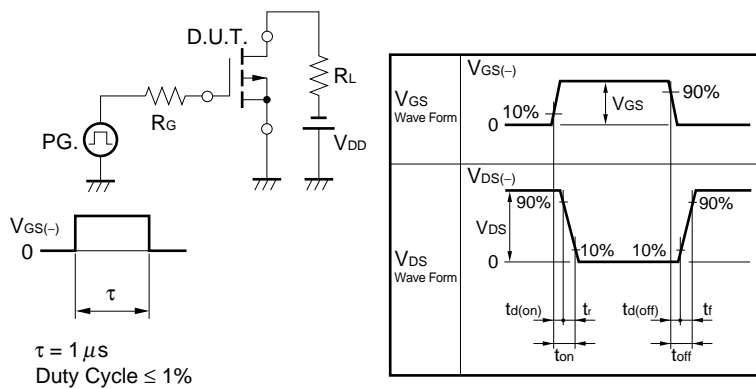
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

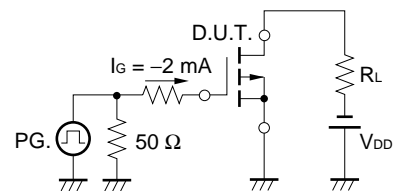
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			±10	μA
Gate Cut-off Voltage ^{Note}	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0	-1.7	-2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -4\text{ A}$	6	12		S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -4\text{ A}$		17.4	20.0	mΩ
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -4\text{ A}$		23.5	29.5	mΩ
	$R_{DS(on)3}$	$V_{GS} = -4.0\text{ V}, I_D = -4\text{ A}$		25.8	34.0	mΩ
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		1500		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		550		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		240		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, I_D = -4\text{ A}$		13		ns
Rise Time	t_r	$V_{GS} = -10\text{ V}$		11		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\text{ }\Omega$		120		ns
Fall Time	t_f			70		ns
Total Gate Charge	Q_G	$V_{DD} = -24\text{ V}$		34		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = -10\text{ V}$		5		nC
Gate to Drain Charge	Q_{GD}	$I_D = -8\text{ A}$		9		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 8\text{ A}, V_{GS} = 0\text{ V}$		0.84	1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 8\text{ A}, V_{GS} = 0\text{ V}$		50		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		37		nC

Note Pulsed: $PW \leq 350\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$

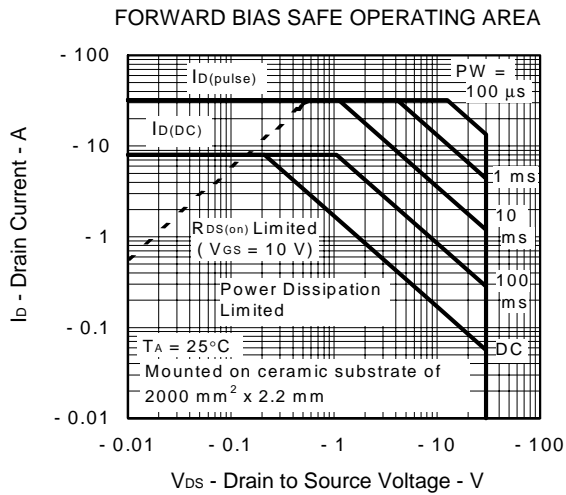
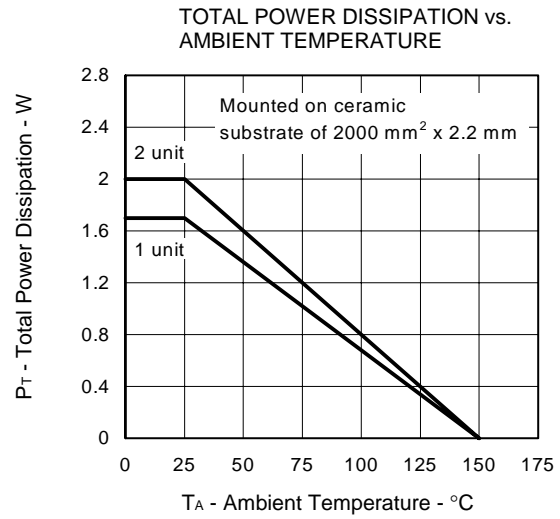
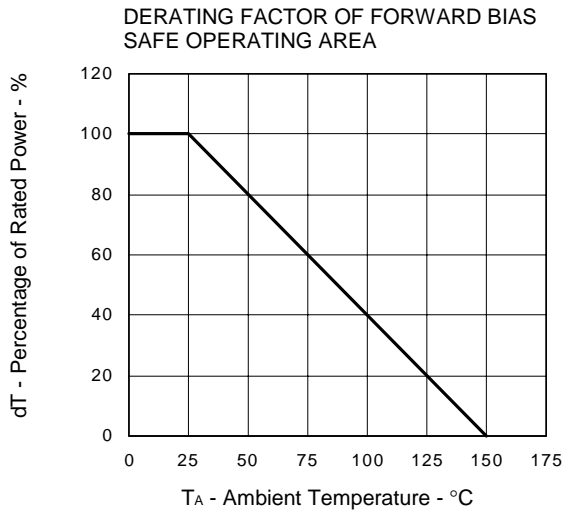
TEST CIRCUIT 1 SWITCHING TIME



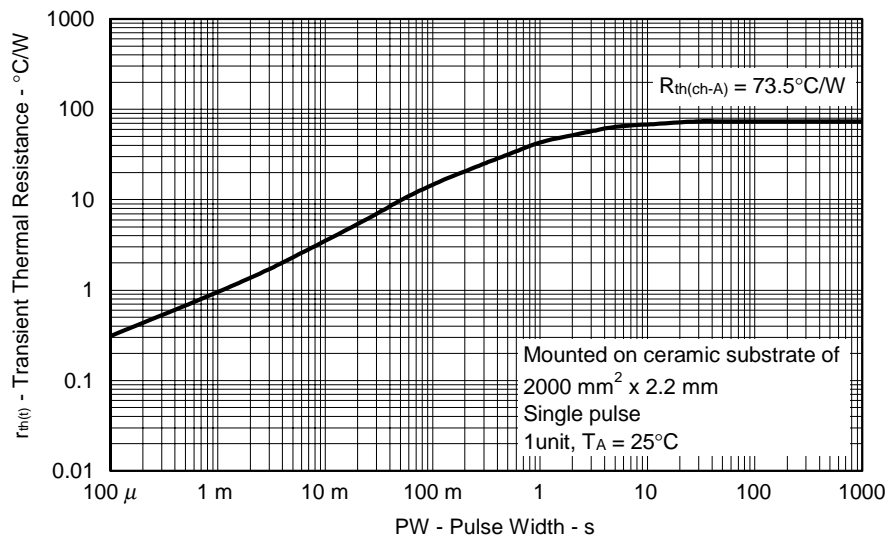
TEST CIRCUIT 2 GATE CHARGE



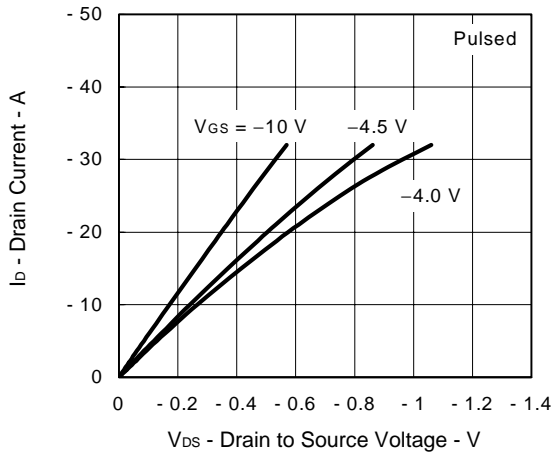
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



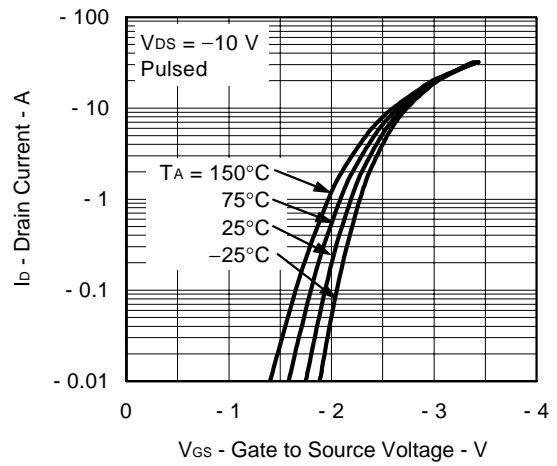
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



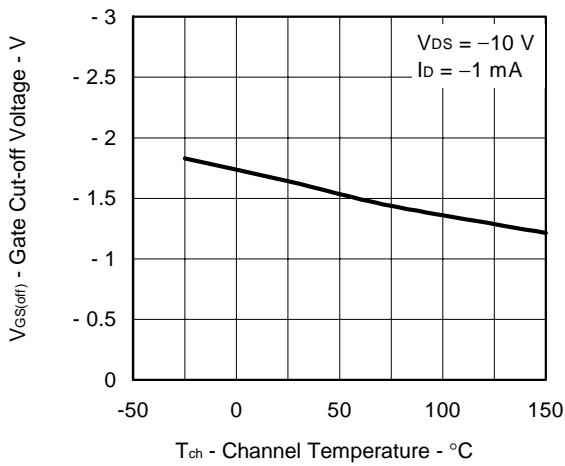
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



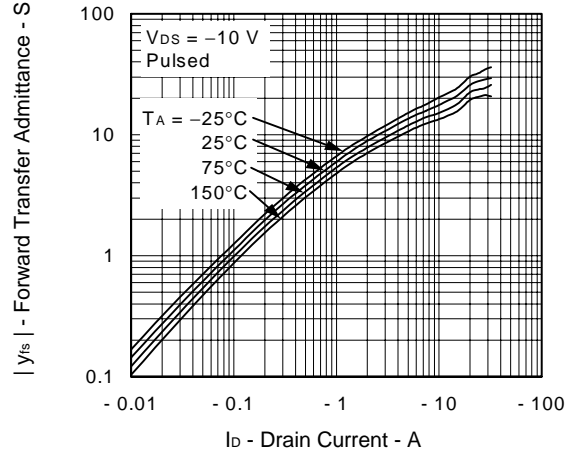
FORWARD TRANSFER CHARACTERISTICS



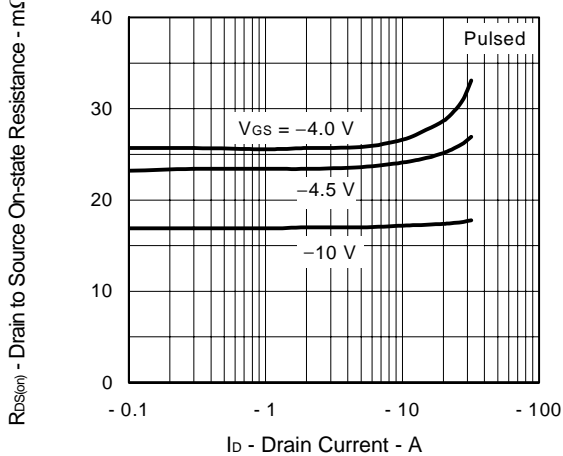
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



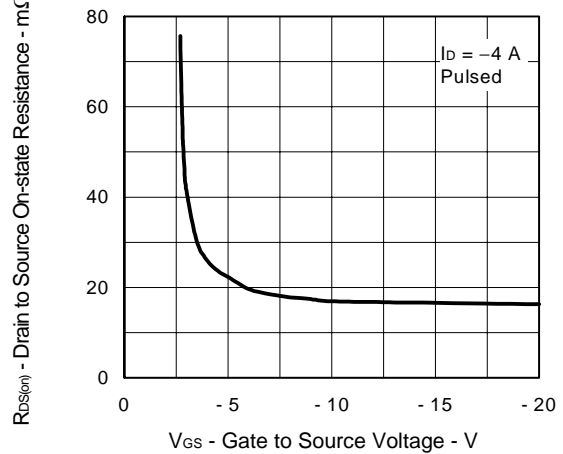
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



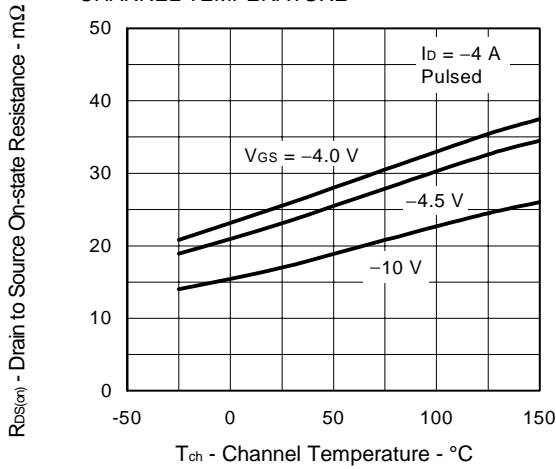
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



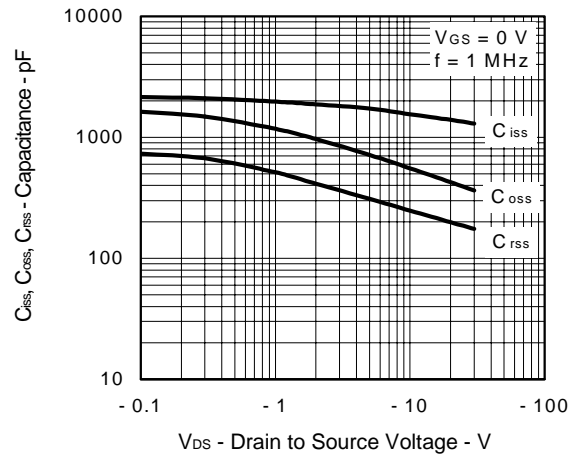
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



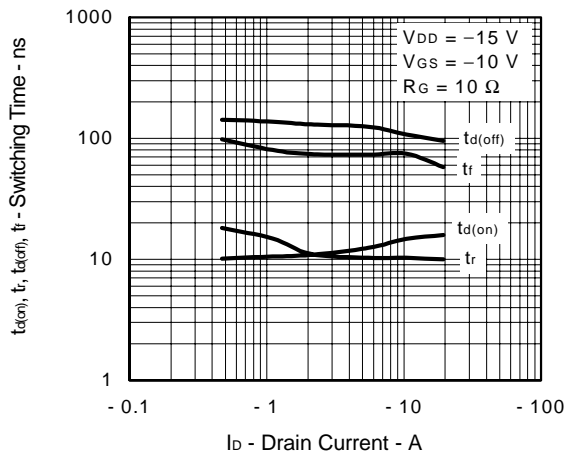
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



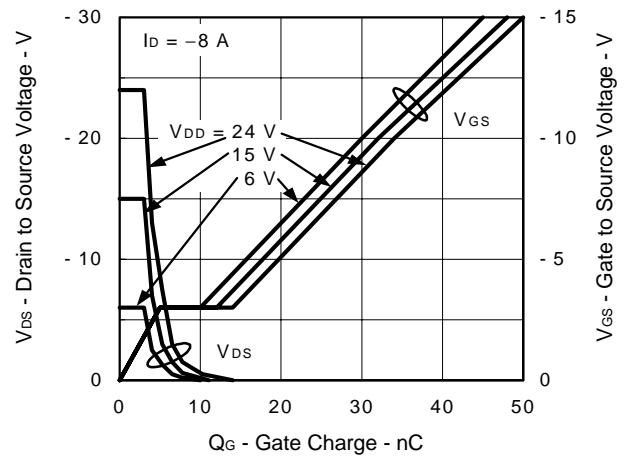
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



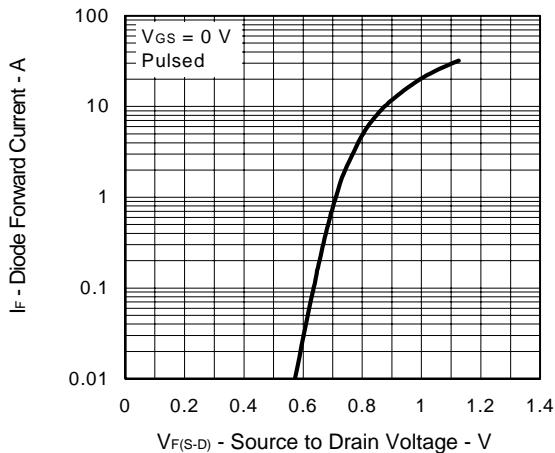
SWITCHING CHARACTERISTICS



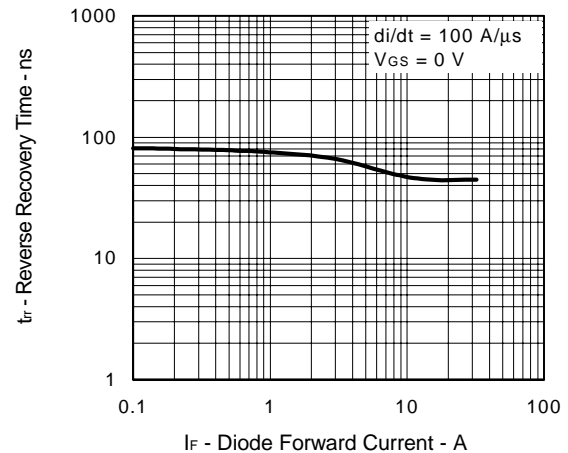
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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