# FEATURES

- Ÿ High-quality zoom and shrink scaling engine (Compatible with VGA thru XGA)
- Ÿ Integrated 8-bit triple-ADC/PLL
- Ÿ On-screen display controller (OSD)
- Ÿ Supports single-RGB inputs
- Ÿ Supports composite sync and SOG separator
- Ÿ Programmable 10-bit gamma correction
- Ÿ Integrated Brightness & Contrast control adjustment
- Ÿ Supports PWM backlit intensity control
- Ÿ Supports sRGB
- Ÿ Green PC and low EMI features
- Ÿ Built-in LVDS transmitter
- Ÿ Low standby power mode (< 15mA)

n High-Performance Scaling Engine
- Ÿ Programmable shrink/zoom capabilities
- Ÿ High-quality scaling for all VESA and IBM mode to fit screen
- Ÿ Variable sharpness control

n Analog RGB Compliant Input Port
- Ÿ Supports up to XGA at 85Hz
- Ÿ Supports Composite Sync and SOG (Sync-on-Green) separator

n Auto-Detection/Tune
- Ÿ Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE), and input mode (all VESA & IBM modes w/ resolution and polarity) detection
- Ÿ Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Ÿ Smart screen-fitting

n On-Screen OSD Controller
- Ÿ Built-in OSD generator with 256 character font programmable RAM
- Ÿ Supports for 4/8 multi-color fonts
- Ÿ Gradient color function
- Ÿ Supports button function
- Ÿ Pattern generator for production test
- Ÿ Support OSD MUX and alpha blending capability

n LVDS Display Interface
- Ÿ Supports Single Link up to 85MHz dot clock for XGA
- Ÿ Supports 2 data output formats: Thine & TI data mappings
- Ÿ Compatible with TIA/EIA
- Ÿ With 6/8 bits options
- Ÿ Reduced swing for LVDS for low EMI

n External Connection/Component
- Ÿ Built-in DDC circuit
- Ÿ Supports serial (up to 400Kbit/sec) bus type

BLOCK DIAGRAM
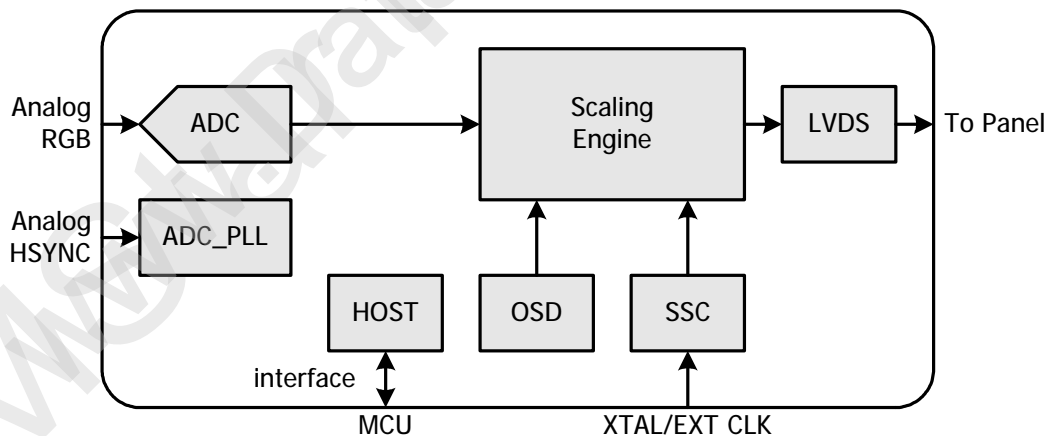
GENERAL DESCRIPTION

The MST8011A is a high performance, and fully integrated graphics processing IC solution for LCD monitors with resolutions up to XGA.   It is configured with an integrated triple-ADC/PLL, a high quality scaling engine, an on-screen display controller, a built-in output clock generator, and LVDS display interface.   To further reduce system costs, the MST8011A also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST8011A)

Pin 1

Top pins (left to right): 128 NC, 127 GNDP, 126 VDDP, 125 NC, 124 NC, 123 NC, 122 NC, 121 NC, 120 NC, 119 NC, 118 NC, 117 VDDC, 116 GNDC, 115 GNDP, 114 VDDP, 113 LVA0M, 112 LVA0P, 111 LVA1M, 110 LVA1P, 109 LVA2M, 108 LVA2P, 107 LVACKM, 106 LVACKP, 105 GNDP, 104 VDDP, 103 LVA3M

Left pins (top to bottom):
1 NC
2 AVSS_MPLL
3 BYPASS
4 NC
5 NC
6 NC
7 NC
8 NC
9 NC
10 GNDP
11 VDDP
12 NC
13 NC
14 NC
15 NC
16 NC
17 NC
18 VDDC
19 GNDC
20 GNDP
21 VDDP
22 NC
23 NC
24 NC
25 NC
26 NC
27 NC
28 DDC1_DAT
29 DDC1_CLK
30 DDCROM_CLK
31 DDCROM_DAT
32 HWRESET
33 XIN
34 XOUT
35 AVDD_MPLL
36 AVSS_MPLL
37 HSYNC0
38 VSYNC0

Center: MST8011A XXXXXXXXXX XXXXX

Right pins (top to bottom):
102 LVA3P
101 NC
100 NC
99 NC
98 NC
97 VDDC
96 GNDC
95 GNDP
94 VDDP
93 NC
92 NC
91 NC
90 NC
89 NC
88 NC
87 VDDC
86 GNDC
85 GNDP
84 VDDP
83 NC
82 NC
81 NC
80 NC
79 NC
78 NC
77 NC
76 NC
75 NC
74 PWM1
73 PWM0
72 INT
71 SCL
70 SDA
69 CS
68 AVSS
67 REFM
66 REFP
65 AVDD

Bottom pins (left to right): 39 AVSS, 40 NC, 41 NC, 42 AVSS, 43 NC, 44 NC, 45 AVDD, 46 NC, 47 NC, 48 AVSS, 49 NC, 50 NC, 51 AVDD, 52 REXT, 53 AVDD_PLL, 54 AVSS_PLL, 55 AVDD, 56 AVSS, 57 BIN0M, 58 BIN0, 59 GIN0M, 60 GIN0, 61 SOGIN0, 62 RIN0M, 63 RIN0, 64 AVSS

PIN DESCRIPTION

CPU Interface

Pin Name	Pin Type	Function	Pin
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware reset; active high	32
CS	Input w/ 5V-tolerant	3 Wire Serial Bus Chip Select; active high	69
SDA	I/O w/ 5V-tolerant	3 Wire Serial Bus Data; 4mA driving strength	70
SCL	Input w/ 5V-tolerant	3 Wire Serial Bus Clock	71
INT	Output	CPU interrupt; 4mA driving strength	72

Analog Interface

Pin Name	Pin Type	Function	Pin
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC input	37
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC input	38
REFP		Internal ADC top de-coupling pin	66
REFM		Internal ADC bottom de-coupling pin	67
RIN0	Analog Input	Analog red input	63
RIN0M	Analog Input	Reference ground for analog red input	62
SOGIN0	Analog Input	Sync-on-green input	61
GIN0	Analog Input	Analog green input	60
GIN0M	Analog Input	Reference ground for analog green input	59
BIN0	Analog Input	Analog blue input	58
BIN0M	Analog Input	Reference ground for analog blue input	57
REXT		External resistor 390 ohm to AVDD	52

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	Negative LVDS Differential Data Output	113
LVA0P	Output	Positive LVDS Differential Data Output	112
LVA1M	Output	Negative LVDS Differential Data Output	111
LVA1P	Output	Positive LVDS Differential Data Output	110
LVA2M	Output	Negative LVDS Differential Data Output	109
LVA2P	Output	Positive LVDS Differential Data Output	108
LVA3M	Output	Negative LVDS Differential Data Output	103
LVA3P	Output	Positive LVDS Differential Data Output	102
LVACKM	Output	Negative LVDS Differential Clock Output	107
LVACKP	Output	Positive LVDS Differential Clock Output	106

GPIO Interface

Pin Name	Pin Type	Function	Pin
GOUT1/PWM1	Output	GOUT1/PWM1; 4mA driving strength	74
GOUT0/PWM0	Output	GOUT0/PWM0; 4mA driving strength	73

Misc. Interface

Pin Name	Pin Type	Function	Pin
BYPASS		For External Bypass Capacitor	3
DDC1_DAT	I/O w/ 5V-tolerant	DDC Data for analog interface; 4mA driving strength	28
DDC1_CLK	Input w/ 5V-Tolerant	DDC Clock for analog interface	29
DDCROM_CLK	Input w/ 5V-Tolerant	DDC ROM Clock	30
DDCROM_DAT	I/O w/ 5V-tolerant	DDC ROM Data; 4mA driving strength	31
XIN	Crystal Oscillator Input	Xin	33
XOUT	Crystal Oscillator Output	Xout	34

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD	3.3V Power	ADC Power	45, 51, 55, 65
AVSS	Ground	ADC Ground	39, 42, 48, 56, 64, 68
AVDD_PLL	3.3V Power	PLL Power	53
AVSS_PLL	Ground	PLL Ground	54
AVDD_MPLL	3.3V Power	MPLL Power	35
AVSS_MPLL	Ground	MPLL Ground	2, 36
VDDP	3.3V Power	Digital Output Power	11, 21, 84, 94, 104, 114, 126
GNDP	Ground	Digital Output Ground	10, 20, 85, 95, 105, 115, 127
VDDC	2.5V Power	Digital Core Power	18, 87, 97, 117
GNDC	Ground	Digital Core Ground	19, 86, 96, 116

No Connects

Pin Name	Pin Type	Function	Pin
NC		No Connect. Leave These Pins Floating.	1, 4-9, 12-17, 22-27, 40, 41, 43, 44, 46, 47, 49, 50, 75-83, 88-93, 98-101, 118-125, 128

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
Resolution		8		Bits
DC ACCURACY				
Differential Nonlinearity		±0.5	+1.25/-1.0	LSB
Integral Nonlinearity		±1		LSB
No Missing Codes		Guaranteed		
ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			20	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	20		162.5	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		TBD		ps/$°$C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
Channel to Channel Matching		0.5%		Full-Scale

Specifications subject to change without notice.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	-0.3		3.6	V
2.5V Supply Voltages	V_{VDD_25}	-0.3		2.75	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$	-0.3		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}	-0.3		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Conversion	θ_{JA}		34		°C/W
Thermal Resistance (Junction to Case) Natural Conversion	θ_{JC}		6.0		°C/W

Note: Stress above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST8011A	0°C to +70°C	PQFP	128

MARKING INFORMATION

MST8011A

Part Number
Lot Number
Operation Code A
Operation Code B
Date Code (YYWW)

DISCLAIMER
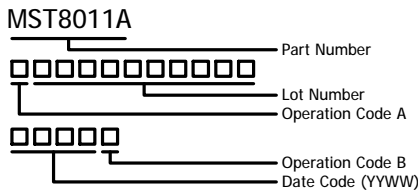
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST8011A comes with ESD protection circuitry, however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.
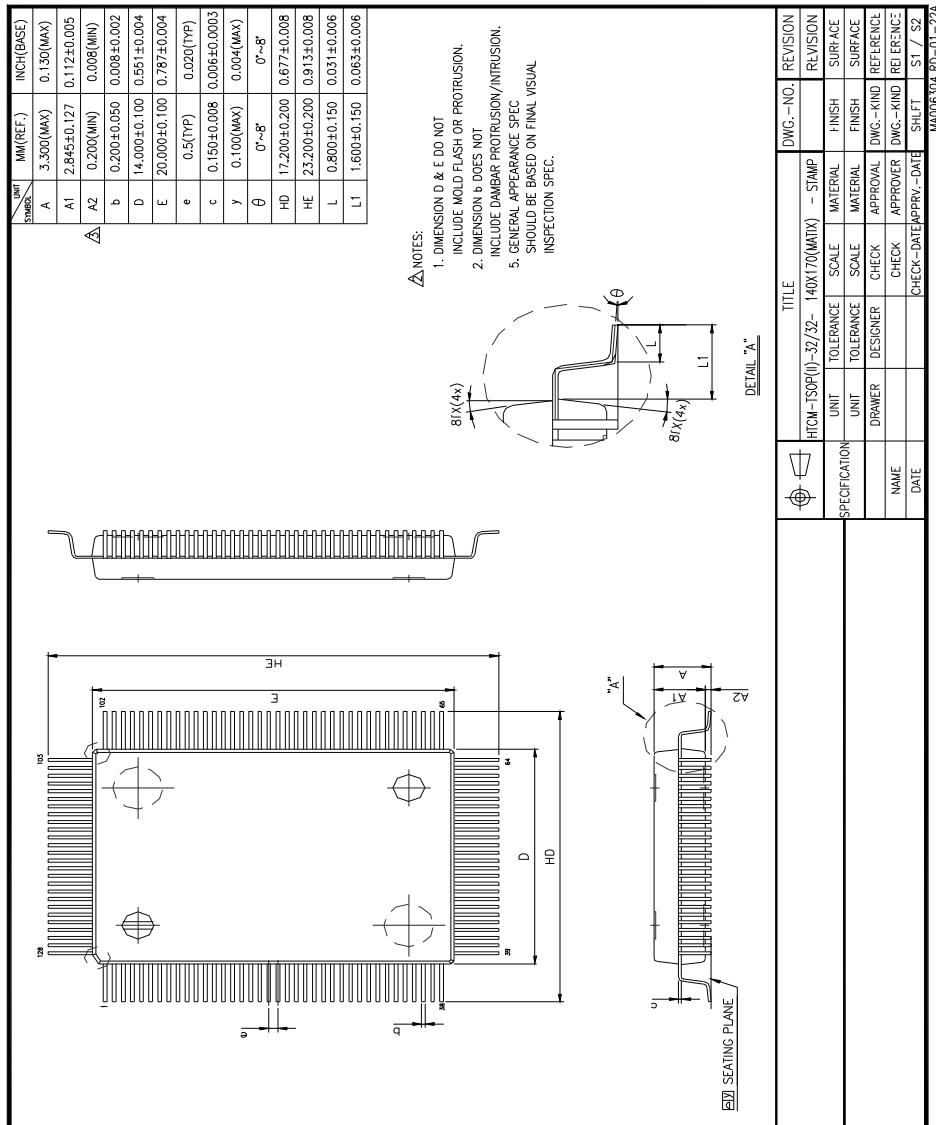
REVISION HISTORY

Document	Description	Date
MST8011A_data_sheet_v01	Ÿ Initial release	May 2003

MECHANICAL DIMENSIONS

UNIT SYMBOL	MM(REF.)	INCH(BASE)
A	3.300(MAX)	0.130(MAX)
A1	2.845±0.127	0.112±0.005
A2	0.200(MIN)	0.008(MIN)
b	0.200±0.050	0.008±0.002
D	14.000±0.100	0.551±0.004
E	20.000±0.100	0.787±0.004
e	0.5(TYP)	0.020(TYP)
c	0.150±0.008	0.006±0.0003
y	0.100(MAX)	0.004(MAX)
θ	0°~8°	0°~8°
HD	17.200±0.200	0.677±0.008
HE	23.200±0.200	0.913±0.008
L	0.800±0.150	0.031±0.006
L1	1.600±0.150	0.063±0.006

NOTES:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
5. GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

DETAIL "A"

TITLE: HTCM-TSOP(II)-32/32- 140X170(MATIX) - STAMP

SPECIFICATION	UNIT	TOLERANCE	SCALE	MATERIAL	FINISH	SURFACE	DWG.-NO.	REVISION
	UNIT	TOLERANCE	SCALE	MATERIAL	FINISH	SURFACE		REVISION
	DRAWER	DESIGNER	CHECK	APPROVAL	DWG.-KIND	REFERENCE		
NAME			CHECK	APPROVER	DWG.-KIND	REFERENCE		
DATE	CHECK-DATE	APPRV.-DATE				SHLFT S1 / S2		

MA006304 RD-01-22A

SEATING PLANE

REGISTER DESCRIPTION

General Control Register

Register Bank Select									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
00h	REGBK	PORR	-			AINC	BUST	REGBK[1:0]		R/W

- n PORR   Power On Reset Ready (read only)
  - Ÿ 0   Not ready
  - Ÿ 1   Ready
- n AINC   Serial bus address auto increase
  - Ÿ 0   Enable
  - Ÿ 1   Disable
- n BUST   BUS type (read only)
  - Ÿ 0   Direct bus
  - Ÿ 1   Serial bus
- n REGBK[1:0]   Register Bank Select
  - Ÿ 00   Register of Scalar
  - Ÿ 01   Register of Internal ADC/DVI Receiver
  - Ÿ 10   Register of Timing Controller
  - Ÿ 11   Reserved

ADC Register (Bank=01)

Double Buffer Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
01h	DBFC	-							DBVB	R/W

- n DBVB   Double buffer load at vertical blanking
  - Ÿ 0   Disable
  - Ÿ 1   Enable

PLL Divider Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
02h	PLLDIVM	PLLDIV[11:4]								R/W
03h	PLLDIVL	PLLDIV[3:0]				-				DB

- n PLLDIV[11:0]   PLL Divider Ratio
  - Ÿ 1685   Default value (1688 - 3)

Input Gain									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
04h	REDGAIN	REDGAIN[7:0]								R/W
05h	GRNGAIN	GRNGAIN[7:0]								R/W
06h	BLUGAIN	BLUGAIN[7:0]								R/W

- n REDGAIN[7:0]   Red channel gain adjust
  - Ÿ 80h   Default value
- n GRNGAIN[7:0]   Green channel gain adjust
  - Ÿ 80h   Default value
- n BLUGAIN[7:0]   Blue channel gain adjust
  - Ÿ 80h   Default value

Input Offset

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
07h	REDOFST	REDOFST[7:0]								R/W
08h	GRNOFST	GRNOFST[7:0]								R/W
09h	BLUOFST	BLUOFST[7:0]								R/W

- **n** REDOFST[7:0] Red channel offset adjust
  - Ÿ 80h Default value
- **n** GRNOFST[7:0] Green channel offset adjust
  - Ÿ 80h Default value
- **n** BLUOFST[7:0] Blue channel offset adjust
  - Ÿ 80h Default value

Clamp Timing

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Ah	CLPLACE	CLPLACE[7:0]								R/W
0Bh	CLDUR	CLDUR[7:0]								R/W

- **n** CLPLACE[7:0] Clamp Placement based on ADC clock
  - Ÿ 05h Default value
- **n** CLDUR[7:0] Clamp Duration based on ADC clock
  - Ÿ 05h Default value

General Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Ch	GCTRL	HSP	ECLK	HSLE	CLPE	CCDIS	WDIS	CSTP	DRBS	R/W

- **n** HSP Input HSYNC polarity
  - Ÿ 0 Active low
  - Ÿ 1 Active high
- **n** ECLK External Clock
  - Ÿ 0 ADC clock from internal ADC PLL
  - Ÿ 1 ADC clock from external clock
- **n** HSLE HS Lock Edge
  - Ÿ 0 Leading edge
  - Ÿ 1 Tailing edge
- **n** CLPE Clamp reference Edge
  - Ÿ 0 Tailing edge
  - Ÿ 1 Leading edge
- **n** CCDIS Disable Clamp during active coast
  - Ÿ 0 Always enable clamp
  - Ÿ 1 Disable clamp during active coast
- **n** WDIS Disable PLL watchdog timer
  - Ÿ 0 Enable PLL watchdog timer
  - Ÿ 1 Disable PLL watchdog timer
- **n** CSTP Coast polarity
  - Ÿ 0 Active low
  - Ÿ 1 Active high, default value
- **n** DRBS DVI input Red/Blue swap (DVI feature only)
  - Ÿ 0 Normal
  - Ÿ 1 Swap

PLL Coefficient

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Dh	BWCOEF	-	BWCOEF[5:0]							R/W
0Eh	FCOEF	-		FREQCOEF[4:0]						R/W
0Fh	DCOEF	-			DAMPCOEF[3:0]					R/W

n BWCOEF[5:0]   PLL Loop filter control
   Ÿ 2   Default value
n FREQCOEF[4:0]   PLL Loop filter control
   Ÿ 9   Default value
n DAMPCOEF[3:0]   PLL Loop filter control
   Ÿ 5   Default value

Clock Phase Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
10h	CLKCTRL1		STAT2	PHASE[5:0]						R/W
11h	CLKCTRL2	STAT[1:0]		PHASECC[5:0]						DB

n PHASE[5:0]   Clock phase adjust (should be always set to PHASECC + 8)
   Ÿ 08h   Default value
n PHASECC[5:0]   Clock phase adjust
   Ÿ 00h   Default value
n STAT[2:0]   Status select
   Ÿ 00h   Default value

VCO Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
12h	VCOCTRL	PDGT	DPL_S[2:0]			SETCNT[3:0]				R/W
13h	RT_CTL	SFTF	DEFE	WDF	RT_CTL[4:0]					R/W

Note: The default value is 0x15h

n PDGT   Phase digitize enable
   Ÿ 0
   Ÿ 1
n DPL_S[2:0]   VCO range
n SETCNT[3:0]   Settling time
n SFTF   DVI error correction enable (DVI feature only)
   Ÿ 0   Error correction disable
   Ÿ 1   Error correction enable
   Ÿ
n DEFE   DVI R/G/B alignment edge on DE (DVI feature only)
   Ÿ 0   DE rising edge
   Ÿ 1   DE falling edge
n WDF   DVI word alignment frozen (DVI feature only)
   Ÿ 0   Disable
   Ÿ 1   Enable
n RT_CTL[4:0]   Resister termination control for DVI (DVI feature only)

SOG/HSYNC Programming Level

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
14h	SOG_LVL	RMID	BMID	OFIR	SOG_LVL[4:0]					R/W
15h	HS_LVL	ADCBW[2:0]			CLPF	XSEL	HS_LVL[2:0]			R/W

n RMID   Middle clamp of Red Channel
   Ÿ 0   Disable

	Ÿ 1	Enable (used when YPbPr input)
n	BMID	Middle clamp of Blue Channel
	Ÿ 0	Disable
	Ÿ 1	Enable (used when YPbPr input)
n	OFIR	Output FIR
	Ÿ 0	Disable
	Ÿ 1	Enable (used when YPbPr input)
n	SOG_LVL[4:0]	SOG trigger level
n	ADCBW[2:0]	ADC bandwidth
	Ÿ 000	300MHz
	Ÿ 001	150MHz
	Ÿ 010	75MHz
	Ÿ 011	33MHz
	Ÿ 111	15MHz
n	CLPF	Clamp Filter
	Ÿ 0	Normal Clamp
	Ÿ 1	Lower current clamp
n	XSEL	XTAL Select
	Ÿ 0	Default XTAL
	Ÿ 1	Backup XTAL
n	HS_LVL[2:0]	HSYNC trigger level

Status

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
16h	STATUS1	LOCK	D7	D6	D5	D4	D3	D2	D1		RO
18h	STATUS5	RCMP[7:0]									RO
19h	STATUS4	PH_STAT[7:0]									RO
1Ah	STATUS5	PH_STAT[15:8]									RO

n	LOCK	PLL Lock Status
n	D7:D1	Status
n	RCMP[7:0]	DVI termination resistor status in 2's complement (DVI feature only)
	Ÿ	Positive value represents resistance value on low side, RT_CTL needs to adjust higher for compensation
	Ÿ	Negative value represents resistance value on high side, RT_CTL needs to adjust lower for compensation
n	PH_STAT[15:0]	DVI phase status indicator in 2's complement (DVI feature only)

DVI Override (DVI feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1Bh	DVI_PHR	OVPR	OVPHR[6:0]							R/W
1Ch	DVI_PHG	OVPG	OVPHG[6:0]							R/W
1Dh	DVI_PHB	OVPB	OVPHB[6:0]							R/W
1Eh	DVI_ERST	ERR_ST[7:0]								R/W
1Fh	DVI_ERTH	ERR_TH [7:0]								R/W

n	{OVPR,OVPHR}	Freeze & override DVI red channel PLL phase selection with OVPHR[6:0]
n	{OVPG,OVPHG}	Freeze & override DVI green channel PLL phase selection with OVPHG[6:0]
n	{OVPB,OVPHB}	Freeze & override DVI blue channel PLL phase selection with OVPHB[6:0]
n	ERR_ST	DVI bit error status indicator
n	ERR_TH	DVI bit error tolerance threshold

Test Mode									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
20h	TESTEN	TSTEN	-	ERRCHSEL[1:0]		ERRD	RDST	PHSEL[1:0]		R/W
26h	TESTA5	OVRD_ON		AMUX	DPLBG	DMIBEX	PHD	DMUX	DVIDET	R/W
27h	TESTA6	ADCR	ADCG	ADCB	DPL	AREF	-		VREF	R/W
2Dh	TESTMOD	TESTMOD[7:0]								R/W

n **TSTEN**   Enable test mode
  Ÿ 0   Disable
  Ÿ 1   Enable
n **ERRCHSEL[1:0]** Channel select for DVI error status indicator (DVI feature only)
  Ÿ 00   Red channel
  Ÿ 01   Green channel
  Ÿ 10   Blue channel
  Ÿ 11   Reserved
n **ERRD**   DVI bit error status indicator (ERR_ST) enable (DVI feature only)
  Ÿ 0   Normal
  Ÿ 1   Read status
n **RDST**   Terminator resistance status (RCMP) & DVI phase status enable (DVI feature only)
  Ÿ 0   Normal
  Ÿ 1   Read status
n **PHSEL[1:0]** Channel select for DVI phase status (DVI feature only)
  Ÿ 00   Red channel
  Ÿ 01   Green channel
  Ÿ 10   Blue channel
  Ÿ 11   Reserved
n **OVRD_ON**   Enable for power down overrides
  Ÿ 0   Auto select in operation mode
  Ÿ 1   Overriding enable
n **AMUX**   Analog mux override select
  Ÿ 0   Select ADC0
  Ÿ 1   Select ADC1
n **DPLBG**   Override value for DPL bandgap
  Ÿ 0   Bandgap on
  Ÿ 1   Bandgap off
n **DMIBEX**   Override value for output current bias
  Ÿ 0   Bias on
  Ÿ 1   Bias off
n **PHD**   Override value for phase digitizer
  Ÿ 0   Phase digitizer on
  Ÿ 1   Phase digitizer off
n **DMUX**   Override value for DVI de-multiplexer (DVI feature only)
  Ÿ 0   De-multiplexer on
  Ÿ 1   De-multiplexer off
n **DVIDET**   Override value for DVI clock detection (DVI feature only)
  Ÿ 0   Detection on
  Ÿ 1   Detection off
n **ADCR**   Power down ADC red channel
  Ÿ 0   ADC red channel on
  Ÿ 1   ADC red channel off
n **ADCG**   Power down ADC green channel
  Ÿ 0   ADC green channel on
  Ÿ 1   ADC green channel off
n **ADCB**   Power down ADC blue channel
  Ÿ 0   ADC blue channel on
  Ÿ 1   ADC blue channel off

n DPL   Power down DPL regulator
  Ÿ 0   DPL on
  Ÿ 1   DPL off
n AREF   Power down ADC voltage reference
  Ÿ 0   ADC voltage reference on
  Ÿ 1   ADC voltage reference off
n VREF   Power down HSYNC voltage reference
  Ÿ 0   HSYNC voltage reference on
  Ÿ 1   HSYNC voltage reference off
n TESTMOD[7]   LVDS/RSDS test mode
  Ÿ 0   Default
  Ÿ 1   Stop LVDS internal and output clock/stop RSDS-clock-side internal and output clock
n TESTMOD[4:0]   LVDS/RSDS differential output swing control
  Ÿ 5'b01000   5.0mA for LVDS/ 2.5mA for RSDS
  Ÿ 5'b00111   4.6mA for LVDS/ 2.3mA for RSDS
  Ÿ 5'b00110   4.2mA for LVDS/ 2.1mA for RSDS

PLL Control for Video input									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
30h	PLLCTRLV	PLLCTRLV[7:0]								R/W

n PLLCTRLV[7:0]   PLL Control for composite sync input
  Ÿ 0x95   Recommended value (power on default value is 0)

Scalar Register (Bank=00)

Double Buffer Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
01h	DBFC	-					DBL[1:0]		DBC	R/W

n DBL[1:0]   Double buffer load
  Ÿ 00   Keep old register value
  Ÿ 01   Load new data (auto reset to 00 when load finish)
  Ÿ 10   Automatically load data at VSYNC blanking
  Ÿ 11   Reserved
n DBC   Double buffer Control
  Ÿ 0   Double buffer disable
  Ÿ 1   Double buffer enable

Graphic Port Register (11, 02h - 0Ch)

Input Source Select/Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
02h	ISELECT	NIS	STYPE[1:0]		COMP	CSC	IHSU	ISEL[1:0]		R/W
04h	IPCTRL2	DHSR	DEON	IVSD	HSE	VSE	ESLS	VWRP	HWRP	R/W

n NIS   Output Lock mode
  Ÿ 0   Lock input (input signal exits)
  Ÿ 1   Free Run (no input signal)
n STYPE[1:0]   Input Sync Type
  Ÿ 00   Auto detected
  Ÿ 01   Input is separated HSYNC, VSYNC.
  Ÿ 10   Input is Composite sync
  Ÿ 11   Input is sync on green (SOG)
n COMP   CSYNC/SOG select (only useful when STYPE=00)
  Ÿ 0   CSYNC

    Ÿ 1   SOG

n CSC   **CSC function**
    Ÿ 0   Disable (RGB -> RGB)
    Ÿ 1   Enable (YCbCr -> RGB)

n IHSU   **Input HSYNC Usage**
Ÿ When ISEL=00 or 01
    Ÿ 0   Use HSYNC to do mode detection, HSOUT from ADC to sample pixel
    Ÿ 1   Use HSYNC only
Ÿ When ISEL=10
    Ÿ 0   Normal
    Ÿ 1   Enable DE Ahead/Delay adjust
Ÿ When ISEL=11
    Ÿ 0   Normal
    Ÿ 1   Output Black at blanking

n ISEL[1:0]   **Input Select**
    Ÿ 00   Analog 1
    Ÿ 01   Analog 2
    Ÿ 10   DVI
    Ÿ 11   Video

n DHSR   **Digital Input Horizontal Sample Range**
    Ÿ 0   Use DE as sample range, only V position can be adjusted
    Ÿ 1   Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted

n DEON   **DE Only, HSYNC and VSYNC is ignored**
    Ÿ 0   Disable
    Ÿ 1   Enable

n IVSD   **Input VSYNC Delay select**
    Ÿ 0   Delay 1/4 input HSYNC (recommended)
    Ÿ 1   No delay

n HSE   **Input HSYNC reference edge select**
    Ÿ 0   From HSYNC leading edge, default value
    Ÿ 1   From HSYNC tailing edge

n VSE   **Input VSYNC reference edge select**
    Ÿ 0   From VSYNC leading edge, default value
    Ÿ 1   From VSYNC tailing edge

n ESLS   **Early Sample Line Select**
    Ÿ 0   8 lines
    Ÿ 1   16 lines

n VWRP   **Input image Vertical wrap**
    Ÿ 0   Disable
    Ÿ 1   Enable

n HWRP   **Input image Horizontal wrap**
    Ÿ 0   Disable
    Ÿ 1   Enable

Input Image Sample Range

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
05h	SPRVST-L	SPRVST[7:0]								R/W
06h	SPRVST-H	-					SPRVST[10:8]			DB
07h	SPRHST-L	SPRHST[7:0]								R/W
08h	SPRHST-H	-					SPRHST[10:8]			DB
09h	SPRVDC-L	SPRVDC[7:0]								R/W
0Ah	SPRVDC-H	-					SPRVDC[10:8]			
0Bh	SPRHDC-L	SPRHDC[7:0]								R/W
0Ch	SPRHDC-H	-					SPRHDC[10:8]			

n SPRVST[10:0]   Image vertical sample start point, count by input HSYNC
n SPRHST[10:0]   Image horizontal sample start point, count by input dot clock
n SPRVDC[10:0]   Image vertical resolution (vertical display enable area count by line)
n SPRHDC[10:0]   Image horizontal resolution (horizontal display enable area count by pixel)

Input Lock Point									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Fh	LYL	-				LYL[3:0]				R/W

n LYL[3:0]   Lock Y Line

Display Timing Register (24, 10h - 27h)

Output DE Size									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
10h	DEVST-L	DEVST[7:0]								R/W
11h	DEVST-H	-					DEVST[10:8]			
12h	DEHST-L	DEHST[7:0]								R/W
13h	DEHST-H	-					DEHST[10:8]			
14h	DEVEND-L	DEVEND[7:0]								R/W
15h	DEVEND-H	-					DEVEND[10:8]			
16h	DEHEND-L	DEHEND[7:0]								R/W
17h	DEHEND-H	-					DEHEND[10:8]			

n DEVST[10:0]   Output DE Vertical Start
　Ÿ 00h   Default value
n DEHST[10:0]   Output DE horizontal Start
　Ÿ 48h   Recommended value (power on default value is 3)
n DEVEND[10:0]   Output DE Vertical END
　Ÿ 2FFh   Recommended value for XGA output (power on default value is 6)
　Ÿ 3FFh   Recommended value for SXGA output
n DEHEND[10:0]   Output DE Horizontal END
　Ÿ 447h   Recommended value for XGA output (power on default value is 0)
　Ÿ 547h   Recommended value for SXGA output

Scaling Image Window Size									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
18h	SIHST-L	SIHST[7:0]								R/W
19h	SIHST-H	-					SIHST[10:8]			
1Ah	SIVEND-L	SIVEND[7:0]								R/W
1Bh	SIVEND-H	-					SIVEND[10:8]			
1Ch	SIHEND-L	SIHEND[7:0]								R/W
1Dh	SIHEND-H	-					SIHEND[10:8]			

n SIHST[10:0]   Scaling Image window horizontal start
　Ÿ 48h   Recommended value (power on default value is 0)
n SIVEND[10:0]   Scaling Image window vertical END
　Ÿ 2FFh   Recommended value for XGA output (power on default value is 6)
　Ÿ 3FFh   Recommended value for SXGA output
n SIHEND[10:0]   Scaling Image window horizontal END
　Ÿ 447h   Recommended value for XGA output (power on default value is 0)
　Ÿ 547h   Recommended value for SXGA output

Output SYNC Timing

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1Eh	VDTOT-L	VDTOT[7:0]								R/W
1Fh	VDTOT-H	-					VDTOT[10:8]			
20h	VSST-L	VSST[7:0]								R/W
21h	VSST-H	-			VSRU	VSST[10:8]				
22h	VSEND-L	VSEND[7:0]								R/W
23h	VSEND-H	-					VSEND[10:8]			
24h	HDTOT-L	HDTOT[7:0]								R/W
25h	HDTOT-H	-					HDTOT[10:8]			DB
26h	HSEND	HSEND[7:0]								R/W

- **VDTOT[10:0]**   Output Vertical total
    - 326h   Recommended value for XGA output (power on default value is 3)
    - 42Ah   Recommended value for SXGA output
- **VSST[10:0]**   Output VSYNC start (only useful when AOVS=1)
    - 302h   Recommended value for XGA output (power on default value is 3)
    - 402h   Recommended value for SXGA output
- **VSEND[10:0]**   Output VSYNC end (only useful when AOVS=1)
    - 304h   Recommended value for XGA output (power on default value is 6)
    - 404h   Recommended value for SXGA output
- **VSRU**   VSYNC Register Usage
    - 0   Register 20h - 23h is used to define output VSYNC
    - 1   Register 20h and 21h is used to define No signal VSYNC
    -        Register 22h and 23h is used to define minimum H total
- **HDTOT[10:0]**   Output Horizontal total
    - 53fh   Recommended value for XGA output (power on default value is 3)
    - 697h   Recommended value for SXGA output
- **HSEND[7:0]**   Output HSYNC pulse width
    - 20h   Recommended value (power on default value is 0)

Output Sync Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
27h	OSCTRL1	AOVS	LCM	HSRM	VSGP	EHTT	MOD2	AHRT	CTRL	R/W
28h	OSCTRL2	-		ATEN2	-			SLE	CRM	R/W

- **AOVS**   Auto Output VSYNC
    - 0   OVSYNC is defined automatically
    - 1   OVSYNC is defined manually (register 0x20 – 0x23)
- **LOCK**   Lock mode
    - 0   Mode 0
    - 1   Mode 1
- **HSRM**   HSYNC Remove mode
    - 0   Normal
    - 1   Remove HSYNC when GPOA (Bank 2 register 0x62 – 0x6A) is low
- **VSGP**   VSYNC use GPO9
    - 0   Disable
    - 1   Enable (Using Bank 2 register 0x59 – 0x61 to define OVSYNC)
- **EHTT**   Even H TOTAL
    - 0   Enable, Output HTOTAL always be even pixels
    - 1   Disable, Output HTOTAL may be odd pixels
- **MOD2**   Mode 2
    - 0   Disable
    - 1   Enable
- **AHRT**   Auto H total and Read Start Tuning Enable

Ÿ 0   Disable
Ÿ 1   Enable
n   CTRL   ATCTRL function Enable
Ÿ 0   Disable
Ÿ 1   Enable
n   ATEN2   Lock Coarse Tune Type 2 Enable
Ÿ 0   Disable
Ÿ 1   Enable
n   SLE   Short Line Even Clock Mode
Ÿ 0   Even
Ÿ 1   Odd
n   CRM   Clock Reset Mode
Ÿ 0   Old (near DE)
Ÿ 1   New (move away from DE)

Display Port Register (26, 2Ah - 43h)

Brightness Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
2Ah	BRC	-							BRC	R/W
2Bh	BCR	BCR[7:0]								R/W
2Ch	BCG	BCG[7:0]								R/W
2Dh	BCB	BCB[7:0]								R/W

n   BRC   Brightness function, reference to register 2Bh, 2Ch, 2Eh
Ÿ 0   OFF
Ÿ 1   ON
n   BCR[7:0]   Brightness Coefficient - Red Color
Ÿ 00h   -128
Ÿ 80h   0, default value
Ÿ FFh   +127
n   BCG[7:0]   Brightness Coefficient - Green Color
Ÿ 00h   -128
Ÿ 80h   0, default value
Ÿ FFh   +127
n   BCB[7:0]   Brightness Coefficient - Blue Color
Ÿ 00h   -128
Ÿ 80h   0, default value
Ÿ FFh   +127

Contrast Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
2Eh	CNTR	-			CCLR	CCLG	CCLB	CNTT	CNTR	R/W
2Fh	CCR	CCR[7:0]								R/W
30h	CCG	CCG[7:0]								R/W
31h	CCB	CCB[7:0]								R/W

n   CCLR   Contrast Coefficient LSB- Red Color
n   CCLG   Contrast Coefficient LSB- Green Color
n   CCLB   Contrast Coefficient LSB- Blue Color
n   CNTT   Contrast Type select
Ÿ 0   Use 0 as center point
Ÿ 1   Use 128 as center point
n   CNTR   Contrast function
Ÿ 0   OFF
Ÿ 1   ON

n CCR[7:0]   Contrast Coefficient - Red Color
    Ÿ 00h   0.0000000
    Ÿ 80h   1.0000000, default value
    Ÿ FFh   1.1111111
n CCG[7:0]   Contrast Coefficient - Green Color
    Ÿ 00h   0.0000000
    Ÿ 80h   1.0000000, default value
    Ÿ FFh   1.1111111
n CCB[7:0]   Contrast Coefficient - Blue Color
    Ÿ 00h   0.0000000
    Ÿ 80h   1.0000000, default value
    Ÿ FFh   1.1111111

Border Color										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
32h	FWC	-							FWC	R/W
33h	FCR	FCR[7:0]								R/W
34h	FCG	FCG[7:0]								R/W
35h	FCB	FCB[7:0]								R/W

n FWC   Border color (will be used when output is free run mode)
    Ÿ 0   OFF
    Ÿ 1   ON
n FCR[7:0]   Border Color - Red channel
n FCG[7:0]   Border Color - Green channel
n FCB[7:0]   Border Color - Blue channel

Dither Control										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
36h	DITHCTRL	DITHG[1:0]		DITHB[1:0]		SROT	TROT	OBN	DITH	R/W
37h	DITHCOEF	TL[1:0]		TR[1:0]		BL[1:0]		BR[1:0]		R/W
38h	TRFN	-		DATP	DRT	DT3	DT2	DT1	TDFNC	R/W

Note: The default value of register 37h is 2Dh

n SROT   Spatial Coefficient Rotate
    Ÿ 0   Disable
    Ÿ 1   Enable
n TROT   Temporal Coefficient Rotate
    Ÿ 0   Disable
    Ÿ 1   Enable
n OBN   Output Bits Number (used for 10bits/8 bits gamma)
    Ÿ 0   8 bits output
    Ÿ 1   6 bits output (power on default value)
n DITH   Dither Function
    Ÿ 0   OFF
    Ÿ 1   ON
n DITHG[1:0]   Dither Coefficient for G Channel
n DITHB[1:0]   Dither Coefficient for B Channel
n TL[1:0]   Top - Left Dither Coefficient
n TR[1:0]   Top - Right Dither Coefficient
n BL[1:0]   Bottom - Left Dither Coefficient
n BR[1:0]   Bottom - Right Dither Coefficient
n DATP   Dither based on Auto Phase threshold
    Ÿ 0   Disable
    Ÿ 1   Enable
n DRT   Dither Rotate Type

- Ÿ 0   EOR
- Ÿ 1   Rotate
- **n DT3**   Dither Type 2 control
  - Ÿ 0   Disable dither type 2
  - Ÿ 1   Enable dither type 2
- **n DT2**   Dither Type 2
  - Ÿ 0   Output data bit 1 and 0 according to input pixel value
  - Ÿ 1   Output data bit 2, 1, and 0 according to input pixel value
- **n DT1**   Dither Type 1
  - Ÿ 0   Normal
  - Ÿ 1   Output data bit 1 and 0 are always 00
- **n TDFNC**   Tempo-Dither Frame Number Control
  - Ÿ 0   Tempo-dither every frame
  - Ÿ 1   Tempo-dither every 2 frames

Gamma Control										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
40h	GAMMAC	-				GTCS[1:0]		GTIO	GCFE	R/W
41h	GAMMAP	GAMMAP[7:0]								R/W

- **n GTCS**   Gamma Table Channel Select
  - Ÿ 00   Write Red Channel
  - Ÿ 01   Write Green Channel
  - Ÿ 10   Write Blue Channel
  - Ÿ 11   Write Red/Green/Blue Channel
- **n GTIO**   Gamma Table I/O Access
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n GCFE**   Gamma correction function enable
  - Ÿ 0   OFF
  - Ÿ 1   ON
- **n GAMMAP[7:0]**   Gamma Data Port

Output Control										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
42h	OCTRL1	LCPS	LCS	MLXT	LTIM	OMLX	EMLX	ORBX	ERBX	R/W
43h	OCTRL2	TCOP	DOT	WHTS	BLKS	REV	STO	DPX	DPO	R/W
44h	OCTRL3	-		CKSEL[4:0]						R/W

- **n LCPS**   LVDS Channel Polarity Swap (P/N swap)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n LCS**   LVDS Channel Swap (0/1 swap, 2/5 swap)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n MLXT**   MSB/LSB Exchange Type
  - Ÿ 0   Always reverse bit [7:0]
  - Ÿ 1   Reverse bit [7:2] when 6 bits panel
- **n LTIM**   LVDS TI Mode
  - Ÿ 0   Normal
  - Ÿ 1   TI Mode
- **n OMLX**   Odd channel MSB/LSB Exchange
  - Ÿ 0   Normal
  - Ÿ 1   Exchange
- **n EMLX**   Even channel MSB/LSB Exchange

- Ÿ 0   Normal
- Ÿ 1   Exchange
- **n ORBX**   Odd channel Red/Blue bus Exchange
  - Ÿ 0   Normal
  - Ÿ 1   Exchange
- **n ERBX**   Even channel Red/Blue bus Exchange
  - Ÿ 0   Normal
  - Ÿ 1   Exchange
- **n TCOP**   TCON control pin port select (only used when OBN=1, 6 bits output)
  - Ÿ 0   Use output data port
  - Ÿ 1   Use video in port
- **n DOT**   Differential Output Type
  - Ÿ 0   LVDS/RSDS
  - Ÿ 1   Reduced-swing LVDS/increased-swing RSDS
- **n WHTS**   White Screen (screen Off)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n BLKS**   Black Screen (screen Off)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n REV**   Reverse luminosity
  - Ÿ 0   OFF
  - Ÿ 1   ON
- **n STO**   Stagger output (only used when DPO=1)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n DPX**   Dual pixel exchange (only used when DPO=1)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n DPO**   Dual pixel output
  - Ÿ 0   Single pixel
  - Ÿ 1   Dual pixel
- **n CKSEL[4:0]**   Enable clock of internal control
  - Ÿ   Supposes input interface (ADC/DVI) as the left-side
  - Ÿ CKSEL[4]   Enable clock of down-side GPO
  - Ÿ CKSEL[3]   Enable clock of up-side channel
  - Ÿ CKSEL[2]   Enable clock of down-side channel
  - Ÿ CKSEL[1]   Enable clock of right-side GPO
  - Ÿ CKSEL[0]   Enable clock and output current of right-side channel
  - Ÿ   Please use ADC bank register 0x2D bit 7 to control LVDS internal clock
  - Ÿ 01h   LVDS output
  - Ÿ 1Dh   Dual-Link RSDS output with down-side GPO
  - Ÿ 0Fh   Dual-Link RSDS output with right-side GPO
  - Ÿ 15h   Single-Link RSDS output with down-side GPO
  - Ÿ 07h   Single-Link RSDS output with right-side GPO
  - Ÿ 00h   TTL output

OSD Overlay Registers (7, 46h - 4Ch)

OSD Alpha Blending Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
4Bh	BLENDC	-	CKIND[3:0]				ABM[2:0]			R/W
4Ch	BLENDL	-		NBM	-		BLENDL[2:0]			R/W

Ÿ When OSD register 0x10[7]=1, OSD is not backward compatible

n CKIND[3:0]   Color Index of Color Key

- Ÿ 0000   Color Index 0
- Ÿ 0001   Color Index 1
- Ÿ ...   ...
- Ÿ 1111   Color Index 15
- Ÿ When OSD register 0x10[7]=0, OSD is backward compatible

n CKIND[3]   **Reserved**

n ABM[2:0]   **Alpha Blending Mode**
- Ÿ 000   No alpha blending
- Ÿ 001   Background alpha blending
- Ÿ 010   Foreground alpha blending
- Ÿ 011   Color key alpha blending
- Ÿ 100   Not Color key alpha blending
- Ÿ 101   Entire OSD alpha blending
- Ÿ 11x   Reserved

n NBM   **New Blending Level**
- Ÿ 0   Original blending Level (BLENDL=000 means 0% transparency)
- Ÿ 1   New Blending Level (BLENDL=000 means 12.5% transparency)

n BLENDL[2:0]   **OSD alpha blending level**
- Ÿ 000   12.5% transparency.
- Ÿ 001   25.0% transparency.
- Ÿ 010   37.5% transparency.
- Ÿ 011   50.0% transparency.
- Ÿ 100   62.5% transparency.
- Ÿ 101   75.0% transparency.
- Ÿ 110   87.5% transparency.
- Ÿ 111   100% transparency.

Scaling Function Registers (28, 50h - 6Bh)

Scaling Ratio									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
50h	SRH-L	SRH[7:0]								R/W
51h	SRH-M	SRH[15:8]								R/W
52h	SRH-H	SENH	HFMD	SRH[21:16]						R/W
53h	SRV-L	SRV[7:0]								R/W
54h	SRVH-M	SRV[15:8]								R/W
55h	SRV-H	SENV	VFMD	SRV[21:16]						R/W

n SENH   **Horizontal Scaling Enable**
- Ÿ 0   Disable
- Ÿ 1   Enable

n HFMD   **Horizontal Scaling Factor Mode**
- Ÿ 0   N-1/M-1 for Horizontal Scaling Factor
- Ÿ 1   N/M for Horizontal Scaling Factor

n SRH[21:0]   **Horizontal Scaling Ratio (2 bits integer, 20 bits fraction) for scaling down to 1/3.9999**
- Ÿ   xx.xxxxxxxxxxxxxxxxxxxx

n SENV   **Vertical Scaling Enable**
- Ÿ 0   Disable
- Ÿ 1   Enable

n VFMD   **Vertical Scaling Factor Mode**
- Ÿ 0   N-1 / M-1 for Vertical Scaling Factor
- Ÿ 1   N / M for Vertical Scaling Factor

n SRV[21:0]   **Vertical Scaling Ratio (2 bits integer, 20 bits fraction) for scaling down to 1/2.9999**
- Ÿ   xx.xxxxxxxxxxxxxxxxxxxx

Scaling Filter Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
56h	SFH	SFH[7:0]								R/W
57h	SFV	SFV[7:0]								R/W
58h	HDSUSG	HDSUSG[7:0]								R/W
59h	HDSUSL	-		GSR	TSR	TXTJL[3:0]				R/W
5Ah	VDSUSG	VDSUSG[7:0]								R/W
5Bh	VDSUSL	MCKS	IOCK	GSE	TSE	DSUSL[3:0]				R/W

- n SFH[7:0]   Horizontal Scaling filter
- n SFV[7:0]   Vertical Scaling filter
- n HDSUSG[7:0]   Horizontal DSUS Scaling Parameter
- n GSR   Gray Scale Sensitive Register IO
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n TSR   Text Sensitive Register IO
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n TXTJL[3:0]   Text Judge Level
- n VDSUSG[7:0]   Vertical DSUS Scaling Parameter
- n DSUSL[3:0]   DSUS Scaling Parameter Level
- n MCKS   Manual clock select
  - Ÿ 0   Auto Select
  - Ÿ 1   Manual select
- n IOCK   Input/ FIX clock select (when MCKS=1)
  - Ÿ 0   FIXCLK faster, FIXCLK defined by Reg D1h bit7
  - Ÿ 1   IDCLK faster
- n GSE   Gray Scale Sensitive Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n TSE   Text Sensitive Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable

Post Filter

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
5Ch	PFEN							PFEN		R/W
5Dh	PFCOEF	PFCOEF-H				PFCOEF-L				R/W

- n PFEN   Post Filter Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n PFCOEF-H[3:0]   Post Filter H Coefficient for edge part
  - Ÿ 0000   Blur
  - Ÿ ...   ...
  - Ÿ 1000   No action
  - Ÿ ...   ...
  - Ÿ 1111   Sharp
- n PFCOEF-L[3:0]   Post Filter L Coefficient for no edge part
  - Ÿ 0000   Blur
  - Ÿ ...   ...
  - Ÿ 1000   No action
  - Ÿ ...   ...
  - Ÿ 1111   Sharp

Filter Coefficient

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
65h	FTAPEN				sRGBP	sRGBG	TPP	FFSEL[1:0]		R/W
66h	SRGB12	SRGB12 [7:0]								R/W
67h	SRGB13	SRGB13 [7:0]								R/W
68h	SRGB21	SRGB21 [7:0]								R/W
69h	SRGB23	SRGB23 [7:0]								R/W
6Ah	SRGB31	SRGB31 [7:0]								R/W
6Bh	SRGB32	SRGB32 [7:0]								R/W

- **n sRGBP**   sRGB Precision
  - Ÿ 0   Normal
  - Ÿ 1   Shift 2 bits
- **n sRGBG**   sRGB go through Gamma
  - Ÿ 0   Bypass Gamma
  - Ÿ 1   Go to Gamma
- **n TPP**   Test Pattern Position
  - Ÿ 0   After sRGB
  - Ÿ 1   Before sRGB
- **n FFSEL[1:0]**   Filter Function Select
  - Ÿ 00   Disable
  - Ÿ 01   Enable 3 tap function
  - Ÿ 1x   Enable sRGB Function
- **n SRGB12[7:0]**   Coefficient 12, 1 sign bit, 7 bits
- **n ...**   ...
- **n SRGB32[7:0]**   Coefficient 32, 1 sign bit, 7 bits

Interlaced Mode Line Shift

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
6Fh	INTMDS	-			ILIM	ODDF	SLN[2:0]			R/W

- **n ILIM**   Insert line when interlace mode
  - Ÿ 0   Don't insert
  - Ÿ 1   Insert
- **n ODDF**   Shift Odd Field
  - Ÿ 0   Shift Even Field
  - Ÿ 1   Shift Odd Field
- **n SLN[2:0]**   Shift Line Numbers
  - Ÿ 000   Shift 0 line between odd and even field
  - Ÿ 001   Shift 1 line between odd and even field
  - Ÿ 010   Shift 2 line between odd and even field
  - Ÿ 011   Shift 3 line between odd and even field
  - Ÿ 1xx   Shift 4 line between odd and even field

Auto Adjustment Registers (36, 70h - 93h)

Auto Gain Function Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
78h	ATGCTRL	MAXR	MAXG	MAXB	ACE	AGR	ATGM	ATGR	ATGE	R/W

- **n MAXR**   Max value flag for red channel (read only)
  - Ÿ 0   Normal
  - Ÿ 1   Have max value (255) when AGR=0
  - Ÿ   Output over max value (255) when AGR=1
- **n MAXG**   Max value flag for green channel (read only)

- Ÿ 0   Normal
- Ÿ 1   Have max value(255) when AGR=0
- Ÿ   Output over max value (255) when AGR=1

n MAXB   Max value flag for blue channel (read only)
- Ÿ 0   Normal
- Ÿ 1   Have max value(255) when AGR=0
- Ÿ   Output over max value (255) when AGR=1

n ACE   ADC Calibration Enable
- Ÿ 0   Disable
- Ÿ 1   Enable

n AGR   Auto Gain Result Selection
- Ÿ 0   Output has Max/Min Value
- Ÿ 1   Output is Overflow/Underflow

n ATGM   Auto Gain Mode
- Ÿ 0   Normal Mode (result will be cleared every frame)
- Ÿ 1   History Mode (don't clear result until ATGE=0)

n ATGR   Auto Gain result ready (read only)
- Ÿ 0   Result Not Ready
- Ÿ 1   Result Ready

n ATGE   Auto Gain Function Enable
- Ÿ 0   Disable
- Ÿ 1   Enable

Auto Gain Status

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
79h	ATGST	VCLP	-	CALR	CALG	CALB	MINR	MING	MINB	RO

n VCLP   Video auto gain Mode
- Ÿ 0   RGB mode
- Ÿ 1   YPbPr Mode

n CALR   Calibration value flag for red channel
- Ÿ 0   Normal
- Ÿ 1   Calibration result (need to increase offset) when ACE=1

n CALG   Calibration value flag for green channel
- Ÿ 0   Normal
- Ÿ 1   Calibration result (need to increase offset) when ACE=1

n CALB   Calibration value flag for blue channel
- Ÿ 0   Normal
- Ÿ 1   Calibration result (need to increase offset) when ACE=1

n MINR   Min value flag for red channel
- Ÿ 0   Normal
- Ÿ 1   Have min value (0) when AGR=0, ACE=0
- Ÿ   Output under min value (0) when AGR=1, ACE=0
- Ÿ   Calibration result (need to decrease offset) when ACE=1

n MING   Min value flag for green channel
- Ÿ 0   Normal
- Ÿ 1   Have min value (0) when AGR=0, ACE=0
- Ÿ   Output under min value (0) when AGR=1, ACE=0
- Ÿ   Calibration result (need to decrease offset) when ACE=1

n MINB   Min value flag for blue channel
- Ÿ 0   Normal
- Ÿ 1   Have min value (0) when AGR=0, ACE=0
- Ÿ   Output under min value (0) when AGR=1, ACE=0
- Ÿ   Calibration result (need to decrease offset) when ACE=1

Auto Position Function and Jitter Function Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
7Bh	ATOCTRL	JITLR	JITS	-	JITM	JITR	ATOM	ATOR	ATOE	R/W
7Ch	AOVDV	AOVDV[3:0]				-				R/W

- **n JITLR**   Jitter Function Left/Right Result for 86h and 87h
  - Ÿ 0   Left Result
  - Ÿ 1   Right Result
- **n JITS**   Jitter Software Clear
  - Ÿ 0   No clear
  - Ÿ 1   Clear
- **n JITM**   Jitter function mode
  - Ÿ 0   Update every frame
  - Ÿ 1   Keep the history value
- **n JITR**   Jitter Function Result (read only)
  - Ÿ 0   No Jitter
  - Ÿ 1   Have Jitter
- **n ATOM**   Auto Position function mode
  - Ÿ 0   Update every frame
  - Ÿ 1   Keep the history value
- **n ATOR**   Auto Position result ready (read only)
  - Ÿ 0   Result Not Ready
  - Ÿ 1   Result Ready
- **n ATOE**   Auto Position Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
  - Ÿ   Disable-to-enable needs at least 2 frames apart for ready bit to settle
- **n AOVDV[3:0]** Auto Position Valid Data Value
  - Ÿ 0000   Valid if data >= 0000 0000
  - Ÿ 0001   Valid if data >= 0001 0000
  - Ÿ 0010   Valid if data >= 0010 0000
  - Ÿ ...   ...
  - Ÿ 1111   Valid if data >= 1111 0000

Auto Position Function Result

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
7Eh	AOVST-L	AOVST[7:0]								RO
7Fh	AOVST-H	-					AOVST[10:8]			RO
80h	AOHST-L	AOHST[7:0]								RO
81h	AOHST-H	-				AOHST[11:8]				RO
82h	AOVEND-L	AOVEND[7:0]								RO
83h	AOVEND-H	-					AOVEND[10:8]			RO
84h	AOHEND-L	AOHEND[7:0]								RO
85h	AOHEND-H	-				AOHEND[11:8]				RO

- **n AOVST[10:0]**   Auto Position Detected Result Vertical Starting Point
- **n AOHST[11:0]**   Auto Position Detected Result Horizontal Starting Point
- **n AOVEND[10:0]**   Auto Position Detected Result Vertical End Point
- **n AOHEND[11:0]**   Auto Position Detected Result Horizontal End Point

Jitter Function Detecting Result

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
86h	JLR-L	JLR[7:0]								RO
87h	JLR-H	-					JLR[10:8]			RO

n JLR[10:0] Jitter function detected left/right most point state (previous frame) depend on Reg 7Bh bit 7

Auto Noise Reduction Function

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
88h	ANRF			HNEN	BGEN		ANLV[2:0]			RO

n HNEN High Level Noise Reduction Enable
 Ÿ 0 Disable
 Ÿ 1 Enable
n BGEN Background Noise Reduction Enable
 Ÿ 0 Disable
 Ÿ 1 Enable
n ANLV[2:0] Auto Noise Level
 Ÿ 111 Noise Level = 16

Auto Phase Control and Detecting Result

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
89h	ATPGTH	ATPGTH[7:0]								R/W
8Ah	ATPTTH	ATPTTH[7:0]								R/W
8Bh	ATPCTRL	-	GRY	TXT	APMASK[2:0]			ATPR	ATPE	R/W
8Ch	ATPV1	ATPVALUE[7:0]								RO
8Dh	ATPV2	ATPVALUE[15:8]								RO
8Eh	ATPV3	ATPVALUE[23:16]								RO
8Fh	ATPV4	ATPVALUE[31:24]								RO

n ATPGTH[7:0] Auto Phase Gray Scale Threshold for ATPV3 when ATPN4=0
n ATPTTH[7:0] Auto Phase Text Threshold for ATPV4
n GRY Gray Scale Detect (read only)
n TXT Text Detect (read only)
n ATPTH[4:0] Auto Phase threshold
n ATPMASK[2:0] Noise Mask
 Ÿ 000 Mask 0 bit, default value
 Ÿ 001 Mask 1 bit
 Ÿ 010 Mask 2 bit
 Ÿ 011 Mask 3 bit
 Ÿ 100 Mask 4 bit
 Ÿ 101 Mask 5 bit
 Ÿ 110 Mask 6 bit
 Ÿ 111 Mask 7 bit
n ATPR Auto Phase result ready
 Ÿ 0 Result Not Ready
 Ÿ 1 Result Ready
n ATPE Auto Phase Function Enable
 Ÿ 0 Disable
 Ÿ 1 Enable
n ATPVALUE[31:0] Auto Phase Value

VSYNC Status

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
90h	ASCTRL	IVB	-	DLINE[1:0]		-		UNDER	OVER	R/W
91h	LSLVP-L	LSLVP[7:0]								RO
92h	LSLVP-H	-					LSLVP[10:8]			RO
93h	LSLW-L	LSLW[7:0]								RO

VSYNC Status

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
94h	LSLW-H						LSLW[10:8]			RO
95h	LVSST-L	LVSSTATE[7:0]								RO
96h	LVSST-H		-				LVSSTATE[10:8]			RO
97h	LHTST-L	LHTSTAT[7:0]								RO
98h	LHTST-H	-					LHTSTAT[10:8]			RO
99h	LFRST-L	LFRSTAT[7:0]								R/W
9Ah	LFRST-H	-					LFRSTAT[10:8]			R/W
9Bh	LMARGIN	LHTTMGN[7:0]								R/W
9Ch	LRSV-L	LRSVALUE[7:0]								R/W
9Dh	LRSV-H	-					LRSVALUE[10:8]			R/W
9Eh	LMARGIN	LSSCMGN[7:0]								R/W

- **IVB** Input VSYNC Blanking Status
  - Ÿ 0 In display
  - Ÿ 1 In blanking
- **DLINE[1:0]** Delay Line
- **UNDER** Under run status
- **OVER** Over run status
- **LSLVP[10:0]** Locking Short Line Vertical Position
- **LSLW[10:0]** Locking Short Line Width
- **LVSSTAT[10:0]** Locking Vertical Total Line Number
- **LHTSTAT[10:0]** Locking H total Status
- **LFRSTAT[10:0]** Locking Fraction Status
- **LHTTMGN[7:0]** Locking H total Margin
- **LRSVALUE[10:0]** Locking Read Start Value
- **LSSCMGN[7:0]** Locking SSC Margin

OSD I/O Access

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
A0h	OSDIOA	OSBM	CLR	-	RF	DC	DA	ORBW	-	R/W

- **OSBM** OSD SRAM I/O Access Burst Mode
  - Ÿ 0 Disable
  - Ÿ 1 Enable
- **CLR** OSD Clear Bit (write only)
  - Ÿ 0 Normal
  - Ÿ 1 Clear code with 00h, attribute with 00h
- **RF** OSD RAM Font I/O Access
  - Ÿ 0 Disable
  - Ÿ 1 Enable
- **DC** OSD Display Code I/O Access
  - Ÿ 0 Disable
  - Ÿ 1 Enable
- **DA** OSD Display Attribute I/O Access
  - Ÿ 0 Disable
  - Ÿ 1 Enable
- **ORBW** OSD Register Burst Write Mode
  - Ÿ 0 Disable
  - Ÿ 1 Enable

OSD Register Address/Data Port

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
A1h	OSDRA	-	OSDRA[6:0]							R/W
A2h	OSDRD	OSDRD[7:0]								R/W

n OSDRA[6:0]   OSD Register Address Port
n OSDRD[7:0]   OSD Register Data Port

OSD RAM Font Address/Data Port

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
A3h	RAMFA	RAMFA[7:0]								R/W
A4h	RAMFD	RAMFD[7:0]								R/W

n RAMFA[7:0]   OSD RAM Font Address Port
n RAMFD[7:0]   OSD RAM Font Data Port

OSD Display Code Address/Data Port

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
A5h	DISPCA-L	DISPCA[7:0]								R/W
A6h	DISPCA-H	-							DISPCA[8]	R/W
A7h	DISPCD	DISPCD[7:0]								R/W

n DISPCA[8:0]   OSD Display Code Address Port
n DISPCD[7:0]   OSD Display Code Data Port

OSD Display Attribute Address/Data Port

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
A8h	DISPAA-L	DISPAA[7:0]								R/W
A9h	DISPAA-H	-							DISPAA[8]	R/W
AAh	DISPAD	DISPAD[7:0]								R/W

n DISPAA[8:0]   OSD Display Attribute Address Port
n DISPAD[7:0]   OSD Display Attribute Data Port

Frame Rate Convert for Fail-Safe Mode / LVDS/RSDS Test Mode Data

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
Scaler bank register 0xD0[0] = 0										
ABh	FSM	FSMEN	FSMRATIO[3:0]			-				R/W
Scaler bank register 0xD0[0] = 1										
ABh	TSTDATA	TSTDATA[7:0]								R/W

Ÿ   Scalar bank register 0xD0[0] = 0
n FSMEN   Frame rate control enable
   Ÿ 0   Disable
   Ÿ 1   Enable
n FSMRATIO[3:0]   Output frame rate / input frame rate
   Ÿ Bit[3]   1 / 2
   Ÿ Bit[2]   1 / 4
   Ÿ Bit[1]   1 / 8
   Ÿ Bit[0]   1 / 16
Ÿ   Scalar bank register 0xD0[0] = 1
n TSTDATA[7:0]   LVDS/RSDS test mode data
   Ÿ   When LVDS output, use TSTDATA[7:1]
   Ÿ   When RSDS output, use TSTDATA[7:0]

I/O and PWM Control (16, B8h – C8h)

Watchdog Timer Function Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
B0h	WDTEN	-						WDTC	WDTE	R/W
B1h	WDTKEY	WDTKEY[7:0]								R/W
B2h	WDTCNT	WDTCNT[7:0]								R/W

- n WDTC   Watchdog Timer Clear (protected by WDTKEY)
  - Ÿ 0   Normal
  - Ÿ 1   Clear
- n WDTE   Watchdog Timer Enable (protected by WDTKEY)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n WDTKEY[7:0]   Watchdog Timer Enable Key
  - Ÿ   To disable/clear Watchdog Timer, you must first write the WDTKEY with 55h, Aah to unlock.
- n WDTCNT[7:0]   Watchdog Timer Counter
  - Ÿ   The clock of Watchdog timer is frequency of XTAL/(256*1024)

DDC Function Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
B3h	DDCEN	GPOU[1:0]		DMEN	CSOK	DMST	DMF	GPO1	GPO0	R/W
B4h	DDCEN	D_EN1	DFLT	DIWP	ISPT	CSOK1	D_BSY1	D_RW1	D_DTY1	R/W
B5h	DDC_LAST	-	DDC_LAST1[6:0]							RO
B6h	DDCADDR	S_RW1	DDC_ADDRP1[6:0]							R/W
B7h	DDCDATA	DDC_DATAP1[7:0]								R/W
B8h	DDCEN	D_EN2	-				D_BSY2	D_RW2	D_DTY2	R/W
B9h	DDC_LAST	-	DDC_LAST2[6:0]							RO
Bah	DDCADDR	S_RW2	DDC_ADDRP2[6:0]							R/W
BBh	DDCDATA	DDC_DATAP2[7:0]								R/W

- n GPOU[1:0]   GPO Usage
  - Ÿ 00   GPO
  - Ÿ 01   MPU bypass
  - Ÿ 10   DDC bypass
  - Ÿ 11   ISP bypass (use I2C protocol)
- n DMEN   DDC Master Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n CSOK   DDC Check sum (read only)
  - Ÿ 0   Check sum not ok
  - Ÿ 1   Check sum ok
- n DMST   DDC Master Function Status (read only)
  - Ÿ 0   Busy
  - Ÿ 1   Not busy
- n DMF   DDC Master Finish, already access 128 or 256 byte data (read only)
  - Ÿ 0   Not finish
  - Ÿ 1   Finish
- n GPO[1:0]   GPO
- n D_EN   DDC Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n DFLT   DDC Filter
  - Ÿ 0   Enable

   Ÿ 1   Disable
- **DIWP**   DDC I2C bus Write Protect
  - Ÿ 0   Enable
  - Ÿ 1   Disable
- **ISPT**   ISP Using RS-232 Type
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **CSOK1**   DDC Check sum for input 1 (read only)
  - Ÿ 0   Check sum not ok
  - Ÿ 1   Check sum ok
- **D_BSY**   DDC Busy (read only)
  - Ÿ 0   Not busy
  - Ÿ 1   Busy
- **D_RW**   DDC Last Read/Write Status (read Only)
  - Ÿ 0   Write
  - Ÿ 1   Read
- **D_DTY**   DDC SRAM Dirty status (read/clear)
  - Ÿ 0   Not Dirty
  - Ÿ 1   Dirty
- **DDC_LAST[6:0]**   DDC Last R/W Address
- **S_RW**   DDC SRAM Read/Write
  - Ÿ 0   Write
  - Ÿ 1   Read
- **DDC_ADDRP[6:0]** DDC Address Port
- **DDC_DATAP[7:0]** DDC Data Port

MISC Function Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
BCh	MISCFC	AFT	IDHTT	VSGR	VSP	LBCG	DEGP	-		R/W

- **AFT**   ATP filter for Text (4 frame)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **IDHTT**   DE Only Mode HTT count by IDCLK
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **VSGR**   VSYNC glitch removal with line less than 2 (DE only)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **VSP**   VSYNC protect with V total (DE only)
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **LBGC**   LB Clock no gating mode
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **DEGP**   DE Only Mode Glitch Protect for Position
  - Ÿ 0   Disable
  - Ÿ 1   Enable when F3 Bit7 = 1 and in DE Only Mode

PWM Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
C2h	PWMCLK	-							PCLK	R/W
C3h	PWM0C	PWM0C[7:0]								R/W
C4h	PWM1C	PWM1C[7:0]								R/W

- **PCLK**   PWM base clock select

- Ÿ 0   14.318MHz
- Ÿ 1   14.318MHz / 4
- **n** PWM0C[7:0]   PWM0 Coarse adjustment
- **n** PWM1C[7:0]   PWM1 Coarse adjustment

Interrupt Control (9, Cah – D2h)

Interrupt Control									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
Cah	INTCTRL	HCHGM	DCMD	HSPM	HSST	IVSI	OVSI	TRG	INTT	R/W
CBh	INTPULSE	INTPULSE[7:0]								R/W

- **n** HCHM   HSYNC changing Detect method
  - Ÿ 0   Interrupt only occurred at start and end of transition
  - Ÿ 1   Interrupt occurred at every line
- **n** DCMD   DVI Clock Missing Detected (read only; DVI feature only, independent of Scaler bank register 0x02h, ISEL[1:0])
  - Ÿ 0   DVI clock is OK
  - Ÿ 1   DVI clock is missing
- **n** HSPM   ADC mode: HSYNC pin monitor (read only), DVI mode: SCDT value
- Ÿ When input is analog
  - Ÿ 0   HSYNC pin is low
  - Ÿ 1   HSYNC pin is high
- Ÿ When input is DVI
  - Ÿ 0   SCDT is missing
  - Ÿ 1   SCDT is OK
- **n** HSST   HS status (read only)
  - Ÿ 0   Stable
  - Ÿ 1   In change
- **n** IVSI   Input V-SYNC interrupt generate by
  - Ÿ 0   Leading edge
  - Ÿ 1   Tailing edge
- **n** OVSI   Output V-SYNC interrupt generate by
  - Ÿ 0   Leading edge
  - Ÿ 1   Tailing edge
- **n** TRGC   Trigger condition
  - Ÿ 0   Active low for level trigger/falling edge for edge trigger
  - Ÿ 1   Active high for level trigger/rising edge for edge trigger
- **n** INTT   Interrupt trigger
  - Ÿ 0   Generate a edge trigger interrupt
  - Ÿ 1   Generate a level trigger interrupt
- **n** INTPULSE[7:0]   Interrupt Pulse Width by reference clock

Interrupt Status									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
CCh	INTSTA	INTSTA[7:0]								R/C
CDh	INTSTB	INTSTB[7:0]								R/C
Ceh	INTENA	INTENA[7:0]								R/W
CFh	INTENB	INTENB[7:0]								R/W

- **n** INTSTA[7:0]   Interrupt Status Byte A
  - Ÿ Bit 7   Input VSYNC Changed (co-work with register E7h)
  - Ÿ Bit 6   Input HSYNC Changed (co-work with register E6h)
  - Ÿ Bit 5   Input VSYNC disappear
  - Ÿ Bit 4   Input HSYNC disappear
  - Ÿ Bit 3   Input VSYNC edge

- Ÿ Bit 2   Output VSYNC edge
- Ÿ Bit 1   ADC0 HSYNC0 pin toggling (independent with Reg 02h ISEL[1:0])
- Ÿ Bit 0   Composite sync/SOG status change
- **n INTSTB[7:0]**   **Interrupt Status Control Byte B**
  - Ÿ Bit 7   Auto Phase Ready
  - Ÿ Bit 6   Auto Position Ready
  - Ÿ Bit 5   Auto Gain Ready
  - Ÿ Bit 4   Jitter Detected
  - Ÿ Bit 3   ADC1 HSYNC1 pin toggling
  - Ÿ Bit 2   DVI clock status change; no clock <-> with clock
  - Ÿ Bit 1   Watchdog Timer
  - Ÿ Bit 0   Under / over run occurred
- **n INTENA[7:0]**   **Interrupt Enable Control Byte A**
  - Ÿ 0   Disable Interrupt
  - Ÿ 1   Enable Interrupt
- **n INTENB[7:0]**   **Interrupt Enable Control Byte B**
  - Ÿ 0   Disable Interrupt
  - Ÿ 1   Enable Interrupt

Clock generator (16, D0h-Dfh)

Clock Generator Control										
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
D0h	PLLCRTL1	XOUT	EOCK	XDIV[1:0]		BPM	TSTM	PTEN	LRTM	R/W
D1h	PLLCTRL2	MPPDIV	LP_POR	LP_RST	LP_PD	MP_K	MP_POR	MP_RST	MP_PD	R/W

- **n XOUT**   **Enable PWM1 as XTAL clock output**
  - Ÿ 0   Disable
  - Ÿ 1   Enable, default value
- **n EOCK**   **Use External Clock (pin #) as Output Dot Clock**
  - Ÿ 0   Disable (use internal dot clock)
  - Ÿ 1   Enable (use external dot clock), default value
- **n XDIV**   **XTAL clock divide by**
  - Ÿ 00   16
  - Ÿ 01   08
  - Ÿ 10   04
  - Ÿ 11   01
- **n BPM**   **Bypass Clock Mode (IDCLK as ODCLK)**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n TSTM**   **Test Mode**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n PTEN**   **PLL Test Register Protect Bit**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n LRTM**   **LVDS/RSDS Test Mode Enable**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n MPPDIV**   **MPLL Post Divider**
  - Ÿ 0   div 3 (143 MHz)
  - Ÿ 1   div 2.5 (172 MHz), for output dot clock higher than 143Mhz (Vertical=85Hz)
- **n LP_POR**   **Output PLL Power On Reset**
- **n LP_RST**   **Output PLL Reset**
- **n LP_PD**   **Output PLL Power Down**
- **n MP_K**   **Master PLL output frequency divided by 2**

n MP_POR   Master PLL Power On Reset
n MP_RST   Master PLL Reset
n MP_PD   Master PLL Power Down

Master & Output PLL Control										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
D2h	MPLL_M	MP_ICTRL[2:0]			MPLL_M4:0]					R/W
D3h	LPLL_M	-	SDEN	SDMD	LPLL_M4:0]					R/W
D4h	LPLL_CTL2	SCTRL[1:0]		LP_TP	LP_K[1:0]		LP_ICTRL[2:0]			R/W

n MPLL_M[4:0]   Master PLL divider
n MP_K   Master PLL Post Divider
n MP_ICTRL[2:0]   Master PLL Current Control
   Ÿ 000   2.5 uA
   Ÿ 001   5.0 uA
   Ÿ 010   7.5 uA
   Ÿ 011   10.0 uA, recommended
   Ÿ 100   12.5 uA
   Ÿ 101   15.0 uA
   Ÿ 110   20.0 uA
   Ÿ 111   40.0 uA
n LPLL_M[4:0]   Output PLL divider
n LP_PD   Output PLL Power Down
n LP_RST   Output PLL Reset
n LP_POR   Output PLL Power On Reset
n LP_TP   Output PLL Type
   Ÿ 0   LVDS
   Ÿ 1   RSDS/TTL
n SCTRL[1:0]   SSC Control
   Ÿ 0x   Normal
   Ÿ 10   Disable SSC 2 lines
   Ÿ 11   Disable SSC More lines
n SDEN   Output PLL Spread Spectrum Enable
n SDMD   Output PLL Spread Spectrum Mode
   Ÿ 0   Normal
   Ÿ 1   Reverse for Mode 1
n LP_K[1:0]   Output PLL Post Divider
   Ÿ 00   8
   Ÿ 01   4
   Ÿ 10   2
   Ÿ 11   1
n LP_ICTRL[2:0]   Output PLL Current Control
   Ÿ 000   1.25 uA
   Ÿ 001   2.50 uA
   Ÿ 010   3.75 uA
   Ÿ 011   5.00 uA, recommended
   Ÿ 100   6.25 uA
   Ÿ 101   7.50 uA
   Ÿ 110   10.0 uA
   Ÿ 111   20.0 uA

Frequency Synthesizer & SSC Control										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
D5h	LPLL_SET	LP_SET[7:0]								R/W, DB

Frequency Synthesizer & SSC Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
D6h	LPLL_SET	LP_SET[15:8]								R/W, DB
D7h	LPLL_SET	LP_SET[23:16]								R/W, DB
D8h	LPLL_STEP	LP_STEP[7:0]								R/W, DB
D9h	LPLL_STEP						LP_STEP[10:8]			R/W, DB
Dah	LPLL_SPAN	LP_SPAN[7:0]								R/W, DB
DBh	LPLL_SPAN	-	LP_SPAN[14:8]							R/W, DB

n LP_SET[23:0]   Output PLL SET
n LP_STEP[10:0]   Output PLL Spread Spectrum Step
n LP_SPAN[14:0]   Output PLL Spread Spectrum Span

PLL Test Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
DCh	MPLL_TST	MP_TEST[7:0]								R/W
DDh	LPLL_TSTD	LP_TESTD[7:0]								R/W
Deh	LPLL_TSTA	LP_TESTA[7:0]								R/W
DFh	SSC_TST	LP_TESTD[15:8]								R/W

Mode Detect Status (10, E0h-E9h)

Input Sync Monitor									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
E0h	STATUS1	-				IHSM	IVSM	OHSM	OVSM	RO

n IHSM   Input normalized horizontal SYNC pin monitor
   Ÿ   Show input horizontal SYNC pin directly
n IVSM   Input normalized vertical SYNC pin monitor
   Ÿ   Show input vertical SYNC pin directly
n OHSM   Output normalized horizontal SYNC pin monitor (pin OHSYNC)
   Ÿ   Show output horizontal SYNC directly
n OVSM   Output normalized vertical SYNC monitor (pin OVSYNC)
   Ÿ   Show output vertical SYNC directly

Mode Detect Status									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
E1h	STATUS2	-	-	CSD	SOGD	INTM	INTF	IHSP	IVSP	RO
E2h	VTOTAL-L	VTOTAL[7:0]								RO
E3h	VTOTAL-H	-					VTOTAL[10:8]			RO
E4h	HSPRD-L	HSPRD[7:0]								RO
E5h	HSPRD-H	IHDM	-			HSPRD[12:8]				RO

n CSD   Composite Sync Detected Status
   Ÿ 0   Input is not Composite sync.
   Ÿ 1   Input is detected as Composite sync
n SOGD   Sync On Green Detected Status
   Ÿ 0   Input is not SOG.
   Ÿ 1   Input is detected as SOG
n INTM   Interlace/Non-interlace detecting result by this chip
   Ÿ 0   Non-interlace
   Ÿ 1   Interlace
n INTF   Input ODD/EVEN field detecting result by this chip
   Ÿ 0   EVEN

- Ÿ 1   ODD
- **n** IHSP   Incoming input horizontal SYNC polarity detecting result by this chip
  - Ÿ 0   Active low
  - Ÿ 1   Active high
- **n** IVSP   Incoming input vertical SYNC polarity detecting result by this chip
  - Ÿ 0   Active low
  - Ÿ 1   Active high
- **n** VTOTAL[10:0]   Input Vertical Total, count by HSYNC
- **n** IHDM   Input HSYNC period Detect Mode
  - Ÿ 0   One Line
  - Ÿ 1   16 Line
- **n** HSPRD[12:0]   Input Horizontal Period, count by reference clock

Sync Change Tolerance

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
E6h	HSTOL	HSTOL[7:0]								R/W
E7h	VSTOL	-		ANGF	ANG	VSTOL[3:0]				R/W

- **n** HSTOL[7:0]   HSYNC Tolerance
  - Ÿ 5   Default value
- **n** VSTOL[3:0]   VSYNC Tolerance
  - Ÿ 1   Default value
- **n** ANGF   Auto No Signal Filter Mode
- **n** ANG   Auto No Signal

Status Override/Interlace Detect

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
E8h	ISOVRD	VERR	CSHS	UVSP	IVSJ	UHSP	IHSJ	UINT	INTJ	R/W
E9h	MDCTRL	-				VFIV	VEXF	INTF	IFI	R/W

- **n** VERR   Video CCIR656 Error correct
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n** CSHS   HSYNC in coast
  - Ÿ 0   HSOUT (recommended)
  - Ÿ 1   Re-shaped HSYNC
- **n** UVSP   User defined input vertical SYNC Polarity, active when IVSJ=1.
  - Ÿ 0   Active LOW
  - Ÿ 1   Active High
- **n** IVSJ   Input vertical SYNC Polarity judgment
  - Ÿ 0   Use result of internal circuit detection
  - Ÿ 1   Defined by user (UVSP)
- **n** UHSP   User defined input horizontal SYNC Polarity active when IHSJ=1.
  - Ÿ 0   Active LOW
  - Ÿ 1   Active High
- **n** IHSJ   input horizontal SYNC Polarity judgment
  - Ÿ 0   Use result of internal circuit detection
  - Ÿ 1   Defined by user (UHSP)
- **n** UINT   User defined non-interlace/Interlace active when INTJ=1.
  - Ÿ 0   Non-interlace
  - Ÿ 1   Interlace
- **n** INTJ   Interlace judgment
  - Ÿ 0   Use result of internal circuit detection
  - Ÿ 1   Defined by user (UINT)
- **n** VFIV   Video Field Inversion
  - Ÿ 0   Normal

- Ÿ 1   Invert
- n **VEXF**   **Video External Field**
  - Ÿ 0   Use result of internal circuit detection
  - Ÿ 1   Use external field
- n **INTF**   **Interlace Field detect method select**
  - Ÿ 0   Use the HSYNC numbers of a field to judge
  - Ÿ 1   Use the relationship of VSYNC and HSYNC to judge
- n **IFI**   **Interlace Field Invert**
  - Ÿ 0   Normal
  - Ÿ 1   Invert

SOG HSYNC Pulse Width

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
Eah	SOGHSPW	SOGHSPW[7:0]								RO

- n **SOGHSPW[7:0]**   **SOG HSYNC Pulse width (OSC clock base unit)**

Misc. Control (13, Edh – F6h)

Coast Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
Edh	COCTRL1	-		AVIS	DLYV	CSCM	EXVS	COVS	CTA	R/W
Eeh	COCTRL2	COST[7:0]								R/W
Efh	COCTRL3	COEND[7:0]								R/W

- n **AVIS**   **Analog Video Input Select**
  - Ÿ 0   PC
  - Ÿ 1   Component analog video
- n **DLYV**   **Analog Delay Line for component analog video input**
  - Ÿ 0   Delay 1 line
  - Ÿ 1   Don't delay
- n **CSCM**   **Composite SYNC Cut Mode**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n **EXVS**   **External VSYNC polarity (only used when COVS is 1)**
  - Ÿ 0   Normal
  - Ÿ 1   Invert
- n **COVS**   **Coast VSYNC Select**
  - Ÿ 0   Internal VSEP
  - Ÿ 1   External VSYNC
- n **CTA**   **Coast To ADC**
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n **Define the Coast signal coverage range**
- n **COEND[7:0]**   **End tuning**
  - Ÿ 00   COAST end at 1 HSYNC leading edge
  - Ÿ 01   COAST end at 2 HSYNC leading edge, default value
  - Ÿ ...   ...
  - Ÿ 254   COAST end at 255 HSYNC leading edge
  - Ÿ 255   COAST end at 256 HSYNC leading edge
- n **COST[7:0]**   **Front tuning**
  - Ÿ 00   COAST start from 1 HSYNC leading edge
  - Ÿ 01   COAST start from 2 HSYNC leading edge, default value
  - Ÿ ...   ...
  - Ÿ 254   COAST start from 255 HSYNC leading edge
  - Ÿ 255   COAST start from 256 HSYNC leading edge

Power Down Control/Software Reset

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F0h	PDMD	APDLD	APDLA	-	PDDS	GCLK[1:0]		PDMD[1:0]		R/W
F1h	SWRST	-		ADCR	GPR	DPR	BIUR	OSDR	SWR	R/W

n APDLD   Automatically Power Down when Low Power using Digital pin
- Ÿ 0   Disable
- Ÿ 1   Enable

n APDLA   Automatically Power Down when Low Power using Analog Pin
- Ÿ 0   Disable
- Ÿ 1   Enable

n PDDS   Power Down DDC SRAM
- Ÿ 0   Normal
- Ÿ 1   Power Down while not used

n GCLK[1:0]   Gated Clock for SRAM (excluding DDC SRAM)
- Ÿ 00   Normal
- Ÿ 01   V Blank
- Ÿ 10   H Blank and V Blank
- Ÿ 11   Reserved

n PDMD[1:0]   Power Down Mode
- Ÿ 00   Normal (no power saving)
- Ÿ 01   Output (OSD) Only (used when no input signal)
- Ÿ 10   BIU, Mode detection, GOUT are functional
- Ÿ 11   All chip power down

n ADCR   ADC Reset
- Ÿ 0   Normal operation
- Ÿ 1   Reset ADC

n GPR   Graphic Port Reset
- Ÿ 0   Normal operation
- Ÿ 1   Reset

n DPR   Display Port Reset
- Ÿ 0   Normal operation
- Ÿ 1   Reset

n BIUR   BIU Reset
- Ÿ 0   Normal operation
- Ÿ 1   Reset BIU

n OSDR   Internal OSD Reset
- Ÿ 0   Normal operation
- Ÿ 1   Reset Internal OSD

n SWR   Software reset (reset GP, DP, BIU and OSD)
- Ÿ 0   Normal operation
- Ÿ 1   Reset

Output Signal Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F2h	OSCTRL	OCLKDLY[3:0]/RSCK_SKE[3:0]				OCLK	ODE	OVS	OHS	R/W

n OCKDLY[3:0]   OCLK delay adjustment (TCON feature only)
- Ÿ   16 steps to adjust
- Ÿ   Typical 0.8ns delay/step

n RSCK_SKE[3:0]   RSDS clock adjust
- Ÿ RSCK_SKE[3]   RSDS clock inverted
  - Ÿ 0   Normal clock output
  - Ÿ 1   RSDS clock output inverted

- Ÿ RSCK_SKE[2:0] RSDS clock skew adjust
  - Ÿ 000   Max. setup time/min. hold time to RSDS data output
  - Ÿ 001   ...
  - Ÿ 011   ...
  - Ÿ 111   Min. setup time/max. hold time tot RSDS data output
- n OCLK   Output CLK Control
  - Ÿ 0   Normal
  - Ÿ 1   Invert
- n ODE   Output DE Control
  - Ÿ 0   Active High
  - Ÿ 1   Active Low
- n OVS   Output VSYNC Control
  - Ÿ 0   Active High
  - Ÿ 1   Active Low
- n OHS   Output HSYNC Control
  - Ÿ 0   Active High
  - Ÿ 1   Active Low

Input Signal Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F3h	ISCTRL	DEGE	DEGR[2:0]			HSFL	ISSM	-	SCKI	R/W

- n DEGE   DE Glitch Removal Function Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- n DEGR[2:0]   DE Glitch Removal Range
- n HSFL   Input HSYNC filter
- Ÿ When input source is Analog
  - Ÿ 0   Filter OFF
  - Ÿ 1   Filter ON
- Ÿ When input source is DVI
  - Ÿ 0   Normal
  - Ÿ 1   More tolerance for unstable DE
- n ISSM   Input sync sample mode
  - Ÿ 0   Normal
  - Ÿ 1   Glitch-removal
- n SCKI   Input Sample CLK Invert
  - Ÿ 0   Normal
  - Ÿ 1   Invert

Output Tri-State Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F4h	TRISTATE	-	TCS	OEDB	OODB	OVS	OHS	ODE	OCLK	R/W

Note: The default value is 7Fh

- n TCS   HSYNC/VSYNC Control Signal pin tri-state control (TCON feature only)
  - Ÿ 0   Normal
  - Ÿ 1   Tri-state
- n OEDB   Output Even Data Bus pin control
  - Ÿ 0   Normal
  - Ÿ 1   TRI-state
- n OODB   Output Odd Data Bus pin control
  - Ÿ 0   Normal
  - Ÿ 1   TRI-state
- n OVS   OVSYNC pin control
  - Ÿ 0   Normal

  Ÿ 1   TRI-state
- **OHS**   **OHSYNC pin control**
  Ÿ 0   Normal
  Ÿ 1   TRI-state
- **ODE**   **ODE pin control**
  Ÿ 0   Normal
  Ÿ 1   TRI-state
- **OCLK**   **OCLK pin control**
  Ÿ 0   Normal
  Ÿ 1   TRI-state

Output Driving Current Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F5h	ODRV	DEDRV[1:0]		CLKDRV[1:0]		ODDDRV[1:0]		EVENDR[1:0]		R/W

- **DEDRV[1:0]**   **Output DE Driving Current Select**
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA
- **CLKDRV[1:0]**   **Output Clock Driving Current Select**
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA
- **ODDDRV[1:0]**   **Output Data Odd Channel Driving Current Select**
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA
- **EVENDR[1:0]**   **Output Data Even Channel Driving Current Select**
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA

Even Clock Delay Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F6h	ECLKDLY	-		SKEW[1:0]		ECLKDLY[3:0]/TESTMOD[15:12]				R/W

- **SKEW[1:0]**   **Output data skew**
- **ECKDLY[3:0]**   **ECLK delay adjustment (TCON feature only)**
  Ÿ   16 steps to adjust
  Ÿ   Typical 0.8ns delay/step
- **TESTMOD[15:14]** Reserved
- **TESTMOD[13]**   **RSDS differential output clock test mode**
  Ÿ 0   Normal operation
  Ÿ 1   Set RSDS differential output clock low
- **TESTMOD[12]**   **RSDS differential output clock test mode**
  Ÿ 0   Normal operation
  Ÿ 1   Set RSDS differential output clock high

RSDS SRAM Test Status

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F7h	RSDSTEST							RSRP	RSRF	RO

n RSRP   RSDS SRAM Test Result
  Ÿ 0   Not Pass
  Ÿ 1   Pass
n RSRF   RSDS SRAM Test Finish
  Ÿ 0   Not Finish
  Ÿ 1   Finish

Test Mode Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F8h	TEST	-	TEST_CLK_MODE	PLL_DIV2[1:0]		TESTMD[3:0]				R/W

n TEST_CLK_MODE
  Ÿ 0   Disable
  Ÿ 1   Enable, test clock tree
n PLL_DIV2[1:0]
  Ÿ 00   Normal
  Ÿ 01   ODCLK and LBCLK divided by 2
  Ÿ 10   Reserved
  Ÿ 11   Reserved
n TESTMD[3:0]   Test Mode
  Ÿ 0011   BIST

SRAM Test Status									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
F9h	SRAMTEST	DSRP	DSRF	GSRP	GSRF	OSRP	OSRF	LSRP	LSRF	RO

n DSRP   DDC SRAM Test Result
  Ÿ 0   Not Pass
  Ÿ 1   Pass
n DSRF   DDC SRAM Test Finish
  Ÿ 0   Not Finish
  Ÿ 1   Finish
n GSRP   Gamma SRAM Test Result
  Ÿ 0   Not Pass
  Ÿ 1   Pass
n GSRF   Gamma SRAM Test Finish
  Ÿ 0   Not Finish
  Ÿ 1   Finish
n OSRP   Internal OSD SRAM Test Result
  Ÿ 0   Not Pass
  Ÿ 1   Pass
n OSRF   Internal OSD SRAM Test Finish
  Ÿ 0   Not Finish
  Ÿ 1   Finish
n LSRP   Line buffer SRAM Test Result
  Ÿ 0   Not Pass
  Ÿ 1   Pass
n LSRF   Line buffer SRAM Test Finish
  Ÿ 0   Not Finish
  Ÿ 1   Finish

OSD Register

OSD Double Buffer Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
01h	OSDDBC	-					DBL[1:0]		DBE	R/W

- **n** DBL[1:0]   Double buffer load
  - Ÿ 00   Keep old register value
  - Ÿ 01   Load new data (auto reset to 00 when load finish)
  - Ÿ 10   Automatically load data at VSYNC blanking
  - Ÿ 11   Reserved
- **n** DBE   Double Buffer Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable

OSD Start Position

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
02h	OHSTA-L	OHSTA[7:0]								R/W
03h	OHSTA-H	-							OHSTA[8]	DB
04h	OVSTA-L	OVSTA[7:0]								R/W
05h	OVSTA-H	-							OVSTA[8]	DB

- **n** OHSTA[8:0]   OSD window horizontal start position = 4 * OHSTA + 48 (pixel)
- **n** OVSTA[8:0]   OSD window vertical start position = 4 * OVSTA (line)

OSD Size Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
06h	OSDW	-		OSDW[5:0]						R/W, DB
07h	OSDH	-			OSDH[4:0]					R/W, DB

- **n** OSDW[5:0]   OSD window width = OSDW + 1 (column), maximum 64 columns
- **n** OSDH[4:0]   OSD window height = OSDH + 1 (row), maximum 32 rows

OSD Space Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
08h	OHSPA	-		OHSPA[5:0]						R/W
09h	OVSPA	-			OVSPA[4:0]					R/W
0Ah	OSPW	OSPW[7:0]								R/W
0Bh	OSPH	OSPH[7:0]								R/W

- **n** OHSPA[5:0]   OSD window horizontal space start position = OHSPA + 1 (row)
- **n** OVSPA[4:0]   OSD window vertical space start position = OVSPA + 1 (column)
- **n** OSPW[7:0]   OSD space width = 8 * OSPW (pixel)
- **n** OSPH[7:0]   OSD space height = 8 * OSPH (line)

Internal OSD Control 1

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Ch	IOSDC1	OVS[1:0]		OHS[1:0]		MWB	-		MWIN	R/W DB

- **n** OVS[1:0]   OSD vertical scaling
  - Ÿ 00   Vertical normal size
  - Ÿ 01   Vertical enlarged x2 by repeated pixels
  - Ÿ 10   Vertical enlarged x3 by repeated pixels

- Ÿ 11   Vertical enlarged x4 by repeated pixels
- **n OHS[1:0]**   OSD horizontal scaling
  - Ÿ 00   Horizontal normal size
  - Ÿ 01   Horizontal enlarged x2 by repeated pixels
  - Ÿ 10   Horizontal enlarged x3 by repeated pixels
  - Ÿ 11   Horizontal enlarged x4 by repeated pixels
- **n MWBT**   OSD Main Window Border Type
  - Ÿ 0   Bottom-right direction boundary (shadow border)
  - Ÿ 1   All direction boundary (border)
- **n MWIN**   OSD Main Window Display
  - Ÿ 0   Main window OFF
  - Ÿ 1   Main window ON

Internal OSD Control 2									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
0Dh	IOSDC2	CF8E	BCLR[2:0]			BDC	BDW	C16_PAL	CF4E	R/W

- **n CF8E**   8 color font enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n BCLR[3:0]**   OSD Border Color Index; BCLR[3] is located at 0E Bit5
  - Ÿ 0000   Color Index 0
  - Ÿ 0001   Color Index 1
  - Ÿ 1111   Color Index 15
- **n BDC**   OSD Character Border Type Select
  - Ÿ 0   All direction font boundary (border)
  - Ÿ 1   Bottom – right direction font boundary (shadow)
- **n BDW**   OSD Character Border Width Control
  - Ÿ 0   One pixel width for all scale
  - Ÿ 1   Scale with OVS[1:0] and OHS[1:0]
- **n CPAL_SEL**
  - Ÿ 0   8 color palette
  - Ÿ 1   16 color palette
- **n CF4E**   4 Color Font Enable
  - Ÿ 0   Disable
  - Ÿ 1   Enable

Internal OSD Control 3									
Index	**Mnemonic**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Access**
0Eh	IOSDC3		CKIND[3]	BCLR[3]	SCLR[3]	SDC	SCLR[2:0]			R/W, DB

- Ÿ When OSD register 0x10[7]=0, OSD is backward compatible
- **n CKIND[3]**   Color Index Bit 3 of Color Key
- Ÿ When OSD register 0x10[7]=1, OSD is not backward compatible
- **n CKIND[3]**   Resevred
- **n BCLR[3]**   Border Color Bit 3; this bit should work with OSD 0D Bit[6:4]
- **n SDC**   OSD Window Shadow Control
  - Ÿ 0   OFF
  - Ÿ 1   ON
- **n SCLR[3:0]**   OSD Window Shadow Color Index
  - Ÿ 0000   Color Index 0
  - Ÿ 0001   Color Index 1
  - Ÿ ...   ...
  - Ÿ 1111   Color Index 15

OSD Window Shadow Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0Fh	OSHC	OSDSH[3:0]				OSDSW[3:0]				R/W

- **n** OSDSH[3:0]   OSD Shadow Height
- **n** OSDSW[3:0]   OSD Shadow Width

OSD Color Font Format

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
10h	OCFF	OCFF	-			CFCT				R/W

- **n** OCFF   OSD backward compatibility
  - Ÿ 0   Back compatible
  - Ÿ 1   Not backward compatible
- **n** CFCTOSD   Color Font Code Address Type
  - Ÿ 0   RAM base
  - Ÿ 1   Code base

OSD Color Font Starting Address

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
11h	OSDCFA	OSD4CFA[7:0]								R/W

- **n** OSDCFA[7:0]   OSD 4 Color RAM Font Starting Address

OSD Code Buffer Offset/Base Address

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
12h	OCBUFO	COS	-	OOFFSET[5:0]						R/W
13h	OSDBA-L	OSDBA[7:0]								R/W
14h	OSDBA-H	-						OSDBA[9:8]		DB

- **n** COS   OSD Code Buffer Offset Select
  - Ÿ 0   Use OSDW[5:0] as offset
  - Ÿ 1   Use OOFFSET[5:0] as offset
- **n** OOFFSET[5:0] OSD code buffer offset value
- **n** OSDBA[8:0]   OSD Code Base Address

OSD Gradually Color Control

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
15h	GCCTRL	GVS[1:0]		GHS[1:0]		GRAD	GCRNG[2:0]			R/W

- **n** GVS[1:0]   Gradually Color vertical scaling
  - Ÿ 00   Vertical normal size
  - Ÿ 01   Vertical enlarged x2 by repeated pixels
  - Ÿ 10   Vertical enlarged x3 by repeated pixels
  - Ÿ 11   Vertical enlarged x4 by repeated pixels
- **n** GHS[1:0]   Gradually Color horizontal scaling
  - Ÿ 00   Horizontal normal size
  - Ÿ 01   Horizontal enlarged x2 by repeated pixels
  - Ÿ 10   Horizontal enlarged x3 by repeated pixels
  - Ÿ 11   Horizontal enlarged x4 by repeated pixels
- **n** GRAD   Enable OSD Gradually Color Function
  - Ÿ 0   Disable
  - Ÿ 1   Enable
- **n** GCRNG[2:0]   Gradually Color Applied Range
  - Ÿ 000   Sub Window 0

- Ÿ 001   Sub Window 1
- Ÿ 010   Sub Window 2
- Ÿ 011   Sub Window 3
- Ÿ 1xx   Full Screen

OSD Starting Gradually Color

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
16h	GRADCLR	-	F/B	RCLR[1:0]		GCLR[1:0]		BCLR[1:0]		R/W

- **n F/B**   **Gradually Applied Color**
  - Ÿ 0   Background Color
  - Ÿ 1   Foreground Color
- **n RCLR[1:0]**   **Red Starting Gradually Color**
  - Ÿ 00   Red color is 00h
  - Ÿ 01   Red color is 55h
  - Ÿ 10   Red color is Aah
  - Ÿ 11   Red color is FFh
- **n GCLR[1:0]**   **Green Starting Gradually Color**
  - Ÿ 00   Green color is 00h
  - Ÿ 01   Green color is 55h
  - Ÿ 10   Green color is Aah
  - Ÿ 11   Green color is FFh
- **n BCLR[1:0]**   **Blue Starting Gradually Color**
  - Ÿ 00   Blue color is 00h
  - Ÿ 01   Blue color is 55h
  - Ÿ 10   Blue color is Aah
  - Ÿ 11   Blue color is FFh

OSD Horizontal Gradually Color

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
17h	HGRADCR	SR	IRH	R_GRADH[5:0]						R/W
18h	HGRADCG	SG	IGH	G_GRADH[5:0]						R/W
19h	HGRADCB	SB	IBH	B_GRADH[5:0]						R/W
1Ah	HGRADSR	HGRADSR[7:0]								R/W
1Bh	HGRADSG	HGRADSG[7:0]								R/W
1Ch	HGRADSB	HGRADSB[7:0]								R/W

- **n SR**   **Sign Bit of Red Color**
  - Ÿ 0   Increase
  - Ÿ 1   Decrease
- **n IRH**   **Inverse Bit of Red Color**
  - Ÿ 0   Normal
  - Ÿ 1   Invert
- **n R_GRADH[6:0]**   **Increase/Decrease value of Red Color**
- **n SG**   **Sign Bit of Green Color**
  - Ÿ 0   Increase
  - Ÿ 1   Decrease
- **n IGH**   **Inverse Bit of Green Color**
- **n G_GRADH[6:0]**   **Increase/Decrease value of Green Color**
- **n SB**   **Sign Bit of Blue Color**
  - Ÿ 0   Increase
  - Ÿ 1   Decrease
- **n IBH**   **Inverse Bit of Blue Color**
- **n B_GRADH[6:0]**   **Increase/Decrease value of Blue Color**
- **n HGRADSR[7:0]**   **Horizontal Gradually Step of Red Color**

n HGRADSG[7:0]   Horizontal Gradually Step of Green Color
n HGRADSB[7:0]   Horizontal Gradually Step of Blue Color
For example, if RCLR=0, R_GRADH=16h, and HGRADSR=20h, then
Pixel 0   - 19 : 0
Pixel 20 – 39 : 16
Pixel 40 – 59 : 32
Etc.

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
OSD Vertical Gradually Color										
1Dh	VGRADCR	SR	IRV	R_GRADV[5:0]						R/W
1Eh	VGRADCG	SG	IGV	G_GRADV[5:0]						R/W
1Fh	VGRADCB	SB	IBV	B_GRADV[5:0]						R/W
20h	VGRADSR	VGRADSR[7:0]								R/W
21h	VGRADSG	VGRADSG[7:0]								R/W
22h	VGRADSB	VGRADSB[7:0]								R/W

n SR   Sign Bit of Red Color
  Ÿ 0   Increase
  Ÿ 1   Decrease
n IRV   Inverse Bit of Red Color
  Ÿ 0   Normal
  Ÿ 1   Invert
n R_GRADV[6:0]   Increase/Decrease value of Red Color
n SG   Sign Bit of Green Color
  Ÿ 0   Increase
  Ÿ 1   Decrease
n IGV   Inverse Bit of Green Color
n G_GRADV[6:0]   Increase/Decrease value of Green Color
n SB   Sign Bit of Blue Color
  Ÿ 0   Increase
  Ÿ 1   Decrease
n IBV   Inverse Bit of Blue Color
n B_GRADV[6:0]   Increase/Decrease value of Blue Color
n VGRADSR[7:0]   Horizontal Gradually Step of Red Color
n VGRADSG[7:0]   Horizontal Gradually Step of Green Color
n VGRADSB[7:0]   Horizontal Gradually Step of Blue Color

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
OSD Sub Window 0 Control										
23h	SUBW0C					BTN0	BD0	S0C	S0E	R/W, DB

n BTN0   Enable Button Function for sub window 0
  Ÿ 0   OFF
  Ÿ 1   ON
n BD0   Enable OSD Sub Window 0 Border
  Ÿ 0   Disable
  Ÿ 1   Enable
n S0C   Sub Window 0 color select
Ÿ If Button function is disabled
  Ÿ 0   From Sub Window 0 attribute
  Ÿ 1   From attribute RAM
Ÿ If Button function is enabled
  Ÿ 0   Set this bit with 0. Use Sub Window 0 attribute to select FG/BG color and use
                    attribute RAM to select button type
n S0E   Enable OSD Sub Window 0

Ÿ 0   Disable
Ÿ 1   Enable

OSD Sub Window 0 Horizontal/Vertical Position									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
24h	SW0HST	-	SW0HST[5:0]						R/W, DB
25h	SW0HEND	-	SW0HEND[5:0]						R/W, DB
26h	SW0VST	-		SW0VST[4:0]					R/W, DB
27h	SW0VEND	-		SW0VEND[4:0]					R/W, DB

n SW0HST[5:0]   Sub Window 0 Horizontal Start Position
n SW0HEND[5:0]   Sub Window 0 Horizontal End Position
n SW0VST[4:0]   Sub Window 0 Vertical Start Position
n SW0VEND[4:0]   Sub Window 0 Vertical End Position

OSD Sub Window 0 Attribute									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
28h	SUBW0A2	BLNK	FGCLR[2:0]			TRAN	BGCLR[2:0]			R/W

Note: When Button function is enabled, the FG/BG color is defined by window attribute, character attribute is used to define button border type and S0C (sub window color select) is disabled.

n BLNK   OSD Sub Window 0 Blink Control
  Ÿ 0   Disable
  Ÿ 1   Enable
n TRAN   OSD Sub Window 0 Transparency Control
  Ÿ 0   Disable
  Ÿ 1   Enable
n FGCLR[2:0]   OSD Sub Window 0 Foreground Color Select
  Ÿ 000   Color Index 0
  Ÿ 001   Color Index 1
  Ÿ ...   ...
  Ÿ 111   Color Index 7
n BGCLR[2:0]   OSD Sub Window 0 Background Color Select
  Ÿ 000   Color Index 0
  Ÿ 001   Color Index 1
  Ÿ ...   ...
  Ÿ 111   Color Index 7

Attribute SRAM									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
28h	SUBW0A2	-			BTNU	BTNTYPE[3:0]				R/W

n BTNU   Button Up Control
  Ÿ 0   Button Up
  Ÿ 1   Button Down
n BTNTYPE[3:0]   Button border type
  Ÿ 0   No button
  Ÿ 1

1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
□	⌐	⌐	⌐	⌐	⌐	⌐	∟	⌐	|	|	-	_	||	-

Note: The register of sub window 1, 2, and 3 are very similar with sub window 0

OSD Sub Window 1 Register

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
29h	SUBW1C					BTN1	BD1	S1C	S1E	R/W, DB
2Ah	SW1HST	-	SW1HST[5:0]							R/W, DB
2Bh	SW1HEND	-	SW1HEND[5:0]							R/W, DB
2Ch	SW1VST	-		SW1VST[4:0]						R/W, DB
2Dh	SW1VEND	-		SW1VEND[4:0]						R/W, DB
2Eh	SUBW1A	BLNK	FGCLR[2:0]			TRAN	BGCLR[2:0]			R/W

- n BTN1   Enable Button Function for sub window 1
- n BD1   Enable OSD Sub Window 1 Border
- n S1E   Enable OSD Sub Window 1
- n S1C   Sub Window 1 color select
- n SW1HST[5:0]   Sub Window 1 Horizontal Start Position
- n SW1HEND[5:0]   Sub Window 1 Horizontal End Position
- n SW1VST[4:0]   Sub Window 1 Vertical Start Position
- n SW1VEND[4:0]   Sub Window 1 Vertical End Position
- n BLNK   OSD Sub Window 1 Blink Control
- n FGCLR[2:0]   OSD Sub Window 1 Foreground Color Select
- n TRAN   OSD Sub Window 1 Transparency Control
- n BGCLR[2:0]   OSD Sub Window 1 Background Color Select

OSD Sub Window 2 Register

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
2Fh	SUBW2C	-				BTN2	BD2	S2C	S2E	R/W, DB
30h	SW2HST	-	SW2HST[5:0]							R/W, DB
31h	SW2HEND	-	SW2HEND[5:0]							R/W, DB
32h	SW2VST	-		SW2VST[4:0]						R/W, DB
33h	SW2VEND	-		SW2VEND[4:0]						R/W, DB
34h	SUBW2A	BLNK	FGCLR[2:0]			TRAN	BGCLR[2:0]			R/W

- n BTN2   Enable Button Function for sub window 2
- n BD2   Enable OSD Sub Window 2 Border
- n S2E   Enable OSD Sub Window 2
- n S2C   Sub Window 2 color select
- n SW2HST[5:0]   Sub Window 2 Horizontal Start Position
- n SW2HEND[5:0]   Sub Window 2 Horizontal End Position
- n SW2VST[4:0]   Sub Window 2 Vertical Start Position
- n SW2VEND[4:0]   Sub Window 2 Vertical End Position
- n BLNK   OSD Sub Window 2 Blink Control
- n FGCLR[2:0]   OSD Sub Window 2 Foreground Color Select
- n TRAN   OSD Sub Window 2 Transparency Control
- n BGCLR[2:0]   OSD Sub Window 2 Background Color Select

OSD Sub Window 3 Register

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
35h	SUBW3C	-				BTN3	BD3	S3C	S3E	R/W, DB
36h	SW3HST	-	SW3HST[5:0]							R/W, DB
37h	SW3HEND	-	SW3HEND[5:0]							R/W, DB
38h	SW3VST	-		SW3VST[4:0]						R/W, DB
39h	SW3VEND	-		SW3VEND[4:0]						R/W, DB
3Ah	SUBW3A	BLNK	FGCLR[2:0]			TRAN	BGCLR[2:0]			R/W

- n BTN3   Enable Button Function for sub window 3
- n BD3   Enable OSD Sub Window 3 Border

n S3E　　　　　 Enable OSD Sub Window 3
n S3C　　　　　 Sub Window 3 color select
n SW3HST[5:0]　 Sub Window 3 Horizontal Start Position
n SW3HEND[5:0]　 Sub Window 3 Horizontal End Position
n SW3VST[4:0]　 Sub Window 3 Vertical Start Position
n SW3VEND[4:0]　 Sub Window 3 Vertical End Position
n BLNK　　　　　 OSD Sub Window 3 Blink Control
n FGCLR[2:0]　 OSD Sub Window 3 Foreground Color Select
n TRAN　　　　　 OSD Sub Window 3 Transparency Control
n BGCLR[2:0]　 OSD Sub Window 3 Background Color Select

OSD 8 color Font Start Address

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
3Bh	OSD8CFFA	OSD8CFFA[7:0]								R/W
3Ch	OSD8CFCA	OSD8CFCA[7:0]								R/W

n OSD8CFFA[7:0]　 OSD 8 color font RAM address
n OSD8CFCA[7:0]　 OSD 8 color font code address

OSD Color Palette (when C16_PAL=0)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
58h	CLR0R	CLR0R[7:0]								R/W
59h	CLR0G	CLR0G[7:0]								R/W
5Ah	CLR0B	CLR0B[7:0]								R/W
5Bh	CLR1R	CLR1R[7:0]								R/W
5Ch	CLR1G	CLR1G[7:0]								R/W
5Dh	CLR1B	CLR1B[7:0]								R/W
5Eh	CLR2R	CLR2R[7:0]								R/W
5Fh	CLR2G	CLR2G[7:0]								R/W
60h	CLR2B	CLR2B[7:0]								R/W
61h	CLR3R	CLR3R[7:0]								R/W
62h	CLR3G	CLR3G[7:0]								R/W
63h	CLR3B	CLR3B[7:0]								R/W
64h	CLR4R	CLR4R[7:0]								R/W
65H	CLR4G	CLR4G[7:0]								R/W
66h	CLR4B	CLR4B[7:0]								R/W
67h	CLR5R	CLR5R[7:0]								R/W
68h	CLR5G	CLR5G[7:0]								R/W
69h	CLR5B	CLR5B[7:0]								R/W
6Ah	CLR6R	CLR6R[7:0]								R/W
6Bh	CLR6G	CLR6G[7:0]								R/W
6Ch	CLR6B	CLR6B[7:0]								R/W
6Dh	CLR7R	CLR7R[7:0]								R/W
6Eh	CLR7G	CLR7G[7:0]								R/W
6Fh	CLR7B	CLR7B[7:0]								R/W

OSD Color Palette (when C16_PAL=1)
16 color format: col[7:4],4'h0

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
58h	CLR0R	CLR0R[7:4]				CLR8R[7:4]				R/W
59h	CLR0G	CLR0G[7:4]				CLR8G[7:4]				R/W
5Ah	CLR0B	CLR0B[7:4]				CLR8B[7:4]				R/W

OSD Color Palette (when C16_PAL=1)
16 color format: col[7:4],4'h0

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
5Bh	CLR1R	CLR1R[7:4]				CLR9R[7:4]				R/W
5Ch	CLR1G	CLR1G[7:4]				CLR9G[7:4]				R/W
5Dh	CLR1B	CLR1B[7:4]				CLR9B[7:4]				R/W
5Eh	CLR2R	CLR2R[7:4]				CLR10R[7:4]				R/W
5Fh	CLR2G	CLR2G[7:4]				CLR10G[7:4]				R/W
60h	CLR2B	CLR2B[7:4]				CLR10B[7:0]				R/W
61h	CLR3R	CLR3R[7:4]				CLR11R[7:0]				R/W
62h	CLR3G	CLR3G[7:4]				CLR11G[7:4]				R/W
63h	CLR3B	CLR3B[7:4]				CLR11B[7:4]				R/W
64h	CLR4R	CLR4R[7:4]				CLR12R[7:4]				R/W
65H	CLR4G	CLR4G[7:4]				CLR12G[7:4]				R/W
66h	CLR4B	CLR4B[7:4]				CLR12B[7:4]				R/W
67h	CLR5R	CLR5R[7:4]				CLR13R[7:4]				R/W
68h	CLR5G	CLR5G[7:4]				CLR13G[7:4]				R/W
69h	CLR5B	CLR5B[7:4]				CLR13B[7:4]				R/W
6Ah	CLR6R	CLR6R[7:4]				CLR14R[7:4]				R/W
6Bh	CLR6G	CLR6G[7:4]				CLR14G[7:4]				R/W
6Ch	CLR6B	CLR6B[7:4]				CLR14B[7:4]				R/W
6Dh	CLR7R	CLR7R[7:4]				CLR15R[7:4]				R/W
6Eh	CLR7G	CLR7G[7:4]				CLR15G[7:4]				R/W
6Fh	CLR7B	CLR7B[7:4]				CLR15B[7:4]				R/W

OSD Random Test Pattern

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
71h	OSDRTP	-					RTPT	OSDRTP[1:0]		R/W

n RTPT   OSD Random Test Pattern Type
   Ÿ 0   RGB is same
   Ÿ 1   RGB is different
n OSDRTP[1:0]   OSD Random Test Pattern
   Ÿ 00   Disable
   Ÿ 01   1 random bit
   Ÿ 10   2 random bit
   Ÿ 11   Reserved

TCON Register (Bank=10)

Output Format Control 1 (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
02h	OFC1	IFC	IFS	IFE	DPFS	DPFC	DPFE	EEF	TCEN	R/W

n IFC   Inversion Function Combined
   Ÿ 0   Odd data inversion determined by OINV, even data inversion determined by EINV
   Ÿ 1   Odd/Even data inversion both determined by OINV
n IFS   Inversion Function Swap
   Ÿ 0   OINV/EINV=0 when data is inverted
   Ÿ 1   OINV/EINV=1 when data is inverted
n IFE   Inversion Function Enable
   Ÿ 0   Disable
   Ÿ 1   Enable. When enabled, an indication is output for each data bus. If the number of

transitions from pixel to pixel exceed 24 bits from 48 bits (or 18 bits from 36 bits for 6 bits panel), the data is inverted and an indication corresponding to that bus is set active.

n DPFS   Data Polarity Function Swap (useful when DPFE=1)
  Ÿ 0   Odd data inversion determined by OPOL, even data inversion determined by EPOL
  Ÿ 1   Odd data inversion determined by OPOL, even data opposite of ODD data
n DPFC   Data Polarity Function Control
  Ÿ 0   Data Inversion when OPOL/EPOL is 0
  Ÿ 1   Data Inversion when OPOL/EPOL is 1
n DPFE   Data Polarity Function Enable
  Ÿ 0   Disable
  Ÿ 1   Enable (line inversion, use OPOL/EPOL to determine the polarity of the output data)
n EEF   Early End Function
  Ÿ 0   Disable
  Ÿ 1   Enable
n TCEN   Timing Controller Enable
  Ÿ 0   Disable
  Ÿ 1   Enable

Output Format Control 2 (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
03h	OFC2	ESPP	ESPO[3:0]			OSPP	OSPO[3:0]			R/W

n ESPP   Even Start Pulse Position
  Ÿ 0   Start pulse before data
  Ÿ 1   Start pulse after data
n ESPO[2:0] Even Start Pulse Offset
  Ÿ 000   Start pulse 0 clocks before/after data
  Ÿ 001   Start pulse 1 clocks before/after data
  Ÿ 010   Start pulse 2 clocks before/after data
  Ÿ ...   ...
  Ÿ 111   Start pulse 7 clocks before/after data
n OSPP   Odd Start Pulse Position
  Ÿ 0   Start pulse before data
  Ÿ 1   Start pulse after data
n OSPO[2:0] Odd Start Pulse Offset
  Ÿ 000   Start pulse 0 clocks before/after data
  Ÿ 001   Start pulse 1 clocks before/after data
  Ÿ 010   Start pulse 2 clocks before/after data
  Ÿ ...   ...
  Ÿ 111   Start pulse 7 clocks before/after data

Output Drive/Polarity Control (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
04h	ODPC	OESPDC[1:0]		GODC[1:0]		ECP	-	OCP	-	R/W

n OESPDC[1:0]   OSP/ESP Drive Control
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA
n GODC[1:0]   OPOL/EPOL/GPO Drive Control
  Ÿ 00   4 mA
  Ÿ 01   6 mA
  Ÿ 10   8 mA
  Ÿ 11   12 mA

n ECP   ECLK Polarity
   Ÿ 0   Normal
   Ÿ 1   Inverted
n OCP   OCLK Polarity
   Ÿ 0   Normal
   Ÿ 1   Inverted

Output Drive Control (TCON feature only)									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
05h	ODC	EDDC[1:0]		ODDC[1:0]		-	-	RSBMLSW	RSAMLSW	R/W

n EIDC[1:0]   EINV Drive Control
   Ÿ 00   4 mA
   Ÿ 01   6 mA
   Ÿ 10   8 mA
   Ÿ 11   12 mA
n OIDC[1:0]   OINV Drive Control
n RSBMLSW   RSDS B-port MSB/LSB Swap
Ÿ Scaler Bank 0x42[5]=0 & 0x42[2]=1
   Ÿ 0   Default
   Ÿ 1   B-port MSB/LSB swap for 8-bit RSDS output
Ÿ Scaler Bank 0x42[5]=1 & 0x42[2]=1
   Ÿ 0   Default
   Ÿ 1   B-port MSB/LSB swap for 6-bit RSDS output
n RSAMLSW   RSDS A-port MSB/LSB Swap
Ÿ Scaler Bank 0x42[5]=0 & 0x42[3]=1
   Ÿ 0   Default
   Ÿ 1   A-port MSB/LSB swap for 8-bit RSDS output
Ÿ Scaler Bank 0x42[5]=1 & 0x42[3]=1
   Ÿ 0   Default
   Ÿ 1   A-port MSB/LSB swap for 6-bit RSDS output

GPO4 (OE) Active Delay Frame (TCON feature only)									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
06h	GPO4ADF	-					GPO4ADF[2:0]			R/W

n GPO4ADF[2:0]   GPO4 (OE) Active Delay Frame
   Ÿ 000   No delay
   Ÿ 001   Delay 1 frame
   Ÿ ...   ...
   Ÿ 111   Delay 7 frame

Input Format Control									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
07h	IFCTRL	WDG	PUA	G0AT	-	DATI	POLB	SPB	CLKB	R/W

n WDG   White Data Generation (TCON feature only)
   Ÿ 0   Black data generation during vertical blanking (GPOA)
   Ÿ 1   Enable white data generation during vertical blanking (GPOA)
n PUA   Power-up Active (TCON feature only)
   Ÿ 0   Outputs in-active
   Ÿ 1   Outputs active
n G0AT   GPO0 Auto Toggle Control (TCON feature only)
   Ÿ 0   Disable
   Ÿ 1   Enable
n DATI   Data Invert (TCON feature only)

Ÿ 0   OFF
Ÿ 1   ON
n POLB   Polarity Blanked Enable (TCON feature only)
Ÿ 0   Disable
Ÿ 1   Enable (EPOL/OPOL will be forced to blanked when GPOA is low)
n SPB   Start Pulse Blanked Enable (TCON feature only)
Ÿ 0   Disable
Ÿ 1   Enable (ESP/OSP will be forced to blanked when GPOA is low)
n CLKB   Clock Blanked Enable
Ÿ 0   Disable
Ÿ 1   Enable (ECLK/OCLK will be forced to blanked when GPOA is low)

GPO0 (OPOL) (TCON feature only)									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
08h	G0VST-L	G0VST[7:0]								R/W
09h	G0VST-H	-					G0VST[10:8]			R/W
0Ah	G0VEND-L	G0VEND[7:0]								R/W
0Bh	G0VEND-H	-					G0VEND[10:8]			R/W
0Ch	G0HST-L	G0HST[7:0]								R/W
0Dh	G0HST-H	-					G0HST[10:8]			R/W
0Eh	G0HEND-L	G0HEND[7:0]								R/W
0Fh	G0HEND-H	-					G0HEND[10:8]			R/W
10h	G0CTRL	G0CS[2:0]			G0TS[1:0]		G0ES	G0TC	G0OP	R/W

n G0VST[10:0]   Line number that GPO0 start
n G0VEND[10:0]   Line number that GPO0 end
n G0HST[10:0]   Pixel number that GPO0 start
n G0HEND[10:0]   Pixel number that GPO0 end
n G0TS[1:0]   GPO0 Type Select
Ÿ When Toggle Mode=0
Ÿ 00   Normal
Ÿ 01   Duration is greater than a line time
Ÿ 10   Every two lines has one GPO0 pulse
Ÿ 11   Every three lines has one GPO0 pulse
Ÿ When Toggle Mode=1
Ÿ 00   One Line Toggle
Ÿ 01   Reserved
Ÿ 10   Two Lines Toggle
Ÿ 11   Three Lines Toggle
n G0CS[2:0]   GPO0 Combination Select
Ÿ 000   No combination
Ÿ 001   AND
Ÿ 010   OR
Ÿ 011   Select GPO# and GPO#-1 on alternating frames
Ÿ 1xx   Auto select 1 or 2 line toggle according to ATP value
n G0ES   GPO0 Early Start Function
Ÿ 0   Normal
Ÿ 1   Early Start capability
Ÿ   The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frame to determine the Vertical Start position.
n G0TC   GPO0 Toggle circuit enable
Ÿ 0   Normal
Ÿ 1   Toggle
Ÿ   Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in

the vertical duration when in toggle mode.

- **n** G0OP   GPO0 Output Polarity
  - Ÿ 0   Active High
  - Ÿ 1   Active Low

GPO1 (EPOL) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
11h	G1VST-L	G1VST[7:0]								R/W
12h	G1VST-H	-					G1VST[10:8]			R/W
13h	G1VEND-L	G1VEND[7:0]								R/W
14h	G1VEND-H	-					G1VEND[10:8]			R/W
15h	G1HST-L	G1HST[7:0]								R/W
16h	G1HST-H	-					G1HST[10:8]			R/W
17h	G1HEND-L	G1HEND[7:0]								R/W
18h	G1HEND-H	-					G1HEND[10:8]			R/W
19h	G1CTRL	G1CS[2:0]			G1TS[1:0]		G1ES	G1TC	G1OP	R/W

- **n** G1VST[10:0]   Line number that GPO1 start
- **n** G1VEND[10:0]   Line number that GPO1 end
- **n** G1HST[10:0]   Pixel number that GPO1 start
- **n** G1HEND[10:0]   Pixel number that GPO1 end
- **n** G1TS[1:0]   GPO1 Type Select
- **n** G1CS[2:0]   GPO1 Combination Select
- **n** G1ES   GPO1 Early Start Function
- **n** G1TC   GPO1 Toggle circuit enable
- **n** G1OP   GPO1 Output Polarity

GPO2 (RSP2) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
1Ah	G2VST-L	G2VST[7:0]								R/W
1Bh	G2VST-H	-					G2VST[10:8]			R/W
1Ch	G2VEND-L	G2VEND[7:0]								R/W
1Dh	G2VEND-H	-					G2VEND[10:8]			R/W
1Eh	G2HST-L	G2HST[7:0]								R/W
1Fh	G2HST-H	-					G2HST[10:8]			R/W
20h	G2HEND-L	G2HEND[7:0]								R/W
21h	G2HEND-H	-					G2HEND[10:8]			R/W
22h	G2CTRL	G2CS[2:0]			G2TS[1:0]		G2ES	G2TC	G2OP	R/W

- **n** G2VST[10:0]   Line number that GPO2 start
- **n** G2VEND[10:0]   Line number that GPO2 end
- **n** G2HST[10:0]   Pixel number that GPO2 start
- **n** G2HEND[10:0]   Pixel number that GPO2 end
- **n** G2TS[1:0]   GPO2 Type Select
- **n** G2CS[2:0]   GPO2 Combination Select
- **n** G2ES   GPO2 Early Start Function
- **n** G2TC   GPO2 Toggle circuit enable
- **n** G2OP   GPO2 Output Polarity

GPO3 (RSP3) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
23h	G3VST-L	G3VST[7:0]								R/W
24h	G3VST-H	-					G3VST[10:8]			R/W
25h	G3VEND-L	G3VEND[7:0]								R/W

GPO3 (RSP3) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
26h	G3VEND-H	-					G3VEND[10:8]			R/W
27h	G3HST-L	G3HST[7:0]								R/W
28h	G3HST-H	-					G3HST[10:8]			R/W
29h	G3HEND-L	G3HEND[7:0]								R/W
2Ah	G3HEND-H	-					G3HEND[10:8]			R/W
2Bh	G3CTRL	G3CS[2:0]			G3TS[1:0]		G3ES	G3TC	G3OP	R/W

- **n** G3VST[10:0]   Line number that GPO3 start
- **n** G3VEND[10:0]   Line number that GPO3 end
- **n** G3HST[10:0]   Pixel number that GPO3 start
- **n** G3HEND[10:0]   Pixel number that GPO3 end
- **n** G3TS[1:0]   GPO3 Type Select
- **n** G3CS[2:0]   GPO3 Combination Select
- **n** G3ES   GPO3 Early Start Function
- **n** G3TC   GPO3 Toggle circuit enable
- **n** G3OP   GPO3 Output Polarity

GPO4 (RCLK) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
2Ch	G4VST-L	G4VST[7:0]								R/W
2Dh	G4VST-H	-					G4VST[10:8]			R/W
2Eh	G4VEND-L	G4VEND[7:0]								R/W
2Fh	G4VEND-H	-					G4VEND[10:8]			R/W
30h	G4HST-L	G4HST[7:0]								R/W
31h	G4HST-H	-					G4HST[10:8]			R/W
32h	G4HEND-L	G4HEND[7:0]								R/W
33h	G4HEND-H	-					G4HEND[10:8]			R/W
34h	G4CTRL	G4CS[2:0]			G4TS[1:0]		G4ES	G4TC	G4OP	R/W

- **n** G4VST[10:0]   Line number that GPO4 start
- **n** G4VEND[10:0]   Line number that GPO4 end
- **n** G4HST[10:0]   Pixel number that GPO4 start
- **n** G4HEND[10:0]   Pixel number that GPO4 end
- **n** G4TS[1:0]   GPO4 Type Select
- **n** G4CS[2:0]   GPO4 Combination Select
- **n** G4ES   GPO4 Early Start Function
- **n** G4TC   GPO4 Toggle circuit enable
- **n** G4OP   GPO4 Output Polarity

GPO5 (ROE) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
35h	G5VST-L	G5VST[7:0]								R/W
36h	G5VST-H	-					G5VST[10:8]			R/W
37h	G5VEND-L	G5VEND[7:0]								R/W
38h	G5VEND-H	-					G5VEND[10:8]			R/W
39h	G5HST-L	G5HST[7:0]								R/W
3Ah	G5HST-H	-					G5HST[10:8]			R/W
3Bh	G5HEND-L	G5HEND[7:0]								R/W
3Ch	G5HEND-H	-					G5HEND[10:8]			R/W
3Dh	G5CTRL	G5CS[2:0]			G5TS[1:0]		G5ES	G5TC	G5OP	R/W

- **n** G5VST[10:0]   Line number that GPO5 start
- **n** G5VEND[10:0]   Line number that GPO5 end

- **n** G5HST[10:0]   Pixel number that GPO5 start
- **n** G5HEND[10:0]   Pixel number that GPO5 end
- **n** G5TS[1:0]   GPO5 Type Select
- **n** G5CS[2:0]   GPO5 Combination Select
- **n** G5ES   GPO5 Early Start Function
- **n** G5TC   GPO5 Toggle circuit enable
- **n** G5OP   GPO5 Output Polarity

GPO6 (ROE2) (TCON feature only)									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
3Eh	G6VST-L	G6VST[7:0]								R/W
3Fh	G6VST-H	-					G6VST[10:8]			R/W
40h	G6VEND-L	G6VEND[7:0]								R/W
41h	G6VEND-H	-					G6VEND[10:8]			R/W
42h	G6HST-L	G6HST[7:0]								R/W
43h	G6HST-H	-					G6HST[10:8]			R/W
44h	G6HEND-L	G6HEND[7:0]								R/W
45h	G6HEND-H	-					G6HEND[10:8]			R/W
46h	G6CTRL	G6CS[2:0]			G6TS[1:0]			G6ES	G6TC	G6OP	R/W

- **n** G6VST[10:0]   Line number that GPO6 start
- **n** G6VEND[10:0]   Line number that GPO6 end
- **n** G6HST[10:0]   Pixel number that GPO6 start
- **n** G6HEND[10:0]   Pixel number that GPO6 end
- **n** G6TS[1:0]   GPO6 Type Select
- **n** G6CS[2:0]   GPO6 Combination Select
- **n** G6ES   GPO6 Early Start Function
- **n** G6TC   GPO6 Toggle circuit enable
- **n** G6OP   GPO6 Output Polarity

GPO7 (ROE3) (TCON feature only)									
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
47h	G7VST-L	G7VST[7:0]								R/W
48h	G7VST-H	-					G7VST[10:8]			R/W
49h	G7VEND-L	G7VEND[7:0]								R/W
4Ah	G7VEND-H	-					G7VEND[10:8]			R/W
4Bh	G7HST-L	G7HST[7:0]								R/W
4Ch	G7HST-H	-					G7HST[10:8]			R/W
4Dh	G7HEND-L	G7HEND[7:0]								R/W
4Eh	G7HEND-H	-					G7HEND[10:8]			R/W
4Fh	G7CTRL	G7CS[2:0]			G7TS[1:0]			G7ES	G7TC	G7OP	R/W

- **n** G7VST[10:0]   Line number that GPO7 start
- **n** G7VEND[10:0]   Line number that GPO7 end
- **n** G7HST[10:0]   Pixel number that GPO7 start
- **n** G7HEND[10:0]   Pixel number that GPO7 end
- **n** G7TS[1:0]   GPO7 Type Select
- **n** G7CS[2:0]   GPO7 Combination Select
- **n** G7ES   GPO7 Early Start Function
- **n** G7TC   GPO7 Toggle circuit enable
- **n** G7OP   GPO7 Output Polarity

GPO8 (DHS/TCON_LP) (TCON feature only)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
50h	G8VST-L	G8VST[7:0]								R/W
51h	G8VST-H	-					G8VST[10:8]			R/W
52h	G8VEND-L	G8VEND[7:0]								R/W
53h	G8VEND-H	-					G8VEND[10:8]			R/W
54h	G8HST-L	G8HST[7:0]								R/W
55h	G8HST-H	-					G8HST[10:8]			R/W
56h	G8HEND-L	G8HEND[7:0]								R/W
57h	G8HEND-H	-					G8HEND[10:8]			R/W
58h	G8CTRL	G8CS[2:0]			G8TS[1:0]			G8ES	G8TC	G8OP	R/W

n G8VST[10:0]
Ÿ When Scalar bank register ABh bit 7 = 0
   Ÿ G8VST[10:0]   Line number that GPO8 start
Ÿ When Scalar bank register ABh bit 7 = 1
   Ÿ G8VST-L[7:0]   GPO[7:0] gating control
   Ÿ G8VST-H[1:0]   O(E)SP / O(E)INV gating control
n G8VEND[10:0]   Line number that GPO8 end
n G8HST[10:0]   Pixel number that GPO8 start
n G8HEND[10:0]   Pixel number that GPO8 end
n G8TS[1:0]   GPO8 Type Select
n G8CS[2:0]   GPO8 Combination Select
n G8ES   GPO8 Early Start Function
n G8TC   GPO8 Toggle circuit enable
n G8OP   GPO8 Output Polarity

GPO9 (DVS/TCON_FSYNC)

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
59h	G9VST-L	G9VST[7:0]								R/W
5Ah	G9VST-H	-					G9VST[10:8]			R/W
5Bh	G9VEND-L	G9VEND[7:0]								R/W
5Ch	G9VEND-H	-					G9VEND[10:8]			R/W
5Dh	G9HST-L	G9HST[7:0]								R/W
5Eh	G9HST-H	-					G9HST[10:8]			R/W
5Fh	G9HEND-L	G9HEND[7:0]								R/W
60h	G9HEND-H	-					G9HEND[10:8]			R/W
61h	G9CTRL	G9CS[2:0]			G9TS[1:0]			G9ES	G9TC	G9OP	R/W

n G9VST[10:0]   Line number that GPO9 start
n G9VEND[10:0]   Line number that GPO9 end
n G9HST[10:0]   Pixel number that GPO9 start
n G9HEND[10:0]   Pixel number that GPO9 end
n G9TS[1:0]   GPO9 Type Select
n G9CS[2:0]   GPO9 Combination Select
n G9ES   GPO9 Early Start Function
n G9TC   GPO9 Toggle circuit enable
n G9OP   GPO9 Output Polarity

GPOA

Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
62h	GAVST-L	GAVST[7:0]								R/W
63h	GAVST-H	-					GAVST[10:8]			R/W
64h	GAVEND-L	GAVEND[7:0]								R/W

GPOA										
Index	Mnemonic	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
65h	GAVEND-H	-					GAVEND[10:8]			R/W
66h	GAHST-L	GAHST[7:0]								R/W
67h	GAHST-H	-					GAHST[10:8]			R/W
68h	GAHEND-L	GAHEND[7:0]								R/W
69h	GAHEND-H	-					GAHEND[10:8]			R/W
6Ah	GACTRL	GACS[2:0]			GATS[1:0]		GAES	GATC	GAOP	R/W

n GAVST[10:0]   Line number that GPOA start
n GAVEND[10:0]   Line number that GPOA end
n GAHST[10:0]   Pixel number that GPOA start
n GAHEND[10:0]   Pixel number that GPOA end
n GATS[1:0]   GPOA Type Select
n GACS[2:0]   GPOA Combination Select
n GAES   GPOA Early Start Function
n GATC   GPOA Toggle circuit enable
n GAOP   GPOA Output Polarity

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
03/10/03	ADC	Ÿ 0x2D
	Scaler	Ÿ 0xAB
	TCON	Ÿ 0x05
04/01/03	ADC	Ÿ 0x13, 0x15, 0x17, 0x18, 0x26, 0x27, 0x2D
	Scaler	Ÿ 0x04, 0x44, 0x4B, 0x50~0x55, 0x5D, 0x89, 0x8A, 0x90, 0x9F, 0xB3, 0xB4, 0xBC, 0xCA, 0xCC, 0xCD, 0xD1, 0xD4, 0xEA, 0xF2, 0xF6, 0xF8 Ÿ 0xFA (deleted)
	OSD	Ÿ 0x01, 0x0E, 0x10
04/02/03	Scaler	Ÿ 0x88
05/02/03	Scaler	Ÿ 0x44