

**FEATURES**

- 3.3V power supply
- 1.9ns typical propagation delay
- 275MHz  $f_{MAX}$  (Clock bit stream, not pseudo-random)
- Differential LVPECL inputs
- 24mA LVTTL outputs
- Flow-through pinouts
- Internal input resistors: pulldown on D, pulldown and pullup on /D
- Q output will default LOW with inputs open or at GND
- $V_{BB}$  output
- Available in 8-pin MSOP and SOIC package

**DESCRIPTION**

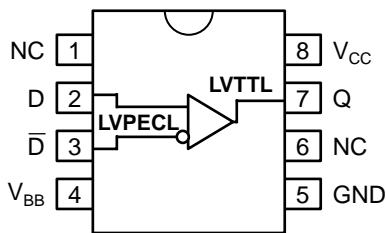
The SY100EPT21L is a single differential LVPECL-to-LVTTL translator using a single +3.3V power supply. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the EPT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

$V_{BB}$  allows a differential, single-ended, or AC-coupled interface to the device. If used, the  $V_{BB}$  output should be bypassed to  $V_{CC}$  with 0.01 $\mu$ F capacitor.

Under open input conditions, the /D will be biased at a  $V_{CC}/2$  voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

The 100EPT is compatible with positive ECL 100K logic levels.

**PIN CONFIGURATION/BLOCK DIAGRAM**



(Available in 8-pin SOIC and 8-pin MSOP)

**PIN NAMES**

Pin	Function
Q	LVTTL Output
D, /D	Differential LVPECL Input Pair
$V_{CC}$	Positive Supply
$V_{BB}$	Output Reference Voltage
GND	Ground

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage	-0.5 to +3.8	V
$V_I$	PECL Input Voltage	0V to $V_{CC}+0.5$	V
$V_O$	Voltage Applied to Output at HIGH State	-0.5 to $V_{CC}$	V
$I_O$	Current Applied to Output at LOW State	Twice the Rated $I_{OL}$	mA
$T_{store}$	Storage Temperature	-65 to +150	°C
$T_A$	Operating Temperature	-40 to +85	°C

**TRUTH TABLE**

D	/D	Q
L	H	L
H	L	H
Open	Open	L

**NOTE:**

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**LV TTL DC ELECTRICAL CHARACTERISTICS**

$$V_{CC} = +3.3V \pm 5\%$$

Symbol	Parameter	$T_A = -40^\circ\text{C}$		$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
$I_{OS}$	Output Short Circuit Current	-80	-275	-80	-275	-80	—	-275	-80	-275	mA	$V_{OUT} = 0V$
$I_{CC}$	Power Supply Current	—	20	—	20	—	14	20	—	20	mA	
$V_{OH}$	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V	$I_{OH} = -3.0\text{mA}$
$V_{OL}$	Output LOW Voltage	—	0.5	—	0.5	—	—	0.5	—	0.5	V	$I_{OL} = 24\text{mA}$

**LVPECL DC ELECTRICAL CHARACTERISTICS**

$$V_{CC} = +3.3V \pm 5\%$$

Symbol	Parameter	$T_A = -40^\circ\text{C}$		$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$		Unit	Condition	
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
$I_{IH}$	Input HIGH Current	—	150	—	150	—	—	150	—	150	$\mu\text{A}$		
$I_{IL}$	Input LOW Current	D	0.5	—	0.5	—	0.5	—	—	0.5	—	$\mu\text{A}$	
		/D	-300	—	-300	—	-300	—	—	-300	—		
$V_{IH}$	Input HIGH Voltage <sup>(2)</sup> 100EPT	2135	2420	2135	2420	2135	—	2420	2135	2420			
$V_{IL}$	Input LOW Voltage <sup>(2)</sup> 100EPT	1490	1825	1490	1825	1490	—	1825	1490	1825			
$V_{BB}$	Reference Output <sup>(2)</sup> 100EPT	1920	2040	1920	2040	1920	1980	2040	1920	2040			

**NOTES:**

- These values are for  $V_{CC} = 3.3V$ . Level Specifications will vary 1:1  $V_{CC}$ .

## AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = +3.3V \pm 5\%$ 

Symbol	Parameter	TA = -40°C		TA = 0°C		TA = +25°C			TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	1.5	2.5	1.5	2.5	1.5	1.9	2.5	1.5	2.5	ns	C <sub>L</sub> = 20pF
t <sub>skpp</sub>	Part-to-Part Skew <sup>(1,2)</sup>	—	0.5	—	0.5	—	—	0.5	—	0.5	ns	C <sub>L</sub> = 20pF
f <sub>MAX</sub>	Maximum Input Frequency <sup>(3,4)</sup>	275	—	275	—	275	—	—	275	—	MHz	C <sub>L</sub> = 20pF
V <sub>CMR</sub>	Common Mode Range	1.2	V <sub>CC</sub>	1.2	V <sub>CC</sub>	1.2	—	V <sub>CC</sub>	1.2	V <sub>CC</sub>	V	
V <sub>PP</sub>	Minimum Peak-to-Peak Input <sup>(5)</sup>	100	—	100	—	100	—	—	100	—	mV	
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Time (1.0V to 2.0V)	0.5	1.0	0.5	1.0	0.5	—	1.0	0.5	1.0	ns	C <sub>L</sub> = 20pF

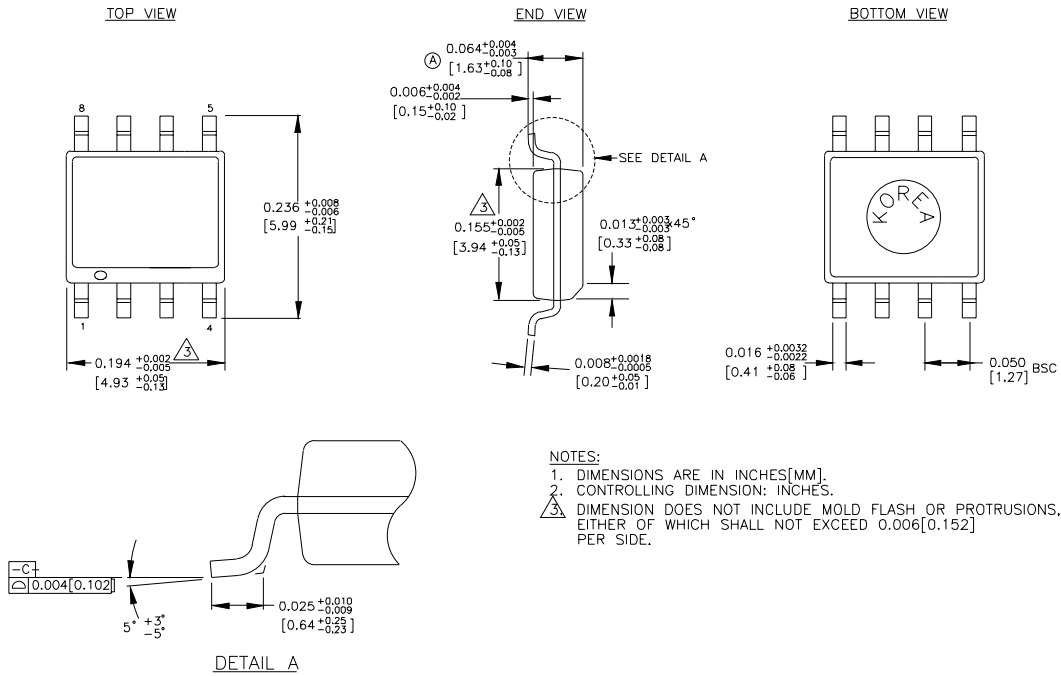
### NOTES:

1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common V<sub>CC</sub> level.
2. These parameters are guaranteed but not tested.
3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
4. The f<sub>MAX</sub> value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.
5. 100mV input guarantees full logic at output.

## PRODUCT ORDERING CODE

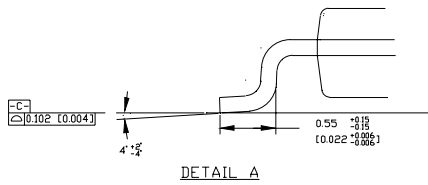
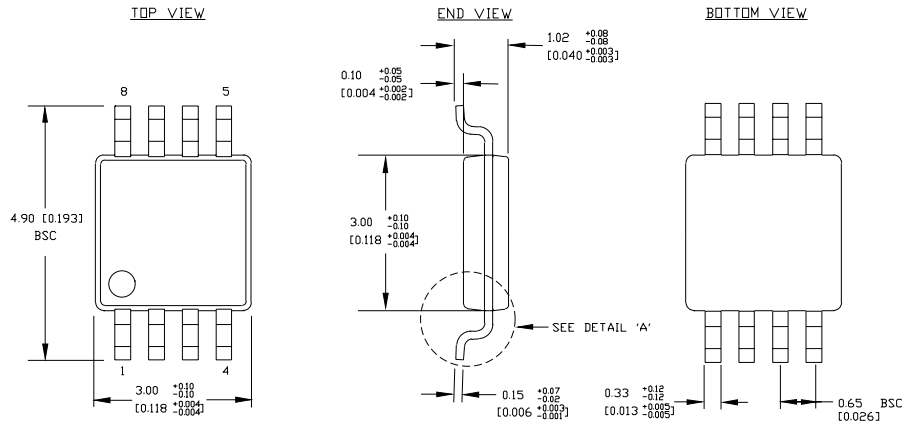
Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY100EPT21LZC	Z8-1	Commercial	+3.3V ±5%
SY100EPT21LZCTR	Z8-1	Commercial	+3.3V ±5%
SY100EPT21LKC	K8-1	Commercial	+3.3V ±5%
SY100EPT21LKCTR	K8-1	Commercial	+3.3V ±5%

**8 LEAD PLASTIC SOIC (Z8-1)**



Rev.03

**8 LEAD MSOP (K8-1)**



- NOTES:**
1. DIMENSIONS ARE IN MM [INCHES].
  2. CONTROLLING DIMENSION: MM
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

Rev. 01





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